# KCU105 10GBASE-R Ethernet TRD User Guide

# KUCon-TRD04

Vivado Design Suite

UG921 (v2017.3) October 9, 2017





## **Revision History**

The following table shows the revision history for this document.

Date	Version	Revision
10/09/2017	2017.3	Updated text for Vivado Design Suite version 2017.3. Updated Table 1-1 rows for CLB LUTs and CLB Registers. Added Table A-1.
07/13/2017	2017.2	Updated text for Vivado Design Suite version 2017.2. Added Documentation Navigator and Design Hubs to Appendix E, .
05/08/2017	2017.1	Updated text and graphics for Vivado Design Suite version 2017.1. Updated Table 1-1 rows for CLB LUTs and CLB Registers.
12/15/2016	2016.4	Updated for Vivado Design Suite version 2016.4. Updated Table 1-1, Figure 4-8, and Figure 4-9.
10/25/2016	2016.3	Updated for Vivado Design Suite version 2016.3. Updated Table 1-1. Updated Appendix E, Additional Resources and Legal Notices.
06/08/2016	2016.2	Updated all references to Vivado Design Suite version 2016.1 to 2016.2. Revised the resource numbers in Table 1-1.
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04/27/2015	2015.1	Updated all references to Vivado Design Suite version 2014.4.1 to 2015.1.
02/25/2015	2014.4.1	Initial Xilinx Release.



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# XILINX

# Introduction

This document describes the features and functions, and how to setup, operate, test, and modify the 10GBASE-R Ethernet targeted reference design (10GBASE-R TRD).

## **10GBASE-R TRD Overview**

The 10GBASE-R TRD targets the Kintex® UltraScale<sup>™</sup> XCKU040-2FFVA1156E FPGA running on the KCU105 evaluation board. It demonstrates 10-Gigabit Ethernet connectivity using 10-Gigabit Ethernet PCS/PMA IP (10GBASE-R) and 10-Gigabit Ethernet MAC IP (10G MAC) cores on two channels. The data source for these channels can be configured to be either from an internal or external Traffic Generator. Figure 1-1 shows the 10GBASE-R TRD block diagram.



Figure 1-1: The 10GBASE-R TRD Environment



The design has two 10 Gb/s Ethernet channels; channel 0 and channel 1. Data from one channel is looped to the other as shown in Figure 1-1. Internal generator mode and external generator mode are supported:

- **Internal generator mode**. In this mode, the Traffic Generator block generates the transmit data. The data is looped back on the PHY side using fiber optic cables. The looped-back data becomes the receive data on the other channel and is verified by the 10-Gigabit Ethernet MAC core.
- **External generator mode**. In this mode, an external generator generates the data. Appendix D describes using an external Ixia NGY-NP4-01 10-Gigabit application network processor load module (Ixia load module). The data received by the 10-Gigabit Ethernet MAC IP core is looped back in the Traffic Generator block and passed as transmit data to the other 10-Gigabit Ethernet MAC IP core. The Ixia load module verifies this data when received.

A MicroBlaze<sup>™</sup> processor-based subsystem monitors the 10-Gigabit Ethernet MAC IP core statistics and passes the information to the Ethernet Controller application (GUI) running on the control computer using the USB-to-UART port on the KCU105 board. This subsystem also controls the Traffic Generator and monitors Ethernet performance.

#### **Components, Features, and Functions**

The 10GBASE-R TRD includes:

- 10-Gigabit Ethernet PCS/PMA IP core:
  - Uses a GTH transceiver (GTHE3) running at 10.3125 Gb/s line rate.
  - Provides a single data rate (SDR) 10-Gigabit Ethernet Media Independent Interface (XGMII) which connects to the 10-Gigabit Ethernet MAC IP core. The XGMII interface runs at 156.25 MHz and the data path is 64-bits wide.
  - Serial interface to fiber-optic connections.
- 10-Gigabit Ethernet MAC IP core:
  - Connects to the 10-Gigabit Ethernet PCS/PMA IP core using the XGMII interface
  - Provides AXI4-Stream protocol support on the user interface running at 156.25 MHz
  - Is monitored through an AXI4-Lite interface
- Traffic Generator and Monitor:
  - Generates Ethernet traffic or loops back Ethernet traffic selected by user input
  - Monitors bandwidth utilization on the transmit and receive AXI4-Stream interfaces of the 10-Gigabit Ethernet MAC IP core
  - Is configured and monitored through an AXI4-Lite interface



- System Management Wizard:
  - Uses the UltraScale<sup>™</sup> architecture System Monitor (SYSMON) block to monitor FPGA temperature, voltages and currents
  - Is configured and monitored through an AXI4-Lite interface
- AXI UART Lite:
  - Provides the controller interface for asynchronous serial data transfer. This interface connects to the USB-to-UART port on the KCU105 board, and is used to communicate with the control computer.
  - Provides an AXI4-Lite interface on the other end to communicate with the MicroBlaze processor subsystem.
- MicroBlaze processor subsystem and AXI Interconnect:
  - Communicates with the 10-Gigabit Ethernet MAC IP core, Traffic Generator and Monitor, System Management wizard, and AXI UART Lite using the AXI4-Lite protocol.
  - Drivers running on the MicroBlaze processor subsystem interpret commands received from the Ethernet Controller application running on the control computer and convert them to AXI4-Lite transactions.
- Ethernet Controller application:
  - Provides a graphical user interface running on the control computer to pass user inputs to the 10GBASE-R TRD and to display status through the KCU105 board USB-to-UART port.

#### **Resource Utilization**

Table 1-1 lists the resources used by the 10GBASE-R TRD after synthesis has run. Place and route can alter these numbers based on placements and routing paths, so use these numbers as a rough estimate of resource utilization. These numbers might vary based on the version of the 10GBASE-R TRD and the tools used to regenerate the design.

Resource Type	Used	Available	Usage (%)
CLB LUTs	14,002	242,400	5.78
CLB Registers	16,7469	484,800	3.46
Block RAM Tiles	35	600	5.83
Global Clock Buffers	8	240	1.67
BUFG_GT_SYNC	4	55	7.27
BUFG_GT	7	120	5.83
GTHE3_CHANNEL	2	20	10.00

Table 1-1: 10GBASE-R TRD Resource Utilization



#### Table 1-1: 10GBASE-R TRD Resource Utilization (Cont'd)

Resource Type	Used	Available	Usage (%)
GTHE3_COMMON	1	5	20.00
SYSMONE1	1	1	100.00





# Setup

This chapter lists the requirements and describes how to do all preliminary setup of the KCU105 board, control computer, and software before bringing up the 10GBASE-R TRD.



**IMPORTANT:** Perform the procedures described in this chapter before performing the bring-up procedures described in Chapter 3, Bringing Up the Design.

## Requirements

#### Hardware

- KCU105 board with the Kintex® UltraScale<sup>™</sup> XCKU040-2FFVA1156E FPGA
- Two USB cables, standard-A plug to micro-B plug
- Power Supply: 100 VAC-240 VAC input, 12 VDC 5.0A output
- Two SFP+ 10GBASE-SR/SW transceiver modules (Avago Technologies)
- One LC-LC duplex 10 Gb multimode 50/125 OM3 fiber optic patch cable, 2 x LC Male to 2 x LC Male, part number FO-10GGBLCX20-001 (Amphenol Corporation)

#### Computer

One computer is required, and is identified as the control computer throughout this document. It is required for running the Vivado® Design Suite, configuring the FPGA, and running the Ethernet Controller application to control and monitor the reference design. It can be a laptop or desktop computer with Microsoft Windows 7 operating system.

#### **Design Tools and Software**

- Vivado Design Suite 2017.3
- USB UART drivers (Silicon Laboratories CP210x VCP drivers)
- Java version 1.7
- Ethernet Controller application (GUI included with the 10GBASE-R TRD)



Download and installation instructions for each required software is described in Preliminary Setup.

## **Preliminary Setup**

Complete these tasks before bringing up the design described in Chapter 3, Bringing Up the Design.

#### Install Vivado Design Suite

Install Vivado Design Suite 2017.3 on the control computer. Follow the installation instructions provided in *Vivado Design Suite User Guide Release Notes, Installation, and Licensing* (UG973) [Ref 1].

#### **Download Targeted Reference Design Files**

- 1. Download the 10GBASE-R TRD ZIP file rdf0308-kcu105-trd04-2017-3.zip from KCU105 Evaluation Kit Documentation.
- 2. Unzip the contents of the file to a working directory.
- 3. The unzipped contents will be located at <working\_dir>/kcu105\_10gbaser\_trd.

The 10GBASE-R TRD directory structure is described in Appendix A, Directory Structure.

#### Install the USB UART Drivers

Download the *CP210x USB to UART Bridge VCP drivers* (for Windows 7) from the Silicon Labs website [Ref 2]. Follow the instructions in *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)[Ref 3].



### **Configure the Control Computer COM Port**

The 10GBASE-R TRD uses the Ethernet Controller application to communicate between the control computer and the KCU105 board. To configure the control computer COM ports for this purpose:

1. Connect the KCU105 board to the control computer and power supply as shown in Figure 2-1.



Figure 2-1: Connection Diagram for Preliminary Setup

2. Power on the KCU105 board by placing switch SW1 to the ON position (SW1 in Figure 2-1).



3. Open the control computer Device Manager (Figure 2-2). In the Windows task bar, click **Start**, click **Control Panel**, and then click **Device Manager**.

🚔 Device Manager	x				
File Action View Help					
🕞 🖳 Monitors	•				
A 📲 Network adapters					
Bluetooth Device (Personal Area Network)					
🛐 Cisco Systems VPN Adapter for 64-bit Windows	_				
Intel(R) 82579LM Gigabit Network Connection					
👰 Intel(R) Centrino(R) Ultimate-N 6300 AGN					
VirtualBox Host-Only Ethernet Adapter					
A TT Ports (COM & LPT)					
Communications Port (COM1)					
ECP Printer Port (LPT1)					
Intel(R) Active Management Technology - SOL (COM3)					
Silicon Labs Dual CP210x USB to UART Bridge: Standard COM Port (COM19)					
Processors					
> 📋 Smart card readers					
Sound, video and game controllers					
Storage controllers	Ψ.				

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 In the Device Manager window (Figure 2-2), expand Ports (COM & LPT), right-click Silicon Labs CP210x USB to UART Bridge: Standard COM Port, and then click Properties.



- 5. In the properties window (Figure 2-3), select the Port Settings tab.
- 6. Set **Bits per second**, **Data bits**, **Parity**, **Stop bits**, and **Flow control** to the values shown in Figure 2-3, and click **OK**.

Silicon Labs Dual CP210x USB to UART Bridge: Standard COM Por
General Port Settings Driver Details Power Management
Bits per second: 115200
Data bits: 8
Parity: None 💌
Stop bits: 1
Flow control: None
Advanced Restore Defaults
OK Cancel

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#### Install Java 1.7

Installation of Java 1.7 is required for the Ethernet Controller Application.

Download Java SE Runtime Environment 7 from Oracle and install it on the control computer. Follow the installation instructions provided with the software.

#### Install the Ethernet Controller Application

The Ethernet Controller application is a Java-based application, so confirm Java has been installed as described in Install Java 1.7.



1. Browse to <working\_dir>/kcu105\_10gbaser\_trd/software/GUI (Figure 2-4).

a Edit View Tools	Help	logbaser_dd y sontware y oor			-
)rganize 🔻 Include in	library	Share with       Share with      Share with	der		
	-	Name	Date modified	Туре	Size
E Desktop		SethernetController-32-installer	5/1/2014 6:47 PM	Application	2,848 KB
🚺 Downloads		EthernetController-64-installer	5/1/2014 6:46 PM	Application	2,850 KB
🔒 Libraries					
<ul> <li>Documents</li> <li>Music</li> <li>Pictures</li> <li>Videos</li> <li>Computer</li> </ul>					

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*Figure 2-4:* **Directory Location, Ethernet Controller Installer** 

2. Right-click either the **EthernetController-32-installer** (for a 32-bit operating system) or **EthernetController-64-installer** (for a 64-bit operating system) and click **Run as administrator** (Figure 2-4).



- 3. Click **Yes** in the dialog box that opens.
- 4. In the License Agreement display (Figure 2-5), click **I Agree** to continue installation.

Xilinx - EthernetController Setup: License Agreement					
Please review the license agreement before installing Xilinx - EthernetController. If you accept all terms of the agreement, click I Agree.					
PART I					
CAREFULLY READ THIS END USER LICENSE AGREEMENT ("AGREEMENT"). BY CLICKING THE "ACCEPT" OR "AGREE" BUTTON, OR OTHERWISE ACCESSING, DOWNLOADING, INSTALLING OR USING THE SOFTWARE, YOU AGREE ON BEHALF OF LICENSEE TO BE BOUND BY THIS AGREEMENT.					
IF LICENSEE DOES NOT AGREE TO ALL OF THE TERMS AND CONDITIONS OF THIS AGREEMENT, DO NOT CLICK THE "ACCEPT" OR "AGREE" BUTTON OR					
Cancel Nullsoft Install System v2,46 I Agree					
X19129-04181					

*Figure 2-5:* License Agreement

5. Browse to the location where the Ethernet Controller application will be installed and click **Install** (Figure 2-6).



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Figure 2-6: Ethernet Controller Installation Location



 $\bigcirc$ 

6. Click **Close** after installation is complete (Figure 2-7).

Xilinx - EthernetController Setup: Completed
Completed
Show <u>d</u> etails
Cancel Nullsoft Install System v2,46 < Back
X19125-041

Figure 2-7: Installation Complete

**TIP:** To uninstall the Ethernet Controller application after design bring-up, open the Control Panel. In the Control Panel, click **All Control Panel Items>Programs and Features** and uninstall program **"Xilinx Ethernet Controller - Powered by Xilinx**."

#### Ready to Bring Up the Design

After all procedures in this chapter are complete, go to Chapter 3, Bringing Up the Design.





# Bringing Up the Design

This chapter describes how to bring up the 10GBASE-R TRD by programming the FPGA with the bitstream and running the 10GBASE-R TRD under the control of the Ethernet Controller application. The procedure for running the internal Traffic Generators is provided at the end of this chapter.



**IMPORTANT:** Perform the preliminary setup procedures described in Chapter 2, Setup before performing the bring-up procedures described in this chapter.

### **Program the Board**

- 1. Connect the KCU105 board to the control computer and power supply as shown in Figure 3-1.
- 2. Insert the SFP+ modules into the SFP cage on the KCU105 board and the connect the fiber optic cables (also shown in Figure 3-1).
- 3. Set the KCU105 board switches and jumpers as shown in Figure 3-1.



Figure 3-1: Connection Diagram for Bring-Up



- 4. Power on the KCU105 board by placing switch SW1 to the ON position (SW1 in Figure 3-1).
- 5. Launch the Vivado Integrated Design Environment (IDE) on the control computer:
  - a. Select Start > All Programs > Xilinx Design Tools > Vivado 2017.3 > Vivado 2017.3.
  - b. On the getting started page, click **Open Hardware Manager** (Figure 3-2).



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Figure 3-2: Vivado IDE Getting Started Page, Open Hardware Manager



- 6. Open the connection wizard to initiate a connection to the KCU105 board:
  - a. Click **Open target** (Figure 3-3).



Figure 3-3: Using the User Assistance Bar to Open a Hardware Target

b. Configure the wizard to establish connection with the KCU105 board by selecting the default value on each wizard page. Click **Next > Next > Next > Finish**.



\$

- Q- Quick Access <u>F</u>ile <u>E</u>dit Tools Window Layout <u>V</u>iew <u>H</u>elp 🌣 ½ 🕖 X Dashboard -A HARDWARE MANAGER - localhost/xilinx\_tcf/Digilent/210308957978 Hardware ? \_ 🗆 🖒 X hw\_vios Q X 🗢 🖉 🕨 🚿 🔳 ۰ hw\_vio\_1 Name Status ard Options Q I Iocalhost (1) Connected Open v @ xcku040\_0 (2) Drogram Hardware Device Properties... Ctrl+E 🦉 SysMon (\$ 🦉 hw\_vio\_1 Program Device. Verify Device... C Refresh Device Add Configuration Memory Device... Boot from Configuration Memory Device < Program BBR Key ... Hardware Device Proper Clear BBR Key... xcku040\_0 Program eFUSE Registers... Export to Spreadsheet... Name: xcku Part: xcku040 ID code: 13822093 X19141-041817
- c. In the hardware view, right-click xcku040 and click Program Device (Figure 3-4).

Figure 3-4: Select Device to Program

**IMPORTANT:** There are no debug cores in this reference design. For this reason, WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3 can be ignored.



d. In the **Bitstream file** field, browse to the location of the BIT file:

```
<working_dir>/kcu105_10gbaser_trd/ready_to_test/kcu105_10gbase
r_download.bit
```

and click **Program** (Figure 3-5).

ptionally select a deb	ug probes file that corresponds to the debug cores contained in the	
itstream programmin	g file.	
Bitstre <u>a</u> m file:	<pre>FRD/UG921/2017.1/ready_to_test/kcu105_10gbaser_download.bi</pre>	t 🖂 🕂
Debu <u>q</u> probes file:		
✓ Enable end of s	tartup check	
2	Program	Cancel

Figure 3-5: Program Device Window

After completing these steps, continue on to Running the Design.



## **Running the Design**

#### Launch the Ethernet Controller Application

 Launch the Ethernet Controller application on the control computer. In Windows, click Start > All Programs > Xilinx > EthernetController (Figure 3-6).



Figure 3-6: Ethernet Controller Application



 Select the COM port associated with the Silicon Labs CP210x USB to UART Bridge and click **Connect** (Figure 3-7) to open the Ethernet Controller application for the 10GBASE-R TRD.



**TIP:** The COM port associated with the Silicon Labs CP210x USB to UART Bridge can be identified using the Windows Device Manager. See step 3, page 12.

🛃 Ethernet Cont	roller	
I	Ethernet Con	troller
COM Port:	COM1 COM1 COM3 COM18 COM19 LPT1	Refresh Connect

Figure 3-7: Select COM Port Associated with the USB to UART Bridge



#### **Running Internal Traffic Generators**

 Ethernet channel 0 and channel 1 are up and ready when the ETH0 PHY and ETH1 PHY indicators are green (Figure 3-8). In the control panel for both channel 0 and channel 1, select **Internal Generator** and enter **1500** in the payload field, and click **Start** for both channels.

10GBASE-R Ethernet TRD			×
<b>E</b> XILINX	KUCon-TRD04 10GBASE-R Etherne	et Targeted Reference Design	Block diagram
ALL PROGRAMMABLES			
Performance Plots Channel 0 Statistics	Channel 1 Statistics Power Plots		
Channel 0		Channel 1	
Control Panel		Control Panel	
Internal Generator	_	Internal Generator     Pavload: 1500	Start
Payload: 1500 External Generator	Start	External Generator	Statt
Tx Statistics	Rx Statistics	Tx Statistics Rx Statistics	
Throughput (Gbps): 0.00	Throughput (Gbps): 0.00	Throughput (Gbps): 0.00 Throughput (Gbps):	0.00
Packet Count: 0	Packet Count: 0	Packet Count: 0 Packet Count	0
(sdq) 7.5 10.0 7.5 10.0 2.5 0.0 1 2 3 T T Throu	4 5 6 7 8 9 ghput ■ Rx Throughput	10.0 (sdg) 7.5 1 2 3 4 5 6 7 0.0 1 2 3 4 5 6 7 • Tx Throughput ® Rx Throughput	8 9

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Figure 3-8: Set Payload Size on Channel 0 and Channel 1



( )

Figure 3-9 shows the performance achieved at this payload size is 9.74 Gb/s per channel per direction. The allowed payload values that can be entered are 46 bytes to 1,500 bytes.



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*Figure 3-9:* Throughput Performance Plots

**TIP:** The relationship between payload size and throughput can be demonstrated by changing the payload size. Reducing the payload size causes a dip in performance. Refer to Appendix B, Performance Estimates for performance estimation on 10G Ethernet protocol.



- 2. Stop traffic generation by clicking **Stop** for both channels.
- 3. Select the **Channel 0 Statistics** tab and verify if any packets were in error or were dropped (Figure 3-10).



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Figure 3-10: Channel 0 MAC Statistics

- 4. Next, select the **Channel 1 Statistics** tab and verify if any packets were in error or were dropped:
  - The TX MAC statistics for Channel 0 should match the RX MAC statistics of Channel 1.
  - The TX MAC statistics for Channel 1 should match the RX MAC statistics of Channel 0.



**IMPORTANT:** When running traffic on both channels, If internal generator mode is selected on one channel, the internal generator mode must be selected on the other channel. If external generator mode is selected on one channel, the external generator mode must be selected on the other channel.



**TIP:** Appendix D, Testing with an External Traffic Generator describes how to setup and test the 10GBASE-R TRD using an external Ixia NGY-NP4-01 10 Gigabit Application Network Processor Load Module.



 Select the **Power Plot** tab to view the FPGA power consumption and die temperature (Figure 3-11).



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Chapter 4

# Implementing and Simulating the Design

This chapter describes how to implement and simulate the 10GBASE-R TRD.

### **Implementing the Design**

The 10GBASE-R TRD is implemented using the Vivado® Design Suite.

#### **Download the Reference Design Files**

See Download Targeted Reference Design Files for instructions.



**TIP:** The Reference Design directory structure is described in Appendix A, Directory Structure.

**IMPORTANT:** The 10-Gigabit Ethernet MAC IP core requires a license to build the design. Obtain the license at the 10 Gigabit Ethernet Media Access Controller (10GEMAC) website [Ref 4]. Click **Evaluate** or **Order** to access the license.

#### Generate the Hardware Bitstream

The reference design can be implemented or simulated on a Windows 7 or a Linux computer. The computer should have Vivado Design Suite 2017.3 installed on it.

- 1. Launch the Vivado Integrated Design Environment (IDE) on the control computer and set up the reference design project.
- On Windows 7:
  - a. Click Start > All Programs > Xilinx Design Tools > Vivado 2017.3 > Vivado 2017.3.



- b. On the getting started page, click **Window > Tcl Console** (Figure 4-1).
- c. In the Tcl console type (Figure 4-1):

cd <working\_dir>/kcu105\_10gbaser\_trd/hardware/vivado

Vivado 2017.1	
Elle Flow Tools Window Help Q- Quick Access	
VIVADO. HLx Editions	E XILINX ALL PROGRAMMABLE.
Quick Start Create Project > Open Project > Open Example Project >	
Tasks Manage IP > Open Hardware Manager > Xillinx Tcl Store >	
Learning Center	? _ D Ľ X
starr_gui cd C:/Haris/TRD/UG921/2017.1/kcul05_l0gbaser_trd/hardware/vivado	Ŷ
annes sevier/louint 10002000 evalual	>
Source seripus/xeuro_iveokork_red.tci	0

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- On Linux:
  - a. On a terminal window, change directory to

<working\_dir>/kcu105\_10gbaser\_trd/hardware/vivado

b. At the command prompt enter:

vivado -source scripts/kcu105\_10GBASER\_trd.tcl



The Vivado IDE displays the 10gbaser\_trd project populated with sources (Figure 4-2).



**IMPORTANT:** When building the design on Windows, if this error occurs: Path Length Exceeds 260-Bytes maximum allowed by Windows, move the kcul05\_l0gbaser\_trd directory directly under C: \.



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Figure 4-2: 10gbaser\_trd Vivado Project



#### 2. Select the **Sources** tab.

In the Hierarchy window, an IP Integrator (IPI) block design (mac\_phy.bd) is referenced that contains the 10-Gigabit Ethernet MAC IP core (10G MAC), 10-Gigabit Ethernet PCS/PMA IP core (10GBASE-R), the Traffic Generator and Monitor, and the MicroBlaze<sup>™</sup> processor subsystem (Figure 4-3).

The design top level file kcu105\_10gbaser\_top.v instantiates the block design.



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Figure 4-3: Vivado Project, Sources View

- 3. In the Flow Navigator, click Generate Bitstream.
- 4. In the No Implementation Results Available window, click **Yes**. The bitstream will be generated and available at:

<working\_dir>/kcu105\_10gbaser\_trd/hardware/vivado/runs/impl\_run/ 10gbaser\_trd.runs/impl\_1/kcu105\_10gbaser\_top.bit



#### Generate ELF file for the MicroBlaze Controller

To generate the MicroBlaze Controller ELF file, the design is exported to the Software Development Kit (SDK). The SDK is an IDE for software developers built on the Eclipse IDE.

1. From the Vivado IDE menu bar, select **File > Export > Export Hardware** (Figure 4-4).



**IMPORTANT:** The IPI Block Design, mac\_phy.bd must be open to successfully export the design to the SDK.

Edit Flow Tools	Window	Layout View Help Q- Quick Access	write_bitstream Complete
			III Default Lavout
New Project		SIGN - mac_phy	
Open Example Project	E.	× Design Signals ? _ □ □	Diagram × Address Editor × ? [
Save Project As			@ @ % % ⊕ Q ∄ ♦ + ~ № № ♂ ℃ ℃ ₽
Write Project Tcl Archive Project Close Project		<pre>sign Sources (1) k kcu105_10gbaser_top (kcu105_10gbaser_top.v) ( debounce_reset : debouncer (debouncer v)</pre>	
Save Block Design Close Block Design		mac_phy_wrapper_i: mac_phy_wrapper (mac_ph & mac_phy_i: mac_phy (mac_phy.bd) (1) nstraints (1)	
Open Checkpoint Open Regent Checkpoint Write Checkpoint	Т.Б	nulation Sources (1)	
New IP Loc <u>ation</u> Open IP Location Open Regent IP Location	Þ		
New File Open File Open Recent <u>Fi</u> le	Ctrl+0	y IP Sources Libraries Compile Order	
Save All Files		hy.bd ← → 🌣	
Add Sources Open Source File	Alt+A Ctrl+N	Block Designs	
Import	F.	283.6 KB	
Export	- DE	Export Hardware	
Launch SDK		Export Block Design 10gbaser_trd.srcs/sou	
Open Log File Open Journal File		Export Simulation	
Print	Ctri+P		
Exit		ole × Messages Log Reports Design R	uns ? - [
	Q	É 🗢 II 回 🖩 🟛	
	open.	_run: Time (s): cpu = 00:00:41 ; elapsed = 00: _bd_design {/wrk/paegl/users/haris/TRD/10GBASE	00:22 . Memory (MB): peak = 7892.242 ; gain = 711.352 ; free physical = 176766 ; free virtual = 248397 -R/2017.1/kcu105_10gbaser_trd/hardware/vivado/runs/impi_run/logbaser_trd.srcs/sources_1/bd/mac_phy/mac_phy.bd)
	· < ==		
	Type a	Tc1 command here	

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Figure 4-4: Export Hardware to the SDK from the Vivado IDE



2. In the Export Hardware Platform for SDK window (Figure 4-5) select **Include bitstream** and click **OK**. The hardware platform will be exported to:

```
<working_dir>/kcu105_10gbaser_trd/hardware/vivado/runs/impl_run/
10gbaser_trd.sdk
```

📤 Export Hardware	
Export hardware platform for softw development tools	are
Include bitstream	
Export to: S <local project="" to=""></local>	
ОК	Cancel
	X19121-041

Figure 4-5: Export Hardware

3. To launch SDK from the Vivado IDE menu bar, select **File > Launch SDK**. In the launch SDK window click **OK**, SDK window will open with the hardware platform populated (Figure 4-6).

A Launch SDK		×
Launch software development tool		
Exported location: S		-
Workspace: 🛜 <local project="" to=""></local>		•
ОК	Canco	el

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Figure 4-6: Launch SDK



4. In the SDK window (Figure 4-7) select File > New > Application Project to build an application.

C/C++ - kcu105_10gbaser_top_hw_pla	tform_0/syste	m.hdf - Xilinx SDK		_ 🗆 🗙
<u>File E</u> dit <u>S</u> ource Refac <u>t</u> or <u>N</u> avigate Se <u>a</u> rcl	h <u>R</u> un <u>P</u> roject	Yiliny Tools Window Help		
New	Shift+Alt+N	🚇 Application Project	i 🐹 🖬 🕼	🖹 🔤C/C++
Open File <u>.</u>		💵 роага заррогс Раскаде		
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		😂 Folder	Hardware 🔶	An outline is not available.
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Con <u>v</u> ert Line Delimiters To	•	et	h_axi_stream_	
🖻 Print		et	h_axi_stream_	
		mac_phy_o	ch0_ten_gig_e	
Switch <u>W</u> orkspace	•	mac_phy_o	ch1_ten_gig_e	
Restart		microblaze sub syste	em microblaz	
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		SV	stem manage 💌	
Properties	Alt+Enter			
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E <u>x</u> it			3:59:32 TNF0	: Processing command
	Description			
🛛 🖻 🗁 Auto Discovered	Description			
			111	
0 items selected				

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Figure 4-7: Creating an Application Project in the SDK



 In the Application Project window (Figure 4-8) enter the project name as kcu105\_10gbaser\_top and click Next.

SDK	New Project	
Application Project	-	G
Create a managed ma	ake application project. 💋 🎽	
	. Margan	
<u>P</u> roject name: kcu10	05_10gbaser_top	
☑ Use <u>d</u> efault locatio	on	
Location: //wrk/paeg1,	/users/haris/TRD/10GBASE-R/2016.4/kcu105_10	
Choose file	system: default 🔅	
OS Platform: stand	lalone	0
Target Hardware		
Hardware Platform:	kcu105_10gbaser_top_hw_platform_0	w)
Processor:	microblaze_sub_system_microblaze_0	٥
Target Software		
Language:	● C ○ C++	
Compiler:	32-bit	
Board Support Packa	age:	
	O Use existing	
?	< <u>Back</u> <u>N</u> ext > Cancel <u>F</u> inish	

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Figure 4-8: Assign Project Name



6. Select **Empty Application** and click Finish (Figure 4-9).

SOK New Pro	ject	
Templates		G
Create one of the available templ application project.	ates to generate a fully-functioning	
Available Templates:		
Dhrystone	A blank C project.	
Empty Application		
Hello World		
lwIP Echo Server		
Memory Tests		
Peripheral Tests		
SREC Bootloader		
SREC SPI Bootloader		
		=
		1.00
	N	
2 - Pack		Finish
		TUIISII

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*Figure 4-9:* **Select Empty Application**


7. In the project explorer tab (Figure 4-10), right-click kcu105\_10gbaser\_top, select **Import**, and under the General tab select **File System**. Click Next.



Figure 4-10: Importing File System



### 8. Browse to source folder:

<working\_dir>/kcu105\_10gbaser\_trd/software/source

Select the source directory in the left pane and click Finish (Figure 4-11).

The application ELF file will be generated and available at:

<working\_dir>/kcu105\_10gbaser\_trd/hardware/vivado/runs/impl\_run/10gb aser\_trd.sdk/kcu105\_10gbaser\_top/Debug/kcu105\_10gbaser\_top.elf



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Figure 4-11: Importing Software/Source Directory



### **Generate Bitstream For Download**

1. Create a bitstream for download. In the Vivado Tcl console (Figure 4-12), run the command:

source scripts/create\_download\_bit.tcl



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### Figure 4-12: Run Script to Create the download.bit Bitstream

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The create\_download\_bit.tcl script runs the update\_mem command and combines kcu105\_10gbaser\_top.bit and kcu105\_10gbaser\_top.elf into single bitfile available at:

<working\_dir>/kcu105\_10gbaser\_trd/hardware/vivado/runs/impl\_run/10g baser\_trd.runs/impl\_1/kcu105\_10gbaser\_download.bit



# Simulating the Design

The 10GBASE-R TRD can be simulated using the Vivado Design Suite simulator. Refer to *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 4], for information describing how to run simulation with different simulators.

The simulation environment sets up the Traffic Generator and Monitor blocks of the TRD to operate in internal generator mode. The Traffic Generator for channel 0 generates 10 packets which are transmitted to the 10-Gigabit Ethernet MAC IP core. The packets are looped back on the PHY and become receive packets on channel 1. Similarly, the Traffic Generator for channel 1 generates 10 packets which are transmitted to the 10-Gigabit Ethernet MAC IP core. The packets are looped back on the PHY and become receive packets on channel 1. Similarly, the Traffic Generator for channel 1 generates 10 packets which are transmitted to the 10-Gigabit Ethernet MAC IP core. The packets are looped back on the PHY and become receive packets on Channel 0. The test bench waits to receive 10 packets on each channel without errors and then ends the simulation with a Simulation Passed message.

Simulating the AXI UART Lite IP and MicroBlaze processor subsystem takes a lot of time. In order to speed up simulation the Traffic Generator and Monitor block is not configured using its AXI4-Lite interface connected to the MicroBlaze processor subsystem. The Traffic Generator and Monitor block provides a port tg\_config to configure the block. This port is used only for simulation. Table 4-1 shows the bitmap for this port.

Table 4-1:	<b>Traffic Generator</b>	Configuration	Port
------------	--------------------------	---------------	------

<b>Bit Position</b>	Description
0	Enable loopback for external generator mode.
1	Enable generator for internal generator mode.
31:16	Ethernet frame data payload size.
	Allowed values (46 bytes to 1,500 bytes).

The test bench for the 10GBASE-R TRD is available at:

<working\_dir>/kcu105\_10gbaser\_trd/hardware/sources/testbench/tb.v.



**IMPORTANT:** Before running a simulation the 10gbaser\_trd project must be open and step 1 under Generate the Hardware Bitstream should have been executed.



To run a simulation in Mentor Graphics Questa ModelSim® Advanced Simulator:

 In the flow navigator panel, under Simulation, click Run Simulation > Run Behavioral Simulation (Figure 4-13).

<u>F</u> ile <u>E</u> dit F <u>l</u> ow <u>T</u> ools	s Window Layout View Help Qr Quick Access
Flow Navigator	ž 🗢 ? 💶 BLOCK DESIGN - mac_phy
<ul> <li>PROJECT MANAGER</li> <li>Settings</li> <li>Add Sources</li> <li>Language Templates</li> <li>IP Catalog</li> </ul>	Sources       ×       Design       Signals       ?       □       Diagram       ×       Address Editor       ×         Q       ₹       ♦       +       ?       •       Φ       Φ       \$\$\$\$\$\$\$\$\$\$       Φ       Q       ₹       ♦       •       Q       \$
✓ IP INTEGRATOR	✓ ▲☑ mac_phy_i: mac_phy (mac_phy.bd)
Create Block Design Open Block Design Generate Block Design SIMULATION Run Simulation	We mac_phy.v) (13) Constraints (1) Simulation Sources (1) Hierarchy IP Sources Libraries Cor
R	Run Behavioral Simulation ? _ C C X
<ul> <li>RTL ANALYSIS</li> <li>Open Elaborati</li> <li>R</li> <li>R</li> <li>R</li> <li>R</li> </ul>	Run Post-Synthesis Functional Simulation <ul> <li></li></ul>
<ul> <li>Run Synthesis</li> <li>Open Synthesized Desig</li> </ul>	gn

*Figure 4-13:* **Run Modelsim Simulation** 

To run a simulation in the Vivado Design Suite simulator:

- 1. In the Flow Navigator Panel, under PROJECT MANAGER, click **Settings**.
- 2. In the Settings window, under **Project Settings**, click **Simulation**.



 Select Vivado Simulator in the Target simulator field and click Yes when asked if it is OK to change your target simulator to Vivado Simulator. Click OK in the Settings window (Figure 4-14).



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Figure 4-14: Set Simulator to Vivado Simulator

4. In the Flow Navigator Panel, under Simulation, click **Simulation > Run behavioral simulation**.



**IMPORTANT:** When simulating the design on Windows, use this command to prevent the path length from exceeding 260 bytes:

exec subst A:<working dir>\rdf0308-kcu105-trd04-2017-3\kcu105\_10gbaser\_trd\hardware



# Chapter 5

# **Reference Design Details**

This chapter describes the hardware design and software components.

# Hardware

Figure 5-1 shows a block-level overview of the 10GBASE-R TRD.



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Figure 5-1: 10GBASE-R TRD Block Diagram

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The details of the hardware architecture are provided in three sections:

- Data Plane Components: Describes the 10-Gigabit Ethernet PCS/PMA IP core (10GBASE-R), 10-Gigabit Ethernet MAC IP core (10G MAC) and the Traffic Generator and Monitor.
- Control Plane Components: Describes the MicroBlaze<sup>™</sup> processor subsystem and the peripherals connected to it.
- Clocking and Reset: Describes how clocks and resets are distributed to the different components in the 10GBASE-R TRD.

### **Data Plane Components**

The 10-Gigabit Ethernet PCS/PMA IP (10GBASE-R) and 10-Gigabit Ethernet MAC IP (10G MAC) cores constitute a 10 Gb/s Ethernet channel. There are two channels in the 10GBASE-R TRD; channel 0 and channel 1. The data source for these channels can be configured to be either an internal or external Traffic Generator.

### 10-Gigabit Ethernet PCS/PMA IP Core

The 10-Gigabit Ethernet PCS/PMA IP core provides an XGMII interface to connect to a 10-Gigabit Ethernet MAC IP core and implements a 10.3125 Gb/s serial single-channel PHY providing a direct connection to an SFP+ optical transceiver module (see [Ref 5]) using the SFI electrical specification. The SFP+ optical transceiver module plugs into an SFP cage on the KCU105 evaluation board. The external Traffic Generator communicates with this IP via the SFP+ interface.

More information is available at the 10 Gigabit Ethernet PCS/PMA (10GBASE-R) website [Ref 6] and in the 10G Ethernet PCS/PMA LogiCORE IP Product Guide (PG068) [Ref 7].

### 10-Gigabit Ethernet MAC IP Core

The 10-Gigabit Ethernet MAC IP core is a single-speed, full-duplex, 10-Gb/s Ethernet Media Access Controller. This 10G MAC connects to the PHY layer through the XGMII interface. The internal Traffic Generator drives data on the AXI4-Stream ports of this IP.

A license can be obtained a the 10 Gigabit Ethernet Media Access Controller (10GEMAC) website [Ref 8]. More information is available in the *10G Ethernet MAC LogiCORE IP Product Guide* (PG072) [Ref 9].

### Traffic Generator and Monitor

The data source for either of the two 10 Gb/s Ethernet channels can be configured to be from an internal or external Traffic Generator. The internal Traffic Generator consists of custom logic implemented in the FPGA that drives the 10-Gigabit Ethernet MAC. The external traffic generator is an off-the-shelf Ethernet traffic generator/checker like the



Ixia load module that can drive the 10-Gigabit Ethernet PCS/PMA IP core as described in Appendix D, Testing with an External Traffic Generator.

Figure 5-2 shows the block diagram of the Traffic Generator and Monitor.



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Figure 5-2: Traffic Generator Block Diagram

The Generator block generates Ethernet traffic when you select internal Traffic Generator mode.

The Loopback module loops back the data received from an external Ethernet traffic generator when you select external Traffic Generator mode.

The Performance Monitor block monitors the AXI4-Stream ports of the 10-Gigabit Ethernet MAC IP core and reports throughput.

The User Control and Status Registers block passes information to and from the Ethernet Controller application using the MicroBlaze processor subsystem.

### Internal Traffic Generator, Generator Module

The Generator module generates Ethernet packets based on user inputs provided from the Ethernet Controller application running on the control computer. Data payload size can be from 46 bytes to 1,500 bytes. Table 5-1 shows the packet format generated by the Generator module.



Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Source	Address	Destination Address					
Sequence	e Number	Length Source Address					
		Sequence Number Sequence Number			e Number		
Sequence	e Number						

The source and destination MAC addresses are parameters into this block. The length field is the data payload value. The actual length of a packet generated by this block is:

 14 bytes of header (Destination Address + Source Address + Length/Type Field) + Data payload

The sequence number field indicates packet count and increments by one every packet.

The generated packets are transmitted on AXI4-Stream interface to the 10-Gigabit Ethernet MAC IP core. Table 5-2 shows the parameters and ports on the generator module.

Port/Parameter Name	Туре	Description	
		Source MAC Address	
XIL_MAC_ID_THIS	Parameter	For channel 0 = 48 'h11110000000 For channel 1 = 48 'h22220000000	
		Destination MAC Address	
XIL_MAC_ID_OTHER	Parameter	For channel 0 = 48 'h22220000000 For channel 1 = 48 'h11110000000	
Clock and reset ports			
reset	Input	Synchronous reset.	
tx_axis_clk	Input	156.25 MHz clock transmit ports on the AXI4-Stream interface.	
Transmit Ports on the AXI4-Stream Interface			
tx_axis_tdata[63:0]	Output	Data to be transmitted to the 10-Gigabit Ethernet MAC IP core.	
		The transmit keep signal is used to determine which data bytes are valid on tx_axis_tdata during a given beat (this signal is valid only if tx_axis_tvalid and tx_axis_tready are both asserted).	
tx_axis_tkeep[7:0]		Bit 0 corresponds to the least significant byte on tx_axis_tdata and bit 7 corresponds to the most significant byte.	
		When tx_axis_tlast is not asserted, the only valid value is $0xFF$ . When tx_axis_tlast is asserted, valid values are $0x01$ to $0xFF$ .	
tx_axis_tlast	Output	End of frame indicator on transmit packets. Valid only along with assertion of tx_axis_tvalid.	
tx_axis_tvalid	Output	Source ready to provide transmit data. Indicates that the generator is presenting valid data on tx_axis_tdata.	
tx_axis_tuser	Output	If asserted indicates an underrun frame. This is tied to 1'b0.	

Table 5-2: Generator Module Parameters and Ports



Table 5-2:	Generator Module Parameters and Ports	Gont'd)
------------	---------------------------------------	---------

Port/Parameter Name	Туре	Description
ty avis tready	Input	Destination ready for transmit. Indicates that the 10-Gigabit Ethernet MAC IP core is ready to accept data on tx_axis_tdata.
tx_axis_tready	input	The simultaneous assertion of tx_axis_tvalid and tx_axis_tready marks the successful transfer of one data beat on tx_axis_tdata.
Control Ports		
enable_gen	Input	Enable internal generator.
data_payload	Input	Size of the payload (46 bytes to 1,500 Bytes).

The data flow with internal generator mode enabled on the Traffic Generator for channel 0 is:

Generator module CH0  $\rightarrow$  CH0 TX AXI4-Stream interface of the 10-Gigabit Ethernet MAC IP  $\rightarrow$  CH0 TX XGMII interface of the 10GBASE-R  $\rightarrow$  CH0 TXN/TXP serial lines  $\rightarrow$ loopback to CH1 RXN/RXP serial lines  $\rightarrow$  CH1 RX XGMII interface of the 10GBASE-R  $\rightarrow$ CH1 RX AXI4-Stream interface of the 10-Gigabit Ethernet MAC IP core

The data flow with internal generator mode enabled on the Traffic Generator for channel 1 is:

Generator module CH1  $\rightarrow$  CH1 TX AXI4-Stream interface of the 10-Gigabit Ethernet MAC IP core  $\rightarrow$  CH1 TX XGMII interface of the 10GBASE-R  $\rightarrow$  CH1 TXN/TXP serial lines  $\rightarrow$  loopback to CH0 RXN/RXP serial lines  $\rightarrow$  CH0 RX XGMII interface of the 10GBASE-R  $\rightarrow$  CH0 RX AXI4-Stream interface of the 10-Gigabit Ethernet MAC IP core

### External Traffic generator, Loopback Module

The Traffic Generator is put into loopback mode when you select **External Generator** in the Ethernet Controller application control panel.

In this mode data is generated by an external generator like the Ixia load module. The data received on the AXI4-Stream RX port of the 10-Gigabit Ethernet MAC IP core is looped back to the other channel's AXI4-Stream TX port. The loopback module changes the source address and destination address on the received data before passing it to the 10-Gigabit Ethernet MAC IP core. The source and destination MAC addresses are parameters into the loopback module. Table 5-3 shows the parameters and ports on the loopback module.

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Port/Parameter Name	Туре	Description
		Source MAC Address
XIL_MAC_ID_THIS	Parameter	For Channel 0 = 48 'h111100000000 For Channel 1 = 48 'h222200000000
		Destination MAC Address (External Generator)
EXT_MAC_ID	Parameter	For Channel 0 = 48 ' h33330000000 For Channel 1 = 48 ' h444400000000
Clock and reset ports		
reset	Input	Synchronous reset.
tx_axis_clk	Input	156.25 MHz clock Transmit Ports on the AXI4-Stream interface.
Transmit Ports on the AX	(I4-Stream I	nterface
tx_axis_tdata[63:0]	Output	Data to be transmitted to 10-Gigabit Ethernet MAC IP core.
		The transmit keep signal is used to determine which data bytes are valid on tx_axis_tdata during a given beat (this signal is valid only if tx_axis_tvalid and tx_axis_tready are both asserted).
tx_axis_tkeep[7:0]		Bit 0 corresponds to the least significant byte on tx_axis_tdata and bit 7 corresponds to the most significant byte.
		When tx_axis_tlast is not asserted, the only valid value is $0 \times FF$ . When tx_axis_tlast is asserted, valid values are $0 \times 01$ to $0 \times FF$ .
tx_axis_tlast	Output	End of frame indicator on transmit packets. Valid only along with asser-tion of tx_axis_tvalid.
tx_axis_tvalid	Output	Source ready to provide transmit data. Indicates that the generator is presenting valid data on tx_axis_tdata.
tx_axis_tuser	Output	If asserted indicates an underrun frame. This is tied to 1'b0
tx_axis_tready	Input	Destination ready for transmit. Indicates that the 10-Gigabit Ethernet MAC IP core is ready to accept data on tx_axis_tdata. The simultaneous assertion of tx_axis_tvalid and tx_axis_tready marks the successful transfer of one data beat on tx_axis_tdata.
Receive Ports on the AXI	4-Stream In	terface
rx_axis_tdata[63:0]	Input	Data received from the 10-Gigabit Ethernet MAC IP core.
rx_axis_tkeep[7:0]		The receive keep signal is used to determine which data bytes are valid on rx_axis_tdata during a given beat (this signal is valid only if rx_axis_tvalid and rx_axis_tready are both asserted).
rx_axis_tlast	Input	End of frame indicator on received packets. Valid only along with assertion of rx_axis_tvalid.
rx_axis_tvalid	Input	Source ready to provide data. Indicates that the MAC is presenting valid data on rx_axis_tdata.
		rx_axis_tuser input if asserted indicates a good packet is received.

#### Table 5-3: Loopback Module Generator Parameters and Ports



Port/Parameter Name	Туре	Description
rx_axis_tready	Output	Destination ready for receive. Indicates that the loopback module is ready to accept data on rx_axis_tdata.
		The simultaneous assertion of rx_axis_tvalid and rx_axis_tready marks the successful transfer of one data beat on rx_axis_tdata.
		The 10-Gigabit Ethernet MAC IP core doesn't look at this signal and sends received data whenever available.
Control Ports	L	
enable_loopback	Input	Enable external generator.

Tabla E 2.	Loophack Modulo Congrator Parameters and Ports	(Cont'd)	۱
<i>iubie</i> 5-5.	LOOPDack Module Generator Parameters and Ports	(com u)	,

The 10-Gigabit Ethernet MAC IP core AXI4-Stream RX interface doesn't allow back-pressure i.e., after a packet reception has started it completes the entire packet (rx\_axis\_tready is disregarded). If transmit throttles, the receive side cannot stop. AXI4-Stream Data FIFO IP is added in the loopback path to counter this. The FIFO size (8 bytes wide x 256 depth) should accommodate maximum payload size (1,500 bytes). Packet mode is also selected on the FIFO which ensures that a full packet is present in the FIFO before transmission to the 10-Gigabit Ethernet MAC IP core.

The Data flow with loopback mode enabled on the Traffic Generator for Channel 0 is:

IXIA TX CH1  $\rightarrow$  CH1 RXN/RXP serial lines  $\rightarrow$  CH1 RX XGMII interface of the 10GBASE-R  $\rightarrow$  CH1 RX AXI4-Stream interface of the 10G MAC  $\rightarrow$  Loopback Module CH0  $\rightarrow$  CH0 TX AXI4-Stream interface of the 10G MAC  $\rightarrow$  CH0 TX XGMII interface of the 10GBASE-R  $\rightarrow$  CH0 TXN/TXP serial lines  $\rightarrow$  IXIA RX CH0

The Data flow with loopback mode enabled on the Traffic Generator for Channel 1 is:

IXIA TX CH0  $\rightarrow$  CH0 RXN/RXP serial lines  $\rightarrow$  CH0 RX XGMII interface of the 10GBASE-R  $\rightarrow$  CH0 RX AXI4-Stream interface of the 10G MAC  $\rightarrow$  Loopback Module CH1  $\rightarrow$  CH1 TX AXI4-Stream interface of the 10G MAC  $\rightarrow$  CH1 TX XGMII interface of the 10GBASE-R  $\rightarrow$  CH1 TXN/TXP serial lines  $\rightarrow$  IXIA RX CH1

### **Ethernet Performance Monitor**

The Ethernet performance monitor block snoops for valid transactions on the AXI4-Stream interface ports of the 10-Gigabit Ethernet MAC IP core and keeps track of bandwidth utilization. A timer within this block counts the clocks until one second has elapsed, during which time counters have collected data about link performance.

Four counters collect information on the transactions on the AXI4-Stream interface:

• TX Payload Byte Count. This counter counts bytes transferred when tx\_tvalid and tx\_tready signals are asserted between the Traffic Generator block and the 10G MAC. At the end of the packet (tx\_tlast) 14 bytes of header are subtracted from the count to get payload count.



- TX Packet Count. This counter counts the number of transmitted packets. The counter increments when tx\_tvalid and tx\_tready and tx\_tlast signal are asserted.
- RX Payload Byte Count. This counter counts bytes transferred when rx\_tvalid and rx\_tready signals are asserted between the Traffic Generator block and the 10G MAC. At the end of the packet (rx\_tlast) 14 bytes of header are subtracted from the count to get payload count.
- RX Packet Count. This counter counts the number of received packets. The counter increments when rx\_tvalid and rx\_tready and rx\_tlast signal are asserted.

The counts are truncated to a four-byte resolution, and the last two bits of the register indicate the sampling period. The last two bits transition every second from 00 to 01 to 10 to 11. The software polls the performance registers every second. If the sampling bits are the same as the previous read, then the software needs to discard the second read and try again. When the one-second timer expires, the new byte counts are loaded into the registers, overwriting the previous values. Table 5-4 shows the parameters and ports on this module.

Port/Parameter Name	Туре	Description
ONE_SEC_CLOCK_COUNT	Parameter	Defines the number of 156.25 MHz clock cycles equivalent to 1 sec. Default value is 32 'h9502F90.
Clock and reset ports		
reset	Input	Synchronous reset.
clk	Input	156.25 MHz clock.
Transmit ports on the A	(I4-Stream i	nterface
tx_axis_tdata[63:0]	Input	Data to be transmitted to the 10-Gigabit Ethernet MAC IP core.
tx_axis_tkeep[7:0]		The transmit keep signal is used to determine which data bytes are valid on tx_axis_tdata during a given beat (this signal is valid only if tx_axis_tvalid and tx_axis_tready are both asserted).
		Bit 0 corresponds to the least significant byte on tx_axis_tdata and bit 7 corresponds to the most significant byte. When tx_axis_tlast is not asserted, the only valid value is $0xFF$ .
		When tx_axis_tlast is asserted, valid values are $0 \times 01$ to $0 \times FF$ .
tx_axis_tlast	Input	End of frame indicator on transmit packets. Valid only along with assertion of tx_axis_tvalid.
tx_axis_tvalid	Input	Source ready to provide transmit data. Indicates that the generator is presenting valid data on tx_axis_tdata.
tx_axis_tuser	Input	If asserted indicates an underrun frame. This is tied to 1 'b0.
tx_axis_tready	T.	Destination ready for transmit. Indicates that the 10-Gigabit Ethernet MAC IP core is ready to accept data on tx_axis_tdata.
	Πρατ	The simultaneous assertion of tx_axis_tvalid and tx_axis_tready marks the successful transfer of one data beat on tx_axis_tdata.

Table 5-4: Et	thernet Performance	<b>Monitor Para</b>	ameters and Ports
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Port/Parameter Name	Туре	Description				
Receive Ports on the AXI4-Stream Interface						
rx_axis_tdata[63:0]	Input	Data received by the 10-Gigabit Ethernet MAC IP core.				
rx_axis_tkeep[7:0]		The receive keep signal is used to determine which data bytes are valid on rx_axis_tdata during a given beat (this signal is valid only if tx_axis_tvalid and tx_axis_tready are both asserted).				
rx_axis_tlast	Input	End of frame indicator on received packets. Valid only along with asser-tion of rx_axis_tvalid.				
rx_axis_tvalid	Input	Source ready to provide data. Indicates that the MAC is presenting valid data on rx_axis_tdata.				
rx_axis_tuser	Input	If asserted indicates a good packet is received.				
		Destination ready for receive. Indicates that the loopback is ready to accept data on rx_axis_tdata.				
rx_axis_tready	Output	The simultaneous assertion of rx_axis_tvalid and rx_axis_tready marks the successful transfer of one data beat on rx_axis_tdata.				
		The 10-Gigabit Ethernet MAC IP core doesn't look at this signal and sends received data whenever available.				
Performance Statistics P	orts					
tx_byte_count	Output	Number of bytes transmitted in one second.				
tx_pkt_count	Output	Number of packets transmitted in one second.				
rx_byte_count	Output	Number of bytes received in one second.				
rx_pkt_count	Output	Number of packets received in one second.				

#### Table 5-4: Ethernet Performance Monitor Parameters and Ports (Cont'd)

### **User Control and Status Registers**

The user selections made in the Ethernet controller application are passed to the Traffic Generator and Monitor using this block. An AXI4-Lite interface is required for the MicroBlaze processor subsystem to execute reads (status) and writes (control) to this block. The AXI4-Lite to the AXI4-Lite IP Interface IP core (IPIF) is instantiated in the design to read and write to a register map file. See *AXI4-Lite IPIF LogiCORE IP Product Guide* (PG155) [Ref 10].

Providing an AXI4-Lite slave interface provides the flexibility of using this module in other designs. To reuse this block, the control and status signals into the register map must be changed. Appendix C, User-Space Registers describes the registers implemented in the Traffic Generator and Monitor block. Figure 5-3 shows the user register interface.

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Figure 5-3: User Register Interface

### SYSMON for Power and Temperature Monitoring

All UltraScale<sup>™</sup> devices contain a System Monitor (SYSMON). SYSMON is used for monitoring die temperature and voltage and current on different power supply rails which are used to calculate system power.

For more information about SYSMON, see *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 11].

The application driver running on the MicroBlaze processor subsystem sets up SYSMON to read the temperature, voltage, and current data periodically. The System Management wizard for SYSMON is configured with AXI4-Lite interface. This interface is used for communication with the MicroBlaze controller.

For more information on the System Management wizard, see *System Management Wizard LogiCORE IP Product Guide* (PG185) [Ref 12].

Figure 5-4 shows the power and temperature monitoring through SYSMON.



Figure 5-4: Power and Temperature Monitor

### **Control Plane Components**

The Ethernet Controller application running on the control computer sends control information and receives status to and from different components of the 10GBASE-R TRD using the MicroBlaze processor subsystem.



### MicroBlaze Processor Subsystem and AXI Interconnect

The IP cores required to support the MicroBlaze processor and create a subsystem are:

- MicroBlaze local memory
- Processor system reset
- MicroBlaze debug module
- AXI Interrupt controller

In Vivado IPI, adding the MicroBlaze IP core and running the connection automation creates the MicroBlaze processor system shown in Figure 5-5.



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Figure 5-5: IPI-Generated MicroBlaze Processor System

The AXI interconnect IP allows the MicroBlaze processor subsystem to communicate with the AXI Interrupt controller IP using the AXI4 memory mapped interface.

The 10GBASE-R TRD AXI interconnect IP is reconfigured to have seven master ports instead of one. The seven master ports connect to seven AXI slaves:

- AXI interrupt controller
- AXI UART Lite which communicates with the Ethernet Controller application running on the control computer
- System Management wizard for SYSMON
- Channel 0, the 10-Gigabit Ethernet MAC IP core



- The Traffic Generator and Monitor connected to channel 0
- Channel 1, the 10-Gigabit Ethernet MAC IP core
- The Traffic Generator and Monitor connected to channel 1

The AXI interconnect enables communication between the MicroBlaze processor subsystem (Master) and seven Peripherals (Slaves).

The address range assigned to each peripheral is shown in Figure 5-6. The application driver running on the MicroBlaze processor subsystem will use these addresses to map read/write transactions from the Ethernet Controller application to the AXI UART Lite to the MicroBlaze processor subsystem to other peripherals and back.

:	Diagram × Address Editor ×							? 🗗
	Q ★ +							
	Cell	Slave Interface	Base Name	Offset Address	Range		High Address	
	w   microblaze_sub_system/microblaze_0							
	✓ III Data (32 address bits : 4G)							
J	🚥 axi_uartiite_0	S_AXI	Reg	0x4060_0000	64K	v	0x4060_FFFF	
	microblaze_sub_system/microblaze_0_local_memory/dlmb_bram_if_cntir	SLMB	Mem	0x0000_0000	128K	*	0x0001_FFFF	
	🚥 eth_axi_stream_gen_mon_0	s_axi	reg0	0x4AA0_0000	64K	*	0x4AA0_FFFF	
	🚥 eth_axi_stream_gen_mon_1	s_axi	reg0	0x4AA1_0000	64K	*	0x4AA1_FFFF	
	microblaze_sub_system/mdm_1	S_AXI	Reg	0x7E20_0000	64K	*	0x7E20_FFFF	
	microblaze_sub_system/microblaze_0_axi_intc	s_axi	Reg	0x4120_0000	64K	*	0x4120_FFFF	
	🚥 system_management_wiz_0	S_AXI_LITE	Reg	0x44A2_0000	64K	*	0x44A2_FFFF	
	🚥 mac_phy_ch0/ten_gig_eth_mac_ch0	s_axi	Reg	0x74C0_0000	64K	Ŧ	0x74C0_FFFF	
	🚥 mac_phy_ch1/ten_gig_eth_mac_ch1	s_axi	Reg	0x74C1_0000	64K	Ŧ	0x74C1_FFFF	
	<ul> <li>Instruction (32 address bits : 4G)</li> </ul>							
	microblaze_sub_system/microblaze_0_local_memory/ilmb_bram_if_cntlr	SLMB	Mem	0x0000_0000	128K	v	0x0001_FFFF	

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*Figure 5-6:* **Peripheral Address Map** 

For more details on the MicroBlaze processor core, see the MicroBlaze Soft Processor Core website [Ref 13].

For more details on the AXI Interconnect, see the AXI Interconnect website [Ref 14].

### AXI UART Lite

The AXI UART Lite IP core provides the controller interface for asynchronous serial data transfer. The Ethernet Controller application running on the control computer communicates with this serial interface.

The AXI UART Lite IP core also connects to the MicroBlaze processor subsystem through the AXI interface and passes information to and from the Ethernet Controller application to the different components of the design.

For more details on AXI UART Lite, see *AXI UART Lite LogiCORE IP Product Guide* (PG142) [Ref 15] and the AXI UART Lite website [Ref 16].

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## **Clocking and Reset**

The 10-Gigabit Ethernet PCS/PMA core requires a 156.25 MHz differential reference clock for transceivers. The shared logic (clocking and reset logic) within the channel 0 10-Gigabit Ethernet PCS/PMA IP core produces a single ended 156.25 MHz clock. This clock is used for all of the blocks in the design including the MicroBlaze processor subsystem and SYSMON. Figure 5-7 shows the clock distribution.



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An external reset (a debounced pushbutton switch) drives the 10-Gigabit Ethernet PCS/PMA IP cores, the 10-Gigabit Ethernet MAC IP cores and the Processor Subsystem Reset IP core in the MicroBlaze processor System after being debounced.



The Processor System Reset Module provides resets for the MicroBlaze processor subsystem components and resets to the AXI Interconnect and peripherals (AXI4-Lite interfaces on AXI UART Lite, SYSMON, Traffic Generator and Monitor, and 10-Gigabit Ethernet MAC IP). Figure 5-8 shows the reset connections.



Figure 5-8: Resets

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For details on the Processor System Reset Module, see the Processor System Reset Module website [Ref 17].



# Software

There are two major software components to monitor and control the Ethernet Reference Design System:

- GUI/Client Application
- MicroBlaze Processor Server Application

Figure 5-9 shows these components.



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## **GUI/Client Application**

A Java-based GUI/Client application running on the control computer communicates with the MicroBlaze Processor Server application through a UART interface to control test parameters, collect statistics and display current status of the design.

The GUI displays the following information:

- Current mode of operation
- Payload size
- Throughput numbers and graphs when a test is executing
- 10-Gigabit Ethernet MAC IP statistics
- Power consumption and temperature for the FPGA
- Block diagram of the design



### Figure 5-10 shows the GUI.



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Figure 5-10: GUI (Ethernet Controller Application)

The GUI provides control of:

- Test mode: Select use of the internal traffic generator or an external generator to generate Ethernet traffic.
- Payload size: Specify the size of packets when running in internal generator mode.

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The GUI interacts with the KCU105 board through the UART COM port exposed by the Silicon Labs UART driver. All transmitted and received data adheres to a custom command model followed by the client and server.



### **Command Format**

The command format used by the GUI for reading and writing 32-bit values to the registers in the design is described in this section.

### **Read Command**

R <type of request> <output type> <Command number, denoted as a 4-character hexadecimal numeric string, AAAA>

- R denotes a Read command
- type of request indicates the type of request and it can either be:
  - s which specifies a single register read request, or
  - b which specifies a bulk read request

Use a single register read for debugging purposes or for reading registers which are not monitored by the GUI.

Use a bulk read command to make the GUI constantly poll all test parameters and statistics. This eliminates the need to send multiple commands for each individual value. A bulk read command reads the registers in a predefined order.

- output type indicates output type and it can be:
  - h specifies the value sent out by the server will be the actual data width i.e., 4 bytes
  - a specifies the value sent out by the server will be an 8-byte hexadecimal string
- AAAA denotes four character hexadecimal numeric string representation of the command number which will eventually be mapped to the actual register offset in the server application. Using different command numbers instead of the actual register values allows the GUI to remain constant in spite of changes in the hardware design or the application.

Example Read command:

R s a 0001: Read a single register corresponding to command number 0001 and the reported value from the server should be in 8-byte hexadecimal format.

Read command response:

- 1. The command number is read by the server and the appropriate register is identified, its value is read, and is stored in a 4-byte data value.
- 2. Based on the output type specified in the read command, the data is either directly transmitted to the client by the server, or it is converted to an 8-character string denoting an 8-character hexadecimal number and then sent out to the client on the control computer side.





Currently the application only supports output type of 8-character hexadecimal string.

An example Read command output response : F000000F.

### Write Command

W <Command Number denoted as a 4-character hexadecimal numeric string AAAA> < Data, represented as an 8-character hexadecimal numeric string DDDDDDDD>

- w denotes a Write command
- AAAA denotes a 4-character hexadecimal string representation of the command number which will eventually be mapped to the actual register offset in the server application.
- DDDDDDD denotes an 8-character hexadecimal string.

Example Write command:

• W 0001 007D0002: Write a value of 007D0002 to the register corresponding to command value 0001.

Write command is always targeted towards a single register.

The mapping of comm

and numbers to the corresponding register values is the same for both Read and Write commands, i.e., if a write command with a certain command number is used to update a register value, the same command number can be used with a read command to retrieve the value.



## MicroBlaze Processor Server Application

The MicroBlaze Processor Server application running on the FPGA takes care of interpreting the read and write commands sent from the client application and acts accordingly. The software layers are as shown in Figure 5-11.



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### Figure 5-11: Software Layers in the MicroBlaze Processor Server Application

When the hardware platform is exported to the Software Development Kit (SDK) as described in step 2:

- The drivers for standard peripherals (like UART, Interrupt controller, etc.) that are connected to the MicroBlaze processor are already available in the SDK.
- The base address of each peripheral assigned in the hardware platform as shown in Figure 5-6 and is also accessible by the SDK.

The register offsets required by the server application to access relevant registers (TRD configuration registers, performance registers, MAC statistics, and so on) in the IP core product guides being used in this design (e.g., *10G Ethernet MAC LogiCORE IP Product Guide* (PG072) [Ref 9]) and the user-space registers as described in Appendix C, User-Space Registers.

The UART driver is responsible for transferring and receiving data from the UART interface. The server application uses the Application Programming Interface (API) provided by the UART driver and communicates with the client application running on the control computer.



The main task of the server is to read/write values from/to the registers specified in the READ/WRITE commands issued by the GUI.

The various steps undertaken by the server in servicing requests from the client are:

- 1. Register offsets to access registers are put in an integer array during the initialization of MicroBlaze processor server application. The value placed in the integer array is:
  - Base address for the component + register offset
- 2. The order in which these register offset values are placed is made aware to the client application on the host side.
- 3. Each register is identified using a unique command number. This command number is same for both read and write commands.
- 4. When a client initiates a Read/Write command, the data is obtained by the server application through the UART driver.
- 5. The Command Interpreter part of the server application then interprets the data obtained from UART.
- 6. The Command Interpreter identifies the register offset value in the integer array, with respect to the command number associated with the request.
- 7. The Command Interpreter functionality is different for Single Read and Bulk Read commands.
- 8. For a single read request, command number shall give the index of the integer array where the referenced register offset is placed.

Example Single Read Command:

R s a 0001

Here the command number is translated to 1 and the offset value of the register being requested is placed in the zero index of the array.

9. For a bulk read request the command number represents a set of registers with a clearly defined start and end index positions in the array.

Example Bulk Read Command:

R b a 0001

Here the command number 1 represents a set of register offsets in the array, 2 to 17. The values placed at these array indices are the Ethernet performance registers for Channel 0 and Channel 1.

10. The Executor part of the server application then initiates either AXI Read/Write request to the register offset values identified.



11. The Executer then sends an appropriate response to the client on control computer through the UART driver.

**Note:** The bulk Read commands from GUI are serviced by the Server application by going through all the registers associated with the command in a predefined order and transferring the data with a ' ' (white space) as delimiter between each register's value. This mode greatly reduces the number of commands the GUI has to send to obtain the same amount of information.

The source code for the MicroBlaze application is available under the software/source directory (see Appendix A, Directory Structure). The command mapping is defined in CommandDesc.h in the source directory.



# Appendix A

# **Directory Structure**

The directory structures for the 10GBASE-R Ethernet TRD is shown in Figure A-1.



Figure A-1: Targeted Reference Design Directory Structure

## **Directory Content Summary**

The files and folders contained in the 10GBASE-R Ethernet TRD are described in Table A-1. The top-level folder is kcu105\_10gbaser\_trd.



### Table A-1:Directory Content

Folder	Description
software	Contains the software design deliverables.
source	Contains the source code files used for creating the ELF file application that runs on the MicroBlaze <sup>™</sup> processor and communicates with the Ethernet Controller application.
GUI	Contains the EXE file used to install the Ethernet Controller application.
hardware	Contains all the required sources needed to generate a bitstream.
sources	Contains subfolders that contain HDL files, custom IP that is packaged, constraint files, and test bench files.
hdl	Contains HDL files.
ip_packaged	Contains custom IP that is packaged.
constraints	Contains constraint files.
testbench	Contains test bench files.
vivado	Contains files to create a Vivado® Design Suite project and outputs of vivado runs.
scripts	Contains Tcl scripts to create a Vivado project.
runs	Created when the Tcl script file is sourced. The runs folder contains the output of simulation, synthesis, and implementation processes.
ready_to_test	Contains the BIT file to program the KCU105 evaluation board.
readme	A TXT file that describes the 10GBASE-R Ethernet TRD and includes revision history information.

# Appendix B



# **Performance Estimates**

The 10-Gigabit Ethernet MAC IP core operates at a clock rate of 156.25 MHz using a 64-bit data-path width ( $64 \times 156.25 \times 10^6 = 10 \text{ Gb/s}$ ).

For the XGMII, the minimum required interframe gap is 12 bytes. Header overhead consists of a preamble (7 bytes) + Start of frame delimiter (1 byte) + MAC destination address (6 bytes) + MAC source address (6 bytes) + Length/Type field (2 bytes) + FCS (4 bytes). This gives a total overhead of 38 bytes per Ethernet packet.

Table B-1 shows the effective throughput and percentage of maximum bandwidth used for four different payload sizes.

Ethernet Payload Size (Bytes)	Percentage of Bandwidth = Payload size/Packet size * 100	Effective Throughput (Gb/s)
64	64/(38 + 64) = 62.7%	6.27
512	512/(38 + 512) = 93.1%	9.31
1024	1024/(38 + 1024) = 96.3%	9.63
1500	1500/(38 + 1500) = 97.5%	9.75

Table B-1:	Effective Throughput as a Function of Paylo	bad
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# Appendix C



# **User-Space Registers**

User-space registers are user-defined registers implemented in the Traffic Generator and Monitor block shown in Figure 5-1. These registers can be accessed by the MicroBlaze<sup>™</sup> processor subsystem via the AXI4-Lite interface.

Table C-1 through Table C-14 describe the custom registers implemented in the 10GBASE-R TRD. All registers are 32 bits wide. Register bit positions are to be read from bit 31 to bit 0 from left to right. All bits that are undefined in this section are reserved and will return zero when read. Address holes will also return a value of zero when read.

Each peripheral connected to the MicroBlaze processor subsystem is assigned an offset address which is the base address for that peripheral. Figure 5-6 shows the addresses assigned to the Traffic Generator and Monitor blocks

(eth\_axi\_stream\_gen\_mon\_0 and eth\_axi\_stream\_gen\_mon\_1). The Traffic Generator and Monitor base addresses are:

- Traffic Generator and Monitor channel 0 is 0x4AA0\_0000
- Traffic Generator and Monitor channel 1 is 0x4AA1\_0000

# **Control and Status Registers**

### Traffic Generator—Monitor Channel 0

<b>Bit Position</b>	Mode	Default Value	Description
3:0		4′h1	Ethernet reference design1.
15:4	Read Only	12'h141	Software version: Indicates the Vivado® Design Suite version used when developing this reference design. For example, Vivado Design Suite 2014.1 is indicated by 141.
31:16		16'h0105	Target Board: KCU105 board.

#### Table C-1: Design Version Register (0x4AA0\_0000)



Bit Position	Mode	Default Value	Description
1:0		0 0	Sample count. Increments once every second.
31:2	Read Only	0	Transmit payload byte count. This field contains the interface utilization count for active beats (tx_axis_tready = 1 and tx_axis_tvalid = 1) on channel 0 10G Ethernet MAC AXI4-Stream interface for transmit.

#### Table C-2: Ethernet Performance Monitor, Transmit Payload Byte Count Register (0x4AA0\_0004)

Table C-3:	Ethernet Performance Monitor.	<b>Transmit Packet Count</b>	Register (0x	4AA0 0008)

Bit Position	Mode	Default Value	Description
1:0		0 0	Sample count. Increments once every second.
31:2	Read Only	0	Transmit packet count. This field contains the count for the event when there is an active beat on channel 0 10G Ethernet MAC AXI4-Stream interface and end of packet (tx_axis_tlast) is asserted for transmit.

#### Table C-4: Ethernet Performance Monitor, Received Payload Byte Count Register (0x4AA0\_000C)

<b>Bit Position</b>	Mode	Default Value	Description
1:0		0 0	Sample count. Increments once every second.
31:2	Read Only	0	Receive payload byte count. This field contains the interface utilization count for active beats ( $rx_axis_tready = 1$ and $rx_axis_tvalid = 1$ ) on channel 1 10G Ethernet MAC AXI4-Stream interface for receive.

#### Table C-5: Ethernet Performance Monitor, Received Packet Count Register (0x4AA0\_0010)

<b>Bit Position</b>	Mode	Default Value	Description
1:0		0 0	Sample count. Increments once every second.
31:2	Read Only	0	Receive packet count. This field contains the count for the event when there is an active beat on channel 1 10G Ethernet MAC AXI4-Stream interface and end of packet (rx_axis_tlast) is asserted for receive.

#### Table C-6: Traffic Generator Configuration Register (0x4AA0\_0014)

Bit Position	Mode	Default Value	Description
0	Read or Write	0	Enable loopback if external generator is selected.
1		0	Enable generator if internal generator is selected.
31:16		d'125	Ethernet frame data payload size. Allowed values (46 bytes to 1,500 Bytes).



Bit Position	Mode	Default Value	Description
0		0	PHY is up.
31	Read Only	0	Packets dropped in loopback mode when external traffic generator is selected.

### Table C-7: Loopback module and PHY status Register (0x4AA0\_00x18)

### Traffic Generator—Monitor Channel 1

#### Table C-8: Design Version Register (0x4AA1\_0000)

<b>Bit Position</b>	Mode	Default Value	Description
4:0	Read Only	4′h1	Ethernet reference design1.
14:5		12'h141	Design was developed in which Vivado version 141 = Vivado Design Suite 14.1
31:16		16'h0105	Target Board. KCU105 board.

#### Table C-9: Ethernet Performance Monitor, Transmit Payload Byte Count Register (0x4AA1\_0004)

Bit Position	Mode	Default Value	Description
1:0		00	Sample count. Increments once every second.
31:2	Read Only	0	Transmit payload byte count. This field contains the interface utilization count for active beats (tx_axis_tready = 1 and tx_axis_tvalid = 1) on channel 1 10G Ethernet MAC AXI4-Stream interface for transmit.

#### Table C-10: Ethernet Performance Monitor, Transmit Packet Count Register (0x4AA1\_0008)

<b>Bit Position</b>	Mode	Default Value	Description
1:0		0 0	Sample count. Increments once every second.
31:2	Read Only	0	Transmit packet count. This field contains the count for the event when there is an active beat on channel 1 10G Ethernet MAC AXI4-Stream interface and end of packet (tx_axis_tlast) is asserted for transmit.

#### Table C-11: Ethernet Performance Monitor, Received Payload Byte Count Register (0x4AA1\_000C)

Bit Position	Mode	Default Value	Description
1:0		0 0	Sample count. Increments once every second.
31:2	Read Only	0	Receive payload byte count. This field contains the interface utilization count for active beats (rx_axis_tready = 1 and rx_axis_tvalid = 1) on channel 0 - 10G Ethernet MAC AXI4-Stream interface for receive.



<b>Bit Position</b>	Mode	Default Value	Description
1:0		0 0	Sample count. Increments once every second.
31:2	Read Only	0	Receive packet count. This field contains the count for the event when there is an active beat on channel 0 10G Ethernet MAC AXI4-Stream interface and end of packet (rx_axis_tlast) is asserted for receive.

#### Table C-12: Ethernet Performance Monitor, Received Packet Count Register (0x4AA1\_0010)

### Table C-13: Traffic Generator Configuration Register (0x4AA1\_0014)

Bit Position	Mode	Default Value	Description
0	Read or Write	0	Enable loopback if external generator is selected.
1		0	Enable generator if internal generator is selected.
31:16		d'125	Ethernet frame. Data payload size allowed values = 46 bytes to 1,500 Bytes.

#### Table C-14: Loopback module and PHY status Register (0x4AA1\_00x18)

<b>Bit Position</b>	Mode	Default Value	Description
0		0	PHY is up.
31	Read Only	0	Packets dropped in loopback mode when external traffic generator is selected.



# Appendix D

# Testing with an External Traffic Generator

This appendix describes how to setup and test the 10GBASE-R TRD running on the KCU105 board using an Ixia NGY-NP4-01 10 Gigabit Application Network Processor Load Module (Ixia load module).

## Requirements

### Hardware

- KCU105 evaluation board with the Kintex<sup>®</sup> UltraScale<sup>™</sup> XCKU040-2FFVA1156E FPGA
- Two USB cables, standard-A plug to micro-B plug
- Power Supply: 100 VAC-240 VAC input, 12 VDC 5.0A output
- Four SFP+ 10GBASE-SR/SW transceiver modules [Ref 5]
- Four Multimode fiber optic patch cables [Ref 18]
- Ixia XM2 portable chassis with NGY-NP4-01 10-Gigabit application network processor load module (Ixia load module) [Ref 19]

### Computer

The control computer is required for running Vivado® Design Suite, configuring the FPGA, and running the Ethernet Controller application to control and monitor the reference design. It can be a laptop or desktop computer with Microsoft Windows 7 Operating system.

### **Targeted Reference Design ZIP file**

The TRD ZIP file contains:

- Design source files
- Ethernet Controller application files
- Board design file (bitfile)
- Documentation



These files are required to demonstrate the 10GBASE-R TRD on the KCU105 evaluation board.

### Software

- Vivado Design Suite version 2017.3
- USB UART drivers (Silicon Laboratories CP210x VCP drivers)
- Java version 1.7
- Ethernet Controller application (Included with the 10GBASE-R TRD)

Software installation instructions are described in Chapter 2, Setup.

• Ixia software packages installed on the IXIA XM2 portable chassis. Software CDs and installation instructions are provided by IXIA [Ref 19].

0

**TIP:** The IXIA XM2 portable chassis with a load module has windows OS installed on it. Connect a mouse, keyboard and monitor to the chassis to run IxExplorer (The IXIA controller application)

# **Program the KCU105 Evaluation Board**

This section describes how to setup the KCU105 board with the Ixia load module and control computer and how to program the FPGA with the 10GBASE-R TRD BIT file.

- 1. Connect the KCU105 board to the Ixia load module, control computer, and power supply as shown in Figure D-1:
  - a. Connect the power supply to the KCU105 board.
  - b. Connect the USB cable having a micro-B plug to the micro-B receptacle located on U115 on the KCU105 board. Connect the standard-A plug to a USB receptacle on the control computer.
  - c. Connect the USB cable having a micro-B plug to the micro-B receptacle located at J4 on the KCU105 board. Connect the standard-A plug to a USB receptacle on the control computer.
  - d. Insert two SFP+ transceiver modules into the SFP cage on the KCU105 board.
  - e. Insert two SFP+ transceiver modules into the port 01 and port 02 cages on the Ixia load module.
  - f. Connect the four fiber optic patch cables between the two SFP+ transceiver modules on the KCU105 board and the port 01 and port 02 SFP+ transceiver modules on the Ixia load module transmit to receive and receive to transmit.






Figure D-1: KCU105 Board and Ixia Module Connections

**IMPORTANT:** Port 1 of the Ixia load module is connected to connector SPF 1 on the KCU105 board which is Channel 1 in the reference design. Port 2 of the Ixia tester is connected to connector SPF 0 on the KCU105 board which is Channel 0 in the reference design.

2. Power on the KCU105 board by placing switch SW1 to the ON position.

 $\bigstar$ 



- 3. Launch the Vivado Integrated Design Environment (IDE) on the control computer:
  - a. Select Start > All Programs > Xilinx Design Tools > Vivado 2017.3 > Vivado 2017.3.
  - b. On the getting started page, click **Open Hardware Manager** (Figure D-2).



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Figure D-2: Vivado IDE Getting Started Page, Open Hardware Manager

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- 4. Open the connection wizard to initiate a connection to the KCU105 board:
  - a. Click Open a new hardware target (Figure D-3).



Figure D-3: Using the User Assistance Bar to Open a Hardware Target

b. Configure the wizard to establish connection with the KCU105 board by selecting the default value on each wizard page. Click **Next > Next > Next > Next > Finish**.



c. In the hardware view, right-click on **xcku040** and click **program device** (Figure D-4).



Figure D-4: Select Device to Program



#### d. In the Bitstream file field, enter:

```
<working_dir>/kcu105_10gbaser_trd/ready_to_test/kcu105_10gbase
r_download.bit
```

and click **Program** (Figure D-5).

ptionally select a debi itstream programmin	g probes file that correspo file.	nds to the debug c	ores contained ir	n the 🔥
Bitstre <u>a</u> m file:	[RD/UG921/2017.1/ready	_to_test/kcu105_1	Ogbaser_downlo	ad.bit 区
Debu <u>q</u> probes file:				
✓ Enable end of s	artup check			
?			Program	Cancel

Figure D-5: Program Device Window

After completing these steps, continue on to Set Up the Ixia Load Module Parameters.



### Set Up the Ixia Load Module Parameters

This section describes how to setup the Ixia Load Module Ethernet parameters using IxExplorer.

- 1. Power on the Ixia XM2 portable chassis.
- Launch Ixia IxExplorer on the Ixia chassis. Click Start > All Programs > Ixia > Ixia Application Selector > IxOS > IxOS 6.10.750.5 EA > Ixia IxExplorer (Figure D-6).

Adobe Reader X Internet Explorer Accessories	•	
James		ixia
uia Ixia		
Advanced Information Manager	Ε	Documents
IxOS		
🍌 IxOS 6.10.750.5 EA		Computer
🦨 ActiveTcl Wish Console		Network
Ixia IxExplorer		
🔀 Ixia IxServer 🔛 ScriptGen		Control Panel
🆕 Wish Console		Devices and Printers
🎍 Licensing	Ŧ	
4 Back		Run
Search programs and files	]	Shut down 🕨

*Figure D-6:* **Open Ixia IxExplorer** 

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3. Confirm the link between the KCU105 board and the Ixia load module is up. The green icons shown Figure D-7 shows that Port 01 and Port 02 are connected and operating.

🔀 IxExplorer - 6.10.750.5 EA - Untitled.cfg	
Eile Edit View Transmit Capture Collisions Latency Statistics Multiuse	r <u>T</u> ools <u>W</u> indow <u>H</u> elp
Explore Network Resources      Chassis Chain01      Chassis Chain01      Chassis 01      Port 01 - LAN/WAN SFP+ 10GBASE-SR/LR      Port 02 - LAN/WAN SFP+ 10GBASE-SR/LR      Port 03 - LAN/WAN SFP+ 10GBASE-SR/LR      Port 04 - LAN/WAN SFP+ 10GBASE-SR/LR      MII Templates      MII Templates      Layouts	

X19126-041817

Figure D-7: IxExplorer Showing E-7 Link is Up Between the KCU105 Board and Ixia Load Module



4. Click the + next to Port 01 and Port 02 to expand both ports (Figure D-8).



X19120-041817

Figure D-8: Expanded Port 01 and Port 02



5. Click **Packet Streams** on Port 01 to display Ethernet packet parameters (Figure D-9).

Image: State in the state	🗽 txExplorer - 6.10.750.5 EA - Untitled.cfg		
Else Edit View Transmit Capture Caplisions Latency Statistics Multiguer Tools Window Help         Image: Statistic Charitor         Image: Statistic Charitor         Image: Statistic Charitor         Image: Statistic View	<b>2    × № 6    (1 1 1    0    0    0    0   </b>    0    0		
Image: State of the state	<u>Eile E</u> dit <u>V</u> iew T <u>r</u> ansmit C <u>a</u> pture C <u>o</u> llisions <u>L</u> atency Statistics Multi <u>u</u>	<u>u</u> ser <u>T</u> ools <u>W</u> indow <u>H</u> elp	
Explore Network Resources         Image: Control of Control Mode           Image: Control Control Mode         Control Mode           Image: Control Control Mode         Control Contro	<i>□ □ □</i> →		
Resources Central 22 - NGV-NP4 Portot - LANWAN SPP- 10GBASE-SR/LR Portot - LANWAN SPP- 10	Explore Network Resources		
e m No user is logged in.	Poprofer VetWork Kesources     Presources     Chassis Chain01     Chassis 01     Port 01 - LAN/WAN SFP+ 10GBASE-SR/LR     Packet Streams     Statistic View     Port 02 - LAN/WAN SFP+ 10GBASE-SR/LR     Port 02 - LAN/WAN SFP+ 10GBASE-SR/LR     Port 03 - LAN/WAN SFP+ 10GBASE-SR/LR     Port 03 - LAN/WAN SFP+ 10GBASE-SR/LR     Port 04 - LAN/WAN SFP+ 10GBASE-SR/LR     Port 04 - LAN/WAN SFP+ 10GBASE-SR/LR     MII Templates     Layouts	Image: Section 2010       Apply       Section 2010       Befresh Interfaces         Average       Average       100       Average         Inne Rate       10,000       Mbps       Total % Max.       100         Total Data Bit Rate       9.275.362       Mbps       Fixed Mode         Min.       0       Max       10       Total Packets/Sec.       4.528.385.5       fps         Enable       Suspend       Name       Flow       Control       Loop       Frame       Data Pattern         1       T       Continuous Packet       20,000       256       Inc Byte	
✓ III No user is logged in.			
		m No us	er is logged in.

X19131-070717

Figure D-9: Open Packet Streams on Port 01



- 6. Configure frame size, destination, source MAC addresses, and frame type:
  - a. Click **line 1** (highlighted in Figure D-9) to open the stream properties window.
  - b. Select the **DA/SA** tab (Figure D-10) and set the parameters as described here:
    - Frame Size: **1,518** Bytes (Includes Ethernet header and CRC)
    - Destination Address: 00 00 00 00 22 22
    - Source Address: 00 00 00 44 44
    - All other parameters should match values and selections shown in Figure D-10.

Preamble	Type Inc I	• (Starting at offset 14) Byte	Edit	Frame Size Fixed C Rando C Increm C Auto	e (Includes CRC) Size 1.518 m Min 64 ent Max 1.518
DA / SA Protocols Table Destination Address Mode Fixed Value 00 00 00 00 22	UDF   UDF1   UI	DF2   UDF3   UDF4   UD Repeat Count   16	F5  Auto A	ddress	Instrumentation     Offsets     Automatic     Time Stamp     Packet Groups     Sequence Checking     Data Integrity     PRBS
Node Fixed Value 00 00 00 00 44	44	Repeat Count 16	Auto A	iddress	Edit

X19145-041817

Figure D-10: Set Frame Size and Addresses (DA/SA Tab)

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- 7. Select the **Protocols** tab (Figure D-11) and set the parameters as described here:
  - Select 802.3 Raw frame type
  - All other parameters should match values and selections shown in Figure D-11.

Preamble Data FB 55 55 55 55 55 55 D5 Edit	Data Pattem - ( Type Inc Byt Data 00 01	Starting at offset 14)	Edit	Frame Size Fixed C Randon C Increme C Auto	(Includes CRC ) Size 1.518 Min 64 Max 1.518
DA / SA Protocols Table L Data Link Layer ISL VLAN(s) MPLS		2 UDF3 UDF4 UD Protocols © None © IPv4 © IPv4 / IPv6 © IPv6 © IPv6 / IPv4	C IPX Ec C ARP C ARP	fit	Instrumentation Offsets Automatic Time Stamp Packet Groups Sequence Checking Data Integrity PRBS
C None Type C Ethemet II FFF C Ethemet Snap C 802.3 Raw C 802.2 (IPX)	e F	None     TCP / IP     ICMP / IP     IGMP / IP     GOSPF / IP	C UDP/IP C RIP/UDP/IP C DHCP/UDP/IP C GRE/IP		Edit Force Errors No Error Bad CRC No CRC
C Protocol Offset	Edit Offset	Protocol Pad	Edit Data		

X19146-041817

Figure D-11: Set Frame Type to 802.3 (Protocols Tab)



- 8. Select the **Stream** tab (Figure D-12) and set the parameters as described here:
  - Set the Inter Packet gap to 16 bytes
  - Set enforce minimum to 12 bytes
  - All other parameters should match values and selections shown in Figure D-12.
- 9. Click **OK**.

Name Continuous Packet	C         % Max. Rate         C         Packets/Sec         C         Bit Rate         (bps)           99.740597         810,635.54         9.844358e+009
C Continuous Burst Stop after this Stream Advance to Next Stream Retum to ID Retum to ID for Count	Inter-Packet Gap     Enforce Min.       16     Bytes     12
Netum to ID     1       oop Count     20,000       Vackets per Burst     1	Inter-Burst Gap
lursts per Stream	11.2     Nanoseconds       ** This delay will be active after completing this stream **
	Update Gaps

Figure D-12: Stream Control Tab Settings

**IMPORTANT:** The inter-packet gap is set to 16 bytes to accommodate the parts per million (ppm) difference between the Ixia load module clock source and the KCU105 board clock source. In this lab setup, the Ixia load module clock is running faster than the KCU105 board clock. Because the TRD loops back the data coming from the Ixia load module through a FIFO, this FIFO will overflow at some point of time if the IPG is set to 12 on both the Ixia load module and the 10GBASE-R TRD. This is because the receive clock (from the Ixia load module) is faster than the transmit clock (from the KCU105 board). If the transmit data was not dependent on the receive data then the IPG could be set to 12 bytes.

10. Repeat step 5 through step 7 for Port 02 but set the destination address to **00 00 00 00 11 11** and source address to **00 00 00 33 33**.

After completing these steps, continue on to Launch the Ethernet Controller Application.

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### **Running the Design**

#### Launch the Ethernet Controller Application

 Launch the Ethernet Controller application on the control computer. Click Start > All Programs > Xilinx > EthernetController (Figure D-13).



*Figure D-13:* **Ethernet Controller Application** 

 Select the COM port associated with the Silicon Labs CP210x USB to UART Bridge and click **Connect** (Figure D-14) to open the Ethernet Controller application for the 10GBASE-R TRD.

**TIP:** The COM port associated with the Silicon Labs CP210x USB to UART Bridge can be identified using the Windows control panel. See step 3, page 12.



🛓 Ethernet Con	troller		_ <b>_ x</b>
	Ethernet	Control	ler
COM Port:	COM1 COM1		Refresh
	COM3 COM18 COM19 LPT1		Connect

X19139-070717

Figure D-14: Select COM Port Associated with the USB to UART Bridge

3. Ethernet channel 0 and channel 1 are up and ready when the ETH0 PHY and ETH1 PHY indicators are green. For both channels select **External Generator** and click **Start** (Figure D-15).

🛃 10GBASE-R Ethernet TRD		And and a second s	
	KUCon-TRD04 10GBASE-R Ethern	net Targeted Reference Design	Block
ALL PROGRAMMABLE.	ETH0 PHY	ETH1 PHY	diagram
Performance Plots Channel 0 Statistics	Channel 1 Statistics		
Channel 0		Channel 1	
Control Panel		Control Panel	
Internal Generator		Internal Generator	
Payload: External Generator	Stop	Payload: External Generator	Stop
Tx Statistics	Rx Statistics	Tx Statistics Rx Statistics	
Throughput (Gbps): 0.00	Throughput (Gbps): 0.00	Throughput (Gbps): 0.00 Throughput (Gbps)	0.00
Packet Count: 0		Packet Count. 0	
10.0 7.5 7.5 2.5 0.0		10.0 (stdg) 10.0 7.5 5.0 2.5 0.0	
1 2 3	4 5 6 7 8 9 phput Rx Throughput	1 2 3 4 5 6 7	8 9

X19144-041817

Figure D-15: Set External Generator on the Channels



#### **Start Traffic Generation**

1. To start traffic generation by the Ixia load module, switch to IxExplorer on the Ixia chassis, and right-click on **Port 01 Statistics view** and click on **Start Transmit** (Figure D-16).

g IxExplorer - 6.10.750.5 EA - Untitled.cfg								
File Edit View Transmit Capture Collisions Latency Statistics Multi	user Tools Window Help							
Explore Network Resources								
E -	Stats For 10.0.0.1:02.01	Count	Rate	Logging				
📋 🧰 🧰 Chassis Chain01	Link State	Link Up						
📋 🥥 🕒 Chassis 01	Line Speed	10GE LAN						
🚊 🕮 Card 02 - NGY-NP4	Frames Sent	0	0					
🚊 📲 Port 01 - LAN/WAN SFP+ 10GBASE-SR/LR	Valid Frames Received	0	0					
Packet Streams	Bytes Sent	0	0					
Statistic View	Bytes Received	0	0					
🗄 💼 Management 🕨 Start Transmit	5	0	0					
Port 02 - LAN/W Stop Transmit	nd Good CRCs	0	ŏ					
🗈 Packet Strean 🚹 Pause Transmit	s s	ő	ŏ					
Statistic View 🕨 Step Transmit	ed Frames	0	ō					
A Management	rol Frames Received	0	0					
Port 03 - LAN/W 🕪 Start Capture	nd CRC Errors	0	0					
Port 04 - LAN/W Stop Capture	ied Stat 1	0	0					
Global Views	ied Stat 2	0	0	=				
	rigger (UDS 3)	0	0					
Start Collisions	ilter (UDS 4)	0	0					
Stop Collisions	ied Stat 5	0	0					
	ied Stat 6	0	0					
Arp Reguest	erver Transmit	0						
	erver Receive	0						
User <u>M</u> anagement	Arp Keply	0						
Logging and Alerts Configuration	Arp Request	0						
	Transmit Ping Request	0						
	Receive Arn Renky	0						
	Receive Arp Request	ő						
	Receive Ping Reply	0						
	Receive Ping Request	0						
	IPv4 Packets Received	0	0					
	UDP Packets Received	0	0					
	TCP Packets Received	0	0					
	IPv4 Checksum Errors	0	0	-				
·				F.				
Start transmitting Packet Streams			No user is	logged in.				
-								

X19149-041817

Figure D-16: Start Traffic on Port 01



2. Repeat step 1 on Port 02 (Figure D-17).

📧 IxExplorer - 6.10.750.5 EA - Untitled.cfg				
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Eile Edit View Transmit Capture Collisions Latency Statistics Mu	ılti <u>u</u> ser <u>T</u> ools <u>W</u> indow <u>H</u> elp			
∅ ↓ ↓ ↔ ∞ ∞ ♥ ♦ ₩ ■ Ⅱ ₩				
Explore Network Resources				Â
E B Resources	Stats For 10.0.0.1:02.02	Count	Rate	Logging
🖨 🧰 Chassis Chain01	Link State	Link Up		
👝 🥥 Chassis 01	Line Speed	10GE LAN		
🖃 🕮 Card 02 - NGY-NP4	Frames Sent	0	0	
🗄 📲 Port 01 - LAN/WAN SFP+ 10GBASE-SR/LR	Valid Frames Received	0	0	
Packet Streams	Bytes Sent	0	0	
Statistic View	Bytes Received	0	0	
H Management Interface	Fragments	0	0	
Port 02 - LAN/WAN SEP+ 10GBASE-SR/LR	Undersize	0	0	
Dacket Streams	CRC Farmer	0	0	
Statictic View	Vian Tagged Frames	0	0	
	trol Frames Received	0	0	
	and CBC Errors	0	ő	
Port 03 - LAN/V Stop Transmit	ned Stat 1	0	0	
Port 04 - LAN/V Pause Transmit	ned Stat 2	0	0	E
Global Views Step Transmit	rigger (UDS 3)	0	0	
MII Templates	ilter (UDS 4)	0	0	
Layouts Start Capture	ned Stat 5	0	0	
Stop Capture	ned Stat 6	0	0	
Clear All Statistics	erver Transmit	0		
	erver Receive	0		
Start Collisions	Arp Reply	0		
Stop Collisions	Arp Request	0		
	Ping Reply	0		
Arp Keguest	Ping Request	0		
User Management	ITP Reply	0		
	ing Reply	0		
Logging and Alerts Configurat	ion	0		
	IPv4 Packets Received	0	0	
	UDP Packets Received	0	ŏ	
	TCP Packets Received	0	0	
	IPv4 Checksum Errors	0	0	-
	1		2	
Start transmitting Packet Streams			No use	er is logged in.

Figure D-17: Start Traffic on Port 02

X19150-041817



 $\bigcirc$ 

3. The Ethernet Controller application (Figure D-18) shows the performance achieved with a packet size of 1,518 bytes is 9.74 Gb/s per channel per direction.

**TIP:** The relationship between payload size and throughput can be demonstrated by changing the payload size. Reducing the payload size set in IxExplorer will cause a dip in performance. Refer to Appendix B, Performance Estimates for performance estimation on 10G Ethernet protocol.



X19155-041817

*Figure D-18:* Throughput Performance Plots, External Generator



4. Using IxExplorer (Figure D-19), stop traffic generation on Port 01 by right-clicking on **Port 01 Statistics view** then click on **Stop Transmit**.



X19151-041817





5. Repeat step 4 on Port 02 (Figure D-20).

LE IxExplorer - 6.10.750.5 EA - Untitled.cfg				
🚅 🖬 🗙 🖻 🛱 😭 🐛 🖻 🖬 🖻 🛤 🤶 🔒 📰				
<u>File Edit View Transmit Capture Collisions Latency Statistics Mu</u>	ılti <u>u</u> ser <u>T</u> ools <u>W</u> indow <u>H</u> elp			
				*
Explore Network Resources	C 5 100010202	10.		<u> </u>
E- Character Charle 01	Stats For 10.0.0.1:02.02	Count	Kate	Logging
	Link State	Link Up		
	Line Speed	TOGE LAN	0	
□ I I I Card 02 - NGY-NP4	Frames Sent	37,009,780	0	
Port 01 - LAN/WAN SFP+ 10GBASE-SR/LR	Pater Cent	57,299,129	0	
Packet Streams	Bytes Perceived	56 509 261 014	0	
Statistic View	Fragments	0	0	
😥 🧰 Management Interface	Hoderrize	0	0	
Port 02 - LAN/WAN SFP+ 10GBASE-SR/LR	Oversize and Good CBCs	0	0	
Packet Streams	CRC Errors	0	0	
Statistic View	Vian Tagged Frames	0	0	
Managemen Start Transmit	trol Frames Received	0	ů.	
	and CRC Errors	0	0	
	ned Stat 1	0	0	=
E- Port 04 - LAN/V II Pause Transmit	ned Stat 2	0	0	
Global Views	rigger (UDS 3)	37,299,129	0	
MII Templates	ilter (UDS 4)	37,299,129	0	
Stop Capture	ned Stat 5	0	0	
2 Clear All Statistics	erver Transmit	0	0	
	erver Receive	0		
Start Collisions	Arp Reply	0		
Stop Collisions	Ping Reguest	0		
🚠 Arp Request	Ping Request	0		
User Management	rp Reply	0		
	ing Reply	0		
Logging and Alerts Configurat	ion ing Request	0		
	IPv4 Packets Received	0	0	
	UDP Packets Received	0	0	
	TCP Packets Received	0	0	
	I IPv4 Checksum Errors	0	0	
] • [				*
Stop transmitting Packet Streams			No	user is logged in. 🛛 🎢

X19152-041817





6. Select **Statistics View** for Port 01 (Figure D-21) and verify if any packets were in error or were dropped.

🗶 IxExplorer - 6.10.750.5 EA - Untitled.cfg				
」 <mark>☞ ⊌</mark>   X 响 ₪   <mark>۞ *~</mark>   ⊟ □ ⊡ ⊡   A   ¥   ⊕   ⊞				
<u>Eile Edit View Transmit Capture Collisions Latency Statistics Mu</u>	lti <u>u</u> ser <u>T</u> ools <u>W</u> indow <u>H</u> elp			
@ @ ⇒ ▶ 66 % ♥ ▶ ₩ ■ Ⅱ ▶ 표				
Explore Network Resources				
Resources	Stats For 10.0.0.1:02.01	Count	Rate	Logging
- Chassis Chain01	Link State	Link Un		
🛱 🙆 Chassis 01	Line Speed	10GE LAN		
Card 02 - NGV-NP4	Frames Sent	10,273,205	0	
Det 01 - LAN/WAN SED+ 10GBASE-SP/LP	Valid Frames Received	10,747,151	0	
	Bytes Sent	15,594,725,190	0	
Charles Packet Streams	Bytes Received	16,314,175,218	0	
Statistic View	Fragments	0	0	
H	Undersize	0	0	
Port 02 - LAN/WAN SFP+ 10GBASE-SR/LR	Oversize and Good CRCs	0	0	
Packet Streams	CRC Errors	0	0	
	Vlan Tagged Frames	0	0	
🕀 🧰 Management Interface	Flow Control Frames Received	0	0	
Port 03 - LAN/WAN SFP+ 10GBASE-SR/LR	Oversize and CRC Errors	0	0	
Port 04 - LAN/WAN SEP+ 10GBASE-SR/LR	User Defined Stat 1	0	0	
🖂 🗍 Global Views	User Defined Stat 2	0	0	
MIT Tomplator	Capture Trigger (UDS 3)	10,747,151	0	E
in templates	Capture Filter (UDS 4)	10,747,151	0	
Layouts	User Defined Stat 5	0	0	
	User Defined Stat 6	0	0	
	ProtocolServer Transmit	0		
	ProtocolServer Receive	0		
	Transmit Arp Reply	0		
	Transmit Arp Request	0		
	Transmit Ping Reply	0		
	Transmit Ping Request	0		
	Receive Arp Reply	0		
	Receive Arp Request	0		
	Receive Ping Reply	0		
	Receive Ping Request	0	0	
	IPV4 Packets Received	0	0	
	TCD Dackets Received	0	0	
	IByd Chackrup Errors	0	0	
	LIDP Checksum Errors	0	0	
	TCP Checksum Errors	0	0	
	rer encedant enors		v	
4	I			
			L. P. C.	
			No u	ser is logged in.

X19156-041817

Figure D-21: Traffic Statistics on Port 01



7. Select **Statistics View** for Port 02 (Figure D-22) and verify if any packets were in error or were dropped. The transmit frame count for Port 02 should match the receive frame count for Port 01. The transmit frame count for Port 01 should match the receive frame count for Port 02.

-		5		
Ella Edit View Transmit Cantura Collisions Latency Statistics Multi	iurer Tools Window Help			
The Edit View Hanshine Captore Consisting Entercy Statistics man				
Explore Network Resources				<u>^</u>
E- P Resources	Stats For 10.0.0.1:02.02	Count	Rate	Logging
Chassis Chain01 Chassis 01 Card 02 - NGY-NP4 Card 02 - NGY-NP4 Card 02 - LAN/WAN SFP+ 10GBASE-SR/LR Card 02 - LAN/WAN SFP+ 10 - L	Link State Line Speed Frames Sent Valid Frames Received Bytes Sent Bytes Received Fragments Undersize Oversize and Good CRCs CRC Errors Vlan Tagged Frames Flow Control Frames Received Oversize and CRC Errors User Defined Stat 1 User Defined Stat 1 User Defined Stat 2 Capture Filter (UDS 4) User Defined Stat 5 User Defined St	Link Up 10GE LAN 37,669,786 37,299,129 57,182,735,148 56,598,261,014 0 0 0 0 0 0 0 0 0 0 0 0 0		E
·	I IPV4 CHECKSUM ENDIS	U	U	ь
			Not	user is logged in. 🗌 🏑

X19157-041817

Figure D-22: Traffic Statistics on Port 02



8. Using the Ethernet Controller application, select the **Channel 0 Statistics** tab and verify if any packets were in error or were dropped (Figure D-23).

		Hernet Hungeten Kererenete Design	
OGRAMMABLE.	H0 PHY	ETH1 PHY	
Plots Channel 0 Statistics Channel 1 Statistic	cs		
< Statistics		Rx Statistics	
Throughput (Gbps): 0.00 Packet	Count 0	Throughput (Gbps): 0.00 Packet	Count: 0
MAC TX Statistics	Value	MAC RX Statistics	Value
Frames transmitted	10273205	Frames received	10747151
Transmitted Bytes	15594725190	Received Bytes	16314175218
		Frame Check Sequence errors	0
Broadcast frames transmitted	0	Broadcast frames received	0
Multicast frames transmitted	0	Multicast frames received	0
64-byte frames transmitted	0	64-byte frames received	0
65–127 Byte frames transmitted	0	65–127 Byte frames received	0
128–255 Byte frames transmitted	0	128–255 Byte frames received	0
256–511 Byte frames transmitted	0	256–511 Byte frames received	0
512–1023 Byte frames transmitted	0	512–1023 Byte frames received	0
1024 – MaxFrameSize Byte frames transmitted	102/3205	1024 – MaxFrameSize Byte frames received	10/4/151
Control frames transmitted	0	Control frames received	0
10 AN Average of Generation and and		Undersize frames received	0
VLAN tagged frames transmitted	0	VLAN tagged frames received	0
PAUSE frames transmitted	0	PAUSE frames received	0
Control frames received with unsupported opc	. 0	Control frames received with unsupported opcode	U Contraction of the second se
Oversize frames transmitted	U	Oversize frames received	0
		Length/Type out of range	0
Underrun errors		Fragment Trames received	

X19110-041817

*Figure D-23:* Channel 0 MAC Statistics



9. Using the Ethernet Controller application, select the Channel 1 Statistics tab and verify if any packets were in error or were dropped (Figure D-24). The TX MAC statistics for Channel 1 should match the RX MAC statistics of Channel 0. The TX MAC statistics for Channel 0 should match the RX MAC statistics of Channel 1. The numbers should also match up with the statistics reported by the Ixia load module in IxExplorer.

KUCon-TR	D04 10GBASE-R Eth	ernet Targeted Reference Design		Block
ROGRAMMABLE. O	THO PHY	ETH1 PHY		diagi
ce Plots Channel 0 Statistics Channel 1 Statis	tics			
Tx Statistics		Rx Statistics		
Throughout (Chos): 0.00 Backs	t Count	Throughout (Choc): 0.00 Packa	t Count 0	
MAC TX Statistics	Value	MAC RX Statistics	Value	
Frames transmitted	10747151	Frames received	10273205	
Transmitted Bytes	16314175218	Received Bytes	15594725190	
		Frame Check Sequence errors	0	
Broadcast frames transmitted	0	Broadcast frames received	0	
Multicast frames transmitted	0	Multicast frames received	0	
64-byte frames transmitted	0	64-byte frames received	0	
65–127 Byte frames transmitted	0	65–127 Byte frames received	0	
128–255 Byte frames transmitted	0	128–255 Byte frames received	0	
256–511 Byte frames transmitted	0	256–511 Byte frames received	0	
512–1023 Byte frames transmitted	0	512–1023 Byte frames received	0	
1024 – MaxFrameSize Byte frames transmitted	10747151	1024 – MaxFrameSize Byte frames received	10273205	
Control frames transmitted	0	Control frames received	0	
		Undersize frames received		
VLAN tagged frames transmitted		VLAN tagged frames received	0	
PAUSE frames transmitted	0	PAUSE frames received		
Control frames received with unsupported opc.		Control frames received with unsupported opcode	2 0	
Oversize frames transmitted		Oversize frames received		
		Length/Type out of range		
		Fragment frames received		
Underrun errors				

X19018-041817

Figure D-24: Channel 1 MAC Statistics

**IMPORTANT:** When running traffic on both channels, If external generator mode is selected on one channel, then external generator mode should also be selected on the other channel.



5



Appendix E

# Additional Resources and Legal Notices

#### **Xilinx Resources**

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

#### **Solution Centers**

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

#### **Documentation Navigator and Design Hubs**

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select Start > All Programs > Xilinx Design Tools > DocNav.
- At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

*Note:* For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.



## References

The most up-to-date information for this design is available on these websites:

KCU105 Evaluation Kit website

KCU105 Evaluation Kit documentation

KCU105 Evaluation Kit Master Answer Record (AR 63175)

These documents and sites provide supplemental material:

- 1. Vivado Design Suite User Guide Release Notes, Installation, and Licensing (UG973)
- 2. Silicon Labs CP210x USB to UART Bridge VCP Drivers
- 3. Silicon Labs CP210x USB-to-UART Installation Guide (UG1033)
- 4. Vivado Design Suite User Guide: Logic Simulation (UG900)
- 5. Avago Technologies AFBR-709SMZ 10 Gb/s Ethernet, 850 nm, 10GBASE-SR, SFP+ Transceiver
- 6. 10 Gigabit Ethernet PCS/PMA (10GBASE-R) website
- 7. 10G Ethernet PCS/PMA LogiCORE IP Product Guide (PG068)
- 8. 10 Gigabit Ethernet Media Access Controller (10GEMAC) website
- 9. 10G Ethernet MAC LogiCORE IP Product Guide (PG072)
- 10. AXI4-Lite IPIF LogiCORE IP Product Guide (PG155)
- 11. UltraScale Architecture System Monitor User Guide (UG580)
- 12. System Management Wizard LogiCORE IP Product Guide (PG185)
- 13. MicroBlaze Soft Processor Core website
- 14. AXI Interconnect website
- 15. AXI UART Lite LogiCORE IP Product Guide (PG142)
- 16. AXI UART Lite website
- 17. Processor System Reset Module
- Amphenol Corporation Amphenol part number FO-LCX2SIMP00-003, LC-LC Simplex Single-Mode 9/125 Fiber

Optic Patch Cable (OFNR Riser) - LC Male to LC Male (Figure D-1 shows cable application)





#### 19. <mark>Ixia</mark>

XM2 Portable Chassis, NGY-NP4-01 10-Gigabit Application Network Processor Load Module and software CD

- 20. KCU105 Evaluation Board for the Kintex UltraScale FPGA (UG917)
- 21. Amphenol Corporation

Amphenol part number FO-10GGBLCX20-001, LC-LC Duplex 10Gb Multimode 50/125 OM3 Fiber Optic Patch Cable - 2 x LC Male to 2 x LC Male (Figure 3-1 shows cable application)

22. Oracle

Java SE Runtime Environment 7 Downloads

#### **Training Resources**

- 23. Vivado Design Suite Hands-on Introductory Workshop
- 24. Vivado Design Suite Tool Flow

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