XILINX AUTOMOTIVE — FLEXIBLE SOLUTIONS BEYOND SILICON

XILINX®

ENABLING NEXT-GENERATION AUTOMOTIVE ELECTRONICS

Consumers expect driving experiences to align with their technology-oriented digital lifestyles. Each manufacturer is competing to provide the best "connected car" that also maximizes safety on the road. However, economic realities require meeting these goals with fewer resources, smaller budgets, and tighter schedules. Xilinx programmable logic devices yield proven results that go beyond silicon—getting designs to market faster and at lower cost.

DISCOVER XILINX AUTOMOTIVE PLATFORMS AND SOLUTIONS

The Xilinx Automotive Advantage

- PROGRAMMABLE PLATFORMS WITH SYSTEM-LEVEL SCALABILITY AND INTEGRATION
- PROVEN PORTFOLIO OF AUTOMOTIVE QUALIFIED STANDARD DEVICES, WITH ON-CHIP EMBEDDED DSP AND SERIAL CONNECTIVITY RESOURCES
- COMPLETE ECOSYSTEM OF SOFTWARE, IP, DESIGN TOOLS AND DESIGN SERVICES

Advocating Quality and Innovation

-Certified to ISO-9001, ISO-14001

- Support for vehicle networking standards including MOST®, CAN, APIX , and Ethernet AVB

- Member of the Automotive Electronics Council (AEC) Technical Specification Committee

- Member of JASPAR, GENIVI Alliance, and MOST Cooperation

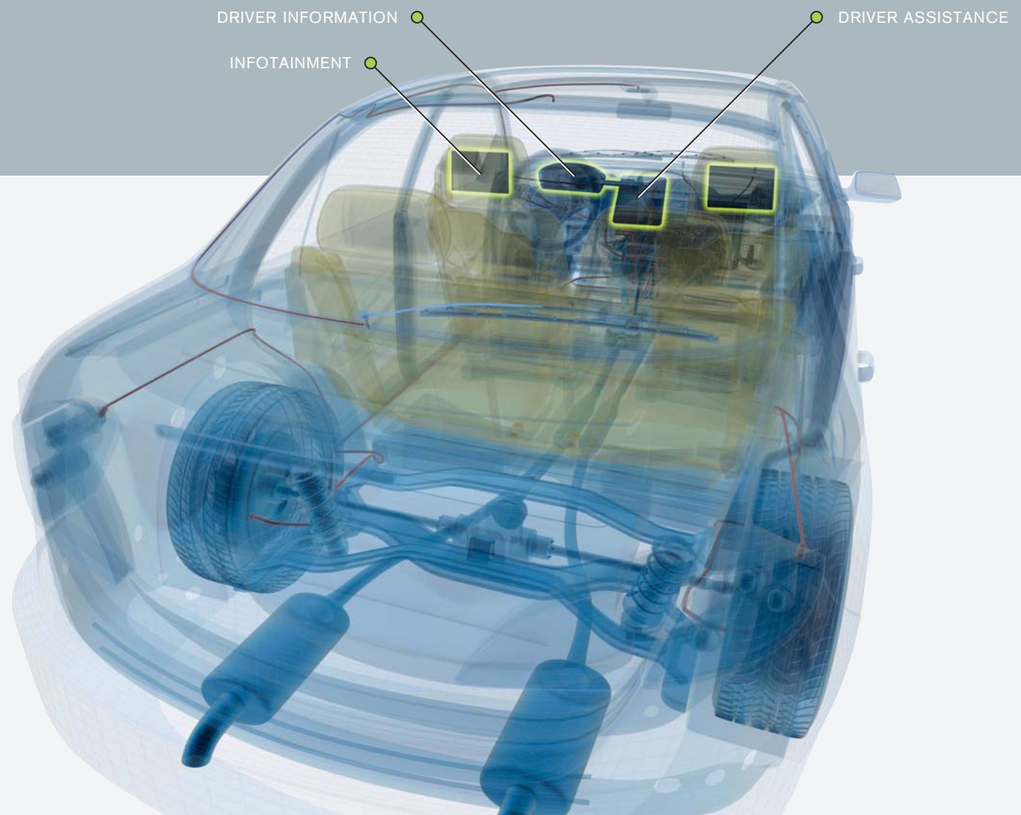
- Founding member of AVnu Alliance

Xilinx is the worldwide leading supplier of programmable logic devices to the automotive market with a proven track record of delivering platforms that go beyond silicon. The Xilinx Automotive (XA) product family is the programmable engine for many of today's automotive electronic systems and a compelling choice for next-generation:

- Infotainment
- Driver assistance
- Driver information systems

With the freedom to upgrade products in the field, even after manufacturing, system developers can respond quickly to changing standards and application requirements.

Xilinx, with Alliance Program member companies and leading-edge automotive suppliers, provides key IP building blocks, operating system and software support, expert custom development, and system integration services.



TAILORED AUTOMOTIVE PLATFORMS

Xilinx enables automotive engineers to meet the demands for greater product differentiation, innovation, and flexibility with next-generation Targeted Design Platforms tailored for specific industry applications. With the Xilinx programmable advantage, the dynamic application requirements of multiple vehicle platforms can be addressed in a scalable, timely, and cost-effective manner.

Xilinx is at the forefront of the 'Programmable Imperative' with an integrated platform approach that combines the latest silicon innovations with complete advanced system development environments specifically tailored for automotive applications.

Xilinx programmable platforms enable automotive electronics developers to spend less time on the infrastructure of applications and more time creating value with designs that enhance the user experience of next-generation infotainment, driver assistance and driver information systems.

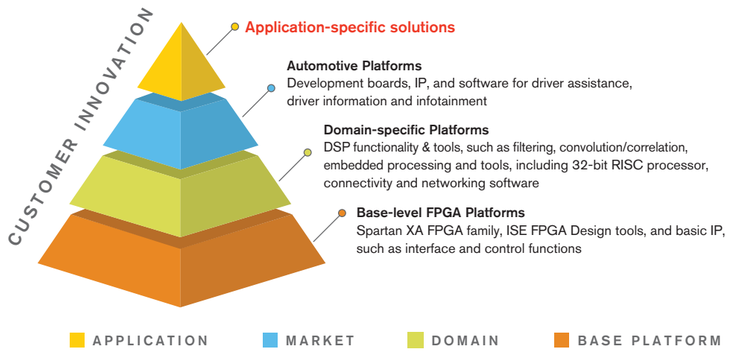
Addressing the Automotive Programmable Imperative

- Industry-leading silicon quality and value in price, power, performance
- Fully integrated hardware and software development platforms
- Smart design methodologies for fast time to innovation
- Programmability for flexible vehicle networking and connectivity
- Real-time performance for image processing and recognition
- High resolution video and graphics solutions for in-vehicle displays

Xilinx Automotive Platforms:

- Image Processing and Recognition
- High-Resolution Video and Graphics
- Vehicle Networking and Connectivity

TARGETED DESIGN PLATFORM FOR AUTOMOTIVE



Focus on Product Differentiation

Targeted Design Platforms from Xilinx ensure optimal performance, the highest quality results, and a superior design experience. Developers can focus on innovation and differentiation throughout product development with an integrated set of hardware and software elements, including silicon devices, IP, application software, design tools, and development kits with pre-validated reference designs.

IMAGE PROCESSING & RECOGNITION

Xilinx Automotive FPGAs offer low-cost digital signal processing with the higher bandwidth and lower power required for high-volume driver assistance (DA) systems, delivering the real-time processing performance that is ideal for vision-based applications requiring a throughput minimum of 30 frames per second.

XA Spartan® series FPGAs deliver more raw DSP throughput than any other low-cost FPGA with parallel processing, significantly outperforming traditional serial DSP families. Domain-optimized devices offer high I/O-to-logic ratio and high-bandwidth DSP with lower power consumption, abundant on-chip system resources, and broad connectivity support. Additionally, in a market that is driven by differentiation, the reprogrammability of FPGAs offer customization advantages over fixed function hardware accelerator blocks found in serial DSPs. With more functionality and bandwidth per dollar than was previously possible, XA Spartan FPGAs set new standards in the programmable logic industry and offer a cost-effective, reconfigurable alternative to ASICs, ASSPs, and microcontrollers.

The Challenges

- Real-time processing of high resolution images is beyond serial DSP capabilities
- Emerging market with changing standards, dynamic application requirements, and rapid algorithm evolution late in the development cycle

The Xilinx Advantage

- FPGA parallel processing provides high data throughput needed for real-time sensor data crunching
- Programmable devices and IP blocks enable late stage design changes without significant time-to-market impact
- Reconfigurable hardware offers the flexibility to implement “in-system” feature changes and product upgrades
- Range of FPGA densities and packages means that standard platforms can be easily scaled and features bundled based on application requirements

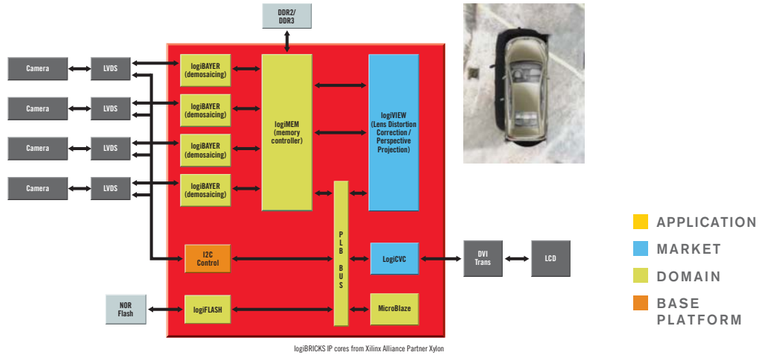
Vision-based Driver Assistance Applications:

- Night Vision
- Lane Departure Warning
- Park/Back-up Aid
- Surround Vision
- Blind-spot Detection
- Collision Warning
- Pedestrian Detection
- Stereo Vision
- Sign Recognition

XILINX AUTOMOTIVE TARGETED DESIGN PLATFORM

Four-Camera System for Surround View

The Xilinx Automotive Targeted Design Platform for four-camera surround view provides the multi-camera support and image processing needed to stitch four images into a seamless single image with 3D multi angle view. Extensive image processing IP, image compensation for fish eye lens and camera offsets are used to provide a single matched image for parking assistance.



logiBRICKS IP cores from Xilinx Alliance Partner Xylon

BASE PLATFORM

Spartan-6 FPGA SP605 Evaluation Kit

The Spartan-6 FPGA SP605 Evaluation Kit delivers the base features of a Xilinx Targeted Design Platform in one flexible environment for system design. The kit integrates hardware, software, IP, and pre-validated reference design — and examples on how to leverage features such as high-speed serial transceivers, PCI Express,® DVI, and/or DDR3 — so designers can begin development right out of the box.

- The Spartan-6 FPGA SP605 Evaluation Kit is used as the base platform for the Surround View Targeted Design Platform with an additional camera interface board connected via the FMC (FPGA Mezzanine Card) connector and four cameras.

HIGH RESOLUTION VIDEO & GRAPHICS

Xilinx Automotive FPGAs provide the flexibility and scalability to support a wide range of high resolution video and graphics systems with the LCD/TFT interfacing capabilities required for automotive infotainment, driver information, and driver assistance applications.

Tomorrows instrument clusters require electromechanical gauges and digital displays in varying numbers and combinations. The broad range of display technologies, resolutions, and interfaces also poses challenges for designers of next-generation driver information and infotainment systems.

With XA devices, designers can change the number and types of displays or mechanical gauges without changing the base silicon or overall system architecture. This includes the ability to control optional heads-up displays. This physical connection to displays is also greatly simplified with built-in support for various I/O standards, including Reduced Swing Differential Signaling (RSDS) and Low Voltage Differential Signaling (LVDS).

The Challenges

- Increased visual content for driver information and infotainment applications
- Support for LCD/TFT-based message centers, gauges, heads-up displays, and entire instrument clusters

The Xilinx Advantage

- Reconfigurable for a wide range of display types, resolutions and interfaces
- Scalable for common architecture and hardware across mid-to-high-end hybrid/reconfigurable clusters with any number and combination of LCD/TFT displays
- Lower non-recurring engineering (NRE) fees than semi-custom ASSP/ASIC solutions

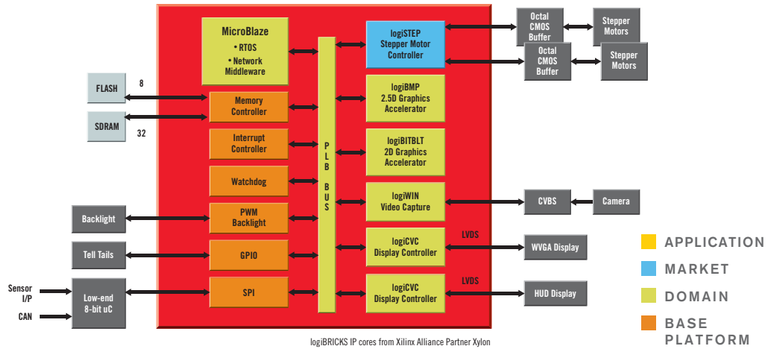
Infotainment and Driver Information Applications:

- Head-Unit
- Rear-Seat Entertainment
- TV Tuner
- Audio/Multimedia Systems
- Game Consoles
- Hybrid Instrument Cluster
- Fully Reconfigurable Instrument Cluster
- Head-up Display

XILINX AUTOMOTIVE TARGETED DESIGN PLATFORM

Hybrid Instrument Cluster

The Xilinx Automotive Targeted Design Platform for hybrid, reconfigurable and head up display (HUD) instrument cluster display applications integrates stepper motor control of analog gauges, graphics control of digital displays, and support for multiple LCD/TFT and HUD displays and camera-based image processing.



logiBRICKS IP cores from Xilinx Alliance Partner Xylon

BASE PLATFORM

logiCRAFT6 Development Board

The Spartan-6 FPGA-based logiCRAFT6 Compact Multimedia Display Development Board provides many of the features required in emerging infotainment and driver information applications. This includes support for a variety of audio/video inputs/outputs, flexible TFT/LCD display interfacing, a high-performance memory configuration for video/graphics applications, and high-speed serial interfaces for remote digital camera or display interfacing. The small package size, automotive-grade power supplies, and vehicle networking support make this an ideal on-bench or in-vehicle prototype platform.

- Available from Xilinx Alliance Partner Xylon

- The logiCRAFT 6 Development Board is part of the base platform of a complete Hybrid Instrument Cluster Targeted Design Platform. The associated fully functional reference design includes stepper motor gauge control, dual TFT displays (including a HUD), and Rear Camera input/display. Image distortion correction is also implemented for both HUD and Rear Camera.

VEHICLE NETWORKING & CONNECTIVITY

The programmable architecture and built-in connectivity of Xilinx FPGAs is ideally suited for automotive infotainment and in-vehicle networking applications, from development through production. The same hardware can be used for multiple car models with different feature offerings and connectivity added or updated as networking standards change over time. The integration of vehicle network connections along with audio/video processing acceleration or graphics subsystems on a single Xilinx device creates an efficient, cost-effective system that works independently or with other application-specific devices.

Today's vehicles would require hundreds of dedicated point-to-point connections for switches, sensors, motors, and controls to handle the myriad of communications possibilities. Xilinx supports multiple in-vehicle networking standards that eliminate the need for bulky, expensive, and complex wiring. XA devices with integrated PCI Express® compliant blocks are especially well-suited for automotive infotainment applications for chip-to-chip communication, either as a complete FPGA-based system on-chip, or as a dedicated companion chip to an ASSP, microcontroller or DSP-based device.

Robust Support for Vehicle Networking Standards

- Media Oriented Systems Transport (MOST®)
- Controller Area Network (CAN)
- Automotive Pixel Link (APIX)
- Ethernet Audio Video Bridging (EAVB)

The Challenges

- Infotainment is part of a fast changing, consumer-driven segment within the automotive market
- Changing networking standards can delay rollout or add costs across multiple platforms
- Limited support for automotive-specific interfacing standards with popular general-purpose microcontrollers and DSP-based processors

The Xilinx Advantage

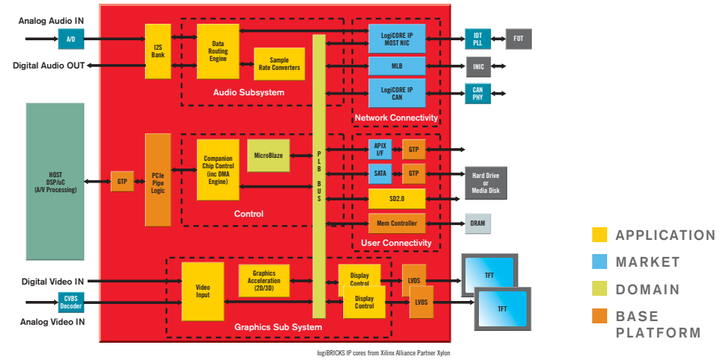
- Ultimate flexibility with programmable interfacing options for different standards
- Scalable device density ensures optimal solution for target application
- Automotive-specific functions with extensive IP support
- Compatibility with standard chip solutions through collaboration with industry consortia and processing platform suppliers

Vehicle Networking and Connectivity Applications:

- MOST
- CAN
- APIX
- PCI Express
- Ethernet AVB
- LVDS
- RSDS
- USB
- SD Card
- I/O Expansion
- I/O Hub

INFOTAINMENT COMPANION CHIP TARGETED DESIGN PLATFORM

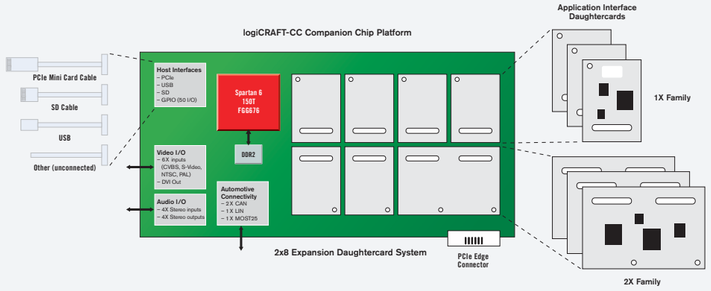
The Xilinx Automotive Infotainment Companion Chip Targeted Design Platform provides flexible interfacing and is optimized to compliment existing or preferred host processors. Available IP and software enables rapid extension of system interfaces, peripherals, or processing with minimal development effort. Various popular host processor interfaces are supported and can be changed quickly based on host availability and overall bandwidth required.



logiBRICKS IP cores from Xilinx Alliance Partner Xylon

BASE PLATFORM

Companion Chip Rapid Prototyping System



The logiCRAFT-CC development board is part of the base platform of the Infotainment Companion Chip Targeted Design Platform. It provides complete host interface flexibility and several popular peripheral interfaces. In addition, eight expansion slots provide for enhanced application specific flexibility and can be used in various combinations. Expansion board layout templates are provided for users wishing to develop their own application specific boards, which enables full prototyping of specific end products.

- logiCRAFT-CC is available from Xilinx Premier Alliance Member Xylon

DEDICATED AUTOMOTIVE PRODUCT LINE

Xilinx Automotive FPGA and CPLD product lines offer automotive-qualified devices in a variety of densities, packages, and extended temperature grades. All devices are pin-compatible with commercial parts for full migration support and tested using a robust qualification process that exceeds AEC-Q100 requirements. Xilinx delivers continuous improvements to ensure world-class quality and reliability.

Delivering platforms that go beyond silicon to address the needs of multiple applications including:

- Infotainment
- Driver Assistance
- Driver Information

XA Spartan-6 FPGA Family

Designed for cost-sensitive applications requiring high-speed connectivity, XA Spartan-6 FPGAs offer an optimal balance of cost, power, and performance with:

- Intelligent mix of logic and hard IP for greater system integration
- Embedded 3.125Gbps low-power serial transceivers, 250MHz DSP slices, hardened memory controllers, and PCI Express interface cores
- XA Spartan-6 LX FPGAs for cost-optimized logic and memory
- XA Spartan-6 LXT FPGAs for high-speed serial connectivity

XA Spartan-3 FPGA Extended Family

- Multiple domain-optimized device families with unique dual power management modes and Device DNA security
- XA Spartan-3A DSP FPGAs for cost-sensitive DSP algorithmic and co-processing applications requiring significant DSP performance with embedded MAC blocks
- XA Spartan-3A FPGAs for lowest cost I/O with up to 1.4M system gates and up to 375 I/Os with support for industry-standard and emerging I/O standards
- XA Spartan-3E FPGAs for lowest cost logic with system gates ranging from 100K to 1.6M gates, and I/Os ranging from 66 to 376 I/Os

XA CoolRunner™-II CPLDs

- High performance and ultra-low power consumption in 0.18-micron non-volatile technology
- Ultra low power of 28.8 µW and 16 µA typical standby
- Multiple device options with densities from 32 to 384 macrocells, multi-voltage I/O operation from 1.5V to 3.3V, and smallest form factor packaging
- Up to 303 MHz performance with less than 100 µA standby current
- 500mV input hysteresis, advanced security, clock management, input gating, and voltage banking capabilities

XA9500XL CPLDs

- Cost-optimized silicon with free design tools and unparalleled support
- Lowest cost per macrocell
- High-performance, nonvolatile programmable logic with 5v, 3.3v and 2.5v I/O interfacing
- Maximum design flexibility with multiple densities, package options and I/O capacities
- Fast in-system programming, second-generation pin locking, and enhanced data security

XA Product Line

		Spartan®-6 LX FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V)							Spartan-6 LXT FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory with High-Speed Serial Connectivity (1.2V)		
	Part Number	XA6SLX4[10,11]	XA6SLX9	XA6SLX16	XA6SLX25[10]	XA6SLX45	XA6SLX75	XA6SLX100	XA6SLX25T[10]	XA6SLX45T	XA6SLX75T
Logic Resources	Slices[1]	600	1,430	2,278	3,758	6,822	11,662	15,822	3,758	6,822	11,662
	Logic Cells[2]	3,840	9,152	14,579	24,051	43,661	74,637	101,261	24,051	43,661	74,637
	CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	30,064	54,576	93,296
Memory Resources	Maximum Distributed RAM (Kb)	75	90	136	229	401	692	976	229	401	692
	Block RAM (18 Kb each)	12	32	32	52	116	172	268	52	116	172
	Total Block RAM (Kb)[3]	216	576	576	936	2,088	3,096	4,824	936	2,088	3,096
Clock Resources	Clock Management Tiles (CMT)[4]	2	2	2	2	4	6	6	2	4	6
I/O Resources	Maximum Single-Ended Pins	132	200	232	266	316	280	326	250	296	268
	Maximum Differential Pairs	66	100	116	133	158	140	163	125	148	134
Embedded Hard IP Resources	DSP48A1 Slices[5]	8	16	32	38	58	132	180	38	58	132
	Endpoint Block for PCI Express®	—	—	—	—	—	—	-	1	1	1
	Memory Controller Blocks	0	2	2	2	2	2	2	2	2	2
	GTP Low-Power Transceivers	—	—	—	—	—	—	-	2	4	4
Miscellaneous	Speed Grade	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2	-2, -3	-2, -3	-2, -3
	Temperature Grade[6]	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q
	XA Released	Q3 2011	Q3 2011	Q3 2011	Q3 2011	Yes	Yes	Q3 2011	Q3 2011	Q3 2011	Yes
Configuration	Configuration Memory (Mb)	2.7	2.7	3.7	6.4	11.9	19.6	26.5	6.4	11.9	19.6
Package	Area										
Chip Scale Packages (CSG): Pb-free wire-bond, chip-scale, BGA (0.8 mm ball spacing)											
CSG225[8]	13 x 13 mm	132	160	160							
CSG324	15 x 15 mm		200	232	226	218			190 (2)	190 (4)	
BGA Packages (FTG): Pb-free wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)											
FTG256	17 x 17 mm		186	186	186						
BGA Packages (FGG): Pb-free wire-bond, fine-pitch, BGA (1.0 mm ball spacing)											
FGG484[9]	23 x 23 mm				266	316	280	326	250 (2)	296 (4)	268 (4)

XMP079 (v2.0)

Notes: 1. Each slice contains four LUTs and eight flip-flops.
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT structure.
3. Block RAM are fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.
6. Temperature Range Automotive I (T_j = –40°C to +100°C); Automotive Q (T_j = –40°C to + 125°C).
7. The LX device pinouts are not compatible with the LXT devices.
8. CSG225 has memory controller support in the LX9 and LX16 devices. There is no memory controller in the XA6SLX4 devices.
9. Devices in the FGG484 have support for two memory controllers.
10. BPI configuration mode not available.
11. SelectMAP configuration modes not available.

Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

INTEGRATED SOFTWARE DESIGN ENVIRONMENT

Get designs done faster and high quality products to market with the proven development and verification tools in the ISE Design Suite. Our award-winning ISE software brings sophisticated FPGA technologies to the automotive design community with domain-specific tool configurations optimized for logic, DSP, embedded processing, and system-level design.

The award-winning ISE Design Suite provides a fully integrated front-to-back design environment tailored for the way engineers work, whether they are developing real-time image processing systems using DSP tools or building sophisticated networking control functions using embedded processors. With seamless interoperability between domain-optimized design configurations and tightly integrated flows, automotive developers can rapidly create and integrate embedded, DSP, IP and custom blocks into a single programmable system-on-chip.

Complex Design Made Logical

- Logic Edition for logic and connectivity designers with the complete FPGA tool flow, base-level IP, and bitstream generation & device programming utilities
- Embedded Edition for embedded systems designers (hardware and software programmers) incorporating one or more processors into their FPGA designs with embedded tools and IP, as well as base-level FPGA tools and IP
- DSP Edition for algorithm, system, and hardware developers with DSP tools and IP, along with base-level FPGA tools and IP
- System Edition for system designers with all the tools, technologies, and IP in the Logic, DSP, and Embedded Editions

ISE DESIGN SUITE

XA Product Line

		Spartan®-3A FPGAs				Spartan-3A DSP FPGAs	
	Part Number	XA3S200A	XA3S400A	XA3S700A	XA3S1400A	XA3SD1800A	XA3SD3400A
Logic Resources	System Gates[1]	200K	400K	700K	1,400K	1,800K	3,400K
	Slices[2]	1,792	3,584	5,888	11,264	16,640	23,872
	Logic Cells	4,032	8,064	12,248	25,344	37,440	53,712
	CLB Flip-Flops	3,584	7,168	11,776	22,528	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kb)	28	56	92	176	260	373
	Block RAM Blocks	16	20	20	32	84	126
	Total Block RAM (Kb)	288	360	360	576	1,512	2,268
Clock Resources	Digital Clock Managers (DCMs) - S3/DLLs - SIIE	4	4	8	8	8	8
I/O Resources	Maximum Single-Ended I/Os	195	311	372	375	519	469
	Maximum Differential I/O Pairs	90	142	165	165	227	213
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, PCI-X 3.3V, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25, LVDS33, LVPECL25, LVPECL33, Mini-LVDS25, Mini-LVDS33, RSDS25, RSDS33, TMDS25, TMDS33, PPDS25, and PPDS33					
Embedded Hard IP Resources	DSP48A Slices	—	—	—	—	84	126
	Dedicated Multipliers	16	20	20	32	84[3]	126[3]
	Device DNA Security	Yes	Yes	Yes	Yes	Yes	Yes
Miscellaneous	Temperature Grades [4]	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q
	Speed Grade	-4	-4	-4	-4	-4	-4
	RoHS (Pb-free)	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released	Yes	Yes	Yes	Yes	Yes	Yes
Configuration	Configuration Memory (Mb)	1.2	1.9	2.7	4.8	8.2	11.7
Package	Area	Maximum User I/Os					
FGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)							
FT256	17 x 17 mm	195	195				
Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)							
CSG484	19 x 19 mm					309	309
FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)							
FGG400	21 x 21 mm		311	311			
FGG484	23 x 23 mm			372	375		
FGG676	27 x 27 mm					519	469

XMP079 (v1.1)

Notes: 1. System gates include 20%–30% of CLBs used as RAMs.
2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).
4. Temperature Range Automotive I (T_j = –40°C to +100°C); Automotive Q (T_j = –40°C to +125°C).

		Spartan®-3 FPGAs					Spartan-3E FPGAs				
	Part Number	XA3S50	XA3S200	XA3S400	XA3S1000	XA3S1500	XA3S100E	XA3S250E	XA3S500E	XA3S1200E	XA3S1600E
Logic Resources	System Gates[1]	50K	200K	400K	1,000K	1,500K	100K	250K	500K	1,200K	1,600K
	Slices[2]	768	1,920	3,584	7,680	13,312	960	2,448	4,656	8,672	14,752
	Logic Cells	1,728	4,320	8,064	17,280	29,952	2,160	5,508	10,476	19,512	33,192
	CLB Flip-Flops	1,536	3,840	7,168	15,360	26,624	1,920	4,896	9,312	17,344	29,504
Memory Resources	Maximum Distributed RAM (Kb)	12	30	56	120	208	15	38	73	136	231
	Block RAM Blocks	4	12	16	24	32	4	12	20	28	36
	Total Block RAM (Kb)	72	216	288	432	576	72	216	360	504	648
Clock Resources	Digital Clock Managers (DCMs) - S3/DLLs - SIIE	2	4	4	4	4	2	4	4	8	8
I/O Resources	Maximum Single-Ended I/Os	124	173	264	333	487	108	172	190	304	376
	Maximum Differential I/O Pairs	56	76	116	149	221	40	68	77	124	156
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, GTL, GTL+, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, Bus LVDS, LDT (ULVDS), LVDS_ext, LVDS25, LVDS33, LVPECL25, and RSDS25					LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL18 Class I, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, PCI-X 3.3V, SSTL2 Class I, SSTL18 Class I, Bus LVDS, LVDS25, LVPECL25, Mini-LVDS25, and RSDS25				
Embedded Hard IP Resources	DSP48A Slices	—	—	—	—	—	—	—	—	—	—
	Dedicated Multipliers	4	12	16	24	32	4	12	20	28	36
	Device DNA Security	—	—	—	—	—	—	—	—	—	—
Miscellaneous	Temperature Grades[4]	I, Q	I, Q	I, Q	I, Q	I	I, Q	I, Q	I, Q	I, Q	I, Q
	Speed Grade	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4
	RoHS (Pb-free)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Configuration	Configuration Memory (Mb)	0.4	1	1.7	3.2	5.2	0.6	1.4	2.3	3.8	6
Package	Area	Maximum User I/Os									
VQFP Packages (VQ): Very thin, QFP (0.5 mm lead spacing)											
VQ100	16 x 16 mm	63	63				66	66			
Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)											
CP132	8 x 8 mm						83	92	92		
TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)											
TQ144[5]	22 x 22 mm		97				108	108			
PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing)											
PQ208	30.6 x 30.6 mm	124	141	141				158	158		
FGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)											
FT256	17 x 17 mm		173	173	173			172	190	190	
FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)											
FG400	19 x 19 mm									304	304
FG456	21 x 21 mm			264	333	333					
FGG494	23 x 23 mm										376
FGG676	27 x 27 mm					487					

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Notes: 1. System gates include 20%–30% of CLBs used as RAMs.
2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).
4. Temperature Range Automotive I (T_j = -40°C to +100°C); Automotive Q (T_j = -40°C to +125°C).

			XA9500XL Family			CoolRunner™-II Family				
	Part Number		XA9536XL	XA9572XL	XA95144XL	XA2C32A	XA2C64A	XA2C128	XA2C256	XA2C384
Logic Resources	System Gates		800	1,600	3,200	750	1,500	3,000	6,000	9,000
	Macrocells		36	72	144	32	64	128	256	384
	Product Terms Per Macrocell		90	90	90	56	56	56	56	56
Clock Resources	Global Clocks		3	3	3	3	3	3	3	3
	Product Term Clocks Per Function Block		18	18	18	16	16	16	16	16
I/O Resources	Maximum I/O		34	72	117	33	64	100	118	118
	Input Voltage Compatible (V)		2.5/3.3/5	2.5/3.3/5	2.5/3.3/5	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
	Output Voltage Compatible (V)		2.5/3.3	2.5/3.3	2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
Speed Grades	Minimum Pin-to-Pin Logic Delay		15.5	15.5	15.5	5.5	6.7	7	7	9.2
	Automotive I Speed Grades		-15	-15	-15	-6	-7	-7	-7	-10
	Automotive Q Speed Grades		-15	-15	-15	-7	-8	-8	-8	-11
Miscellaneous	Temperature Grades[1]		I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q
	RoHS (Pb-free)		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Package	Area[2]	Maximum User I/Os							
	VQFP Packages (VQ): Very thin QFP (VQG44: 0.8 mm lead spacing; VQG64 and VQG100: 0.5 mm lead spacing)									
	VQG44	12 x 12 mm	34	34		33	33			
	VQG64	12 x 12 mm		52						
	VQG100	16 x 16 mm					64	80	80	
	TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)									
	TQG100	16 x 16 mm		72						
	TQG144	22 x 22 mm							118	118
	Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)									
	CPG132	8 x 8 mm						100		
	Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)									
	CSG144	12 x 12 mm			117					

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Notes: 1. Temperature Grade XA CPLD Automotive I (T_A = –40°C to +85°C); Automotive Q (T_A = –40°C to +105°C with $T_{J\ MAXIMUM}$ = +125°C).
2. Area dimensions for lead-frame products are inclusive of the leads.

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Printed in the U.S.A. PN 2444-1