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RT Kintex UltraScale FPGAs for Ultra High Throughput and High Bandwidth Applications

The Xilinx® Radiation Tolerant (RT) Kintex® UltraScale™ XQRKU060 FPGA enables the next generation of high-throughput satellite services, allowing OEMs to offer re-configurable payloads with unprecedented levels of on-board processing across all radiation orbits.

ABSTRACT

Xilinx's UltraScale architecture extends FPGA capability for space applications, delivering a step-function increase in I/O and memory bandwidth, capacity, performance, and in-orbit re-configurability. For the first time, the RT Kintex UltraScale XQRKU060 FPGA enables the satellite industry to access ultra high-throughput on-board processing of hundreds of Gb/s. This capability allows spacecraft operators to offer new applications such as real-time streaming of Earth-Observation remote sensing in super high-resolution, space-based Internet, and broadband mobile telecommunication with the ability to optimize and re-deploy in-orbit payload resources in response to real-time user needs.

Space-grade FPGAs from other vendors suffer from architectural bottlenecks severely limiting their use for ultra high-throughput on-board processing. Xilinx's RT Kintex UltraScale fabric has innovative on-chip communication, I/O and memory bandwidth, DSP capability, clocking, critical paths, and interconnect, using 20nm technology to deliver best-in-class, ASIC-level system performance for the most demanding of satellite applications.

Market Challenges & Trends

Starting from 2020, it is predicted that almost 1,000 satellites will be launched every year for the next decade to provide telecommunication, television-broadcasting, Earth-observation remote sensing, space-based Internet, and navigation services.

The demand for high-throughput services is growing 26% annually and is forecast to reach 8,000 Gb/s by 2028, generating $15 billion in revenue from a diverse range of applications in geosynchronous equatorial orbit (GEO) and non-GEO orbits.

The majority of the satellites will be launched on behalf of Space 2.0 operators planning constellations of small spacecraft targeting the lucrative space-based Internet and Earth-Observation data-analytics markets. Typically, these reside in LEO for three to five years and are constrained by power consumption and cost. Space 2.0 operators are becoming more ambitious, starting to diversify and challenge traditional providers by offering competing services in other orbits.

The defense industry is also exploiting cheaper smaller satellites and lower launch costs, and is planning constellations in all orbits to provide the military with high-throughput, low-latency communication.

To deliver higher performance and added value over competitors, traditional and Space 2.0 operators are seeking ultra high-throughput payloads to deliver the next generation of satellite services.

On-Board Processing Limitations of Existing Space-Grade FPGAs

To address real-time, high-throughput system performance needs in the range of hundreds of Gb/s, a new architectural approach to programmable logic is required. Regardless of whether the application is a telecommunication satellite with a broadband digital payload, an Earth-Observation spacecraft streaming live remote-sensing data, or a Martian rover beaming back images in super high-resolution, a large amount of information needs to be processed.

The problem of moving vast quantities of information through a system is illustrated in Figure 1: data streams on the order of hundreds of Gb/s enter and exit from the left and right using I/O banks and/or high-speed serial transceivers. Future payloads are required to process these in real-time and as soon as the data enters the FPGA, it must fan out to match the data flow, routing, and processing capabilities of the on-chip resources.

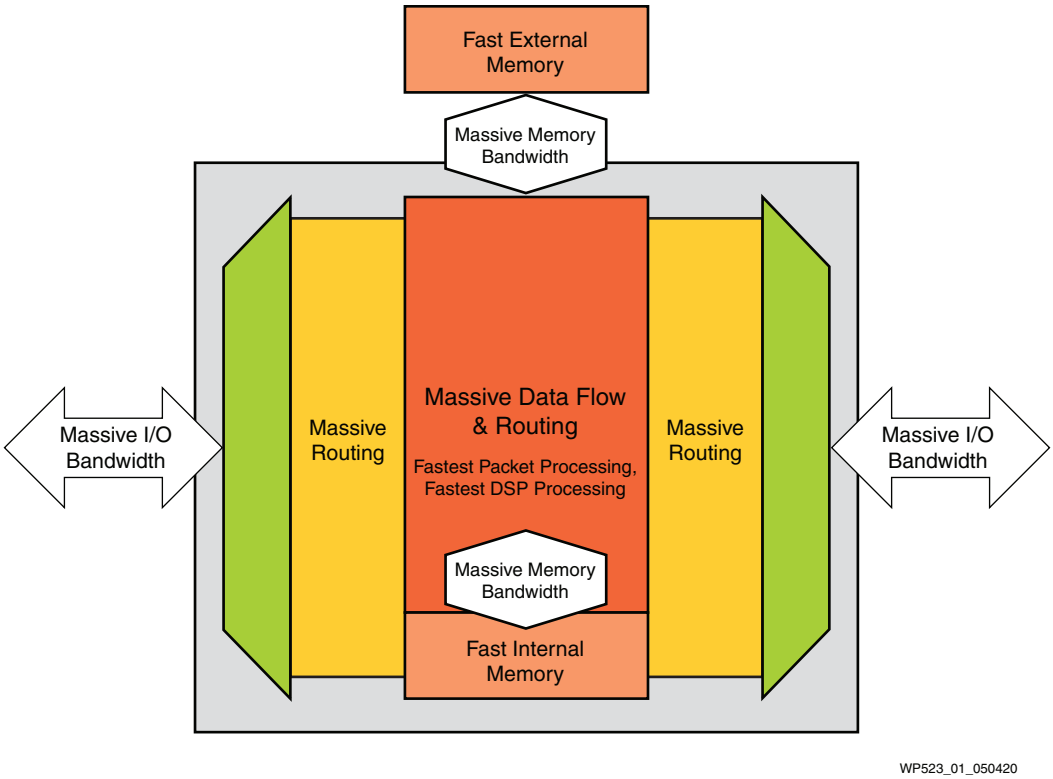

Figure 1: **High-Performance Systems Require Massive Bandwidth**

As an example, assume the I/O bandwidth for the ports on the left and right is 400Gb/s. This means that the FPGA's logic, arithmetic, and memory resources must also process at least 400Gb/s traffic. Design engineers typically use a wide bus ranging in size from 512 to 2,048 bits to manage this throughput.

Designs with narrow datapaths operating at high frequencies often suffer from performance-compromising clock skew, which in extreme cases can approach 50% of the total clock period. This leaves little time to perform actual computation, leading designers to heavily pipeline their designs. Beyond consuming large amounts of register resources, extensive pipelining has a significant impact on overall system latency, which is unacceptable in today's high-performance systems.

While a wider bus implementation might lead to the need for a lower system clock frequency, significant timing-closure challenges now arise due to a lack of routing resources required to support large buses. The situation is further aggravated by the fact that some FPGA vendors use antiquated place-and-route algorithms based on simulated annealing, which are blind to global design metrics, such as the level of congestion or the total wire length. Thus, designers are forced to consider trade-offs that require lowering the performance of the system (typically not an option), extensive pipelining at the expense of latency, or gross underutilization of the available device resources. In all cases, these solutions prove to be inferior or inadequate.

The fundamental limitation in routing resources required to address applications on the order of hundreds of Gb/s exists with all current space-grade FPGAs. This all but guarantees that addressing the next generation of ultra high-throughput satellite applications will be out of the realm of possibility, or will come at the expense of very poor device utilization or latency.

The challenge is how to reliably manage huge dataflows: the incoming high-speed information needs to be fanned-out and routed with low clock skew to processing logic, and to handle the large data rates, computed in real-time by massively-wide functional blocks, e.g., high-throughput arithmetic or DSP. Incoming data or intermediate results must be stored quickly within the system, close to the processing elements, or in fast, external bulk memory located next to the payload using interfaces with huge memory bandwidths. After processing, the data must be routed to I/O banks or the high-speed output transceivers to be passed along as illustrated in Figure 1.

As designs become more complex with wider internal data buses and more physical signals to process, (often brought on-chip by the dramatically increasing number of high-speed serial transceivers), three major challenges become clear:

1. Routing dominates overall delay in the system
2. Clock skew consumes a greater proportion of the available timing margin
3. Sub-optimal logic placement reduces system performance

RT Kintex UltraScale FPGA for Space Applications

Xilinx's RT Kintex UltraScale FPGA is designed to address next-generation system-level performance requirements associated with applications such as high-throughput, massive-bandwidth satellites. Many innovations and enhancements went into developing the new fabric to solve all of these issues.

To efficiently receive, buffer, process, and transmit the vast amounts of data required by the next generation of ultra high-throughput satellite payloads, Xilinx's UltraScale FPGA fabric fundamentally improves on-chip communication, I/O and memory bandwidth, DSP capability, clocking, critical path optimization, and interconnect to address massive data flow and real-time packet and image processing. Innovations include:

- Massive data flow optimized for wide buses supporting hundreds of Gb/s throughput with low latency
- Highly optimized critical paths and built-in high-speed memory, cascading to remove bottlenecks in DSP and packet processing
- Enhanced DSP slices, incorporating 27x18-bit multipliers and dual adders that enable a massive jump in fixed-point and IEEE Std 754 floating-point arithmetic performance and efficiency
- Massive I/O and memory bandwidth, including support for DDR3 and DDR4 interfacing with dramatic reduction in latency
- Multi-region ASIC-like clocking, delivering low-power clock networks with extremely low clock skew and high-performance scalability
- Power management with significant static- and dynamic-power gating across a wide range of functional elements, yielding significant power savings
- Massive routing capacity while intelligently resolving typical bottlenecks in ways never before possible. This significantly mitigates routing congestion, allowing for greater utilization with little or no performance degradation.

- Latency-producing pipelining is virtually unnecessary in systems with massively parallel bus architectures, increasing system speed and capability
- Potential timing-closure problems and interconnect bottlenecks are eliminated, even in systems requiring 90% or more resource utilization
- Next-generation security with advanced approaches to AES bitstream decryption and authentication, key-obfuscation, and secure device programming

These enhancements synergistically combine to enable design teams to create systems that have greater functionality, run faster, and deliver greater performance per watt than ever before.

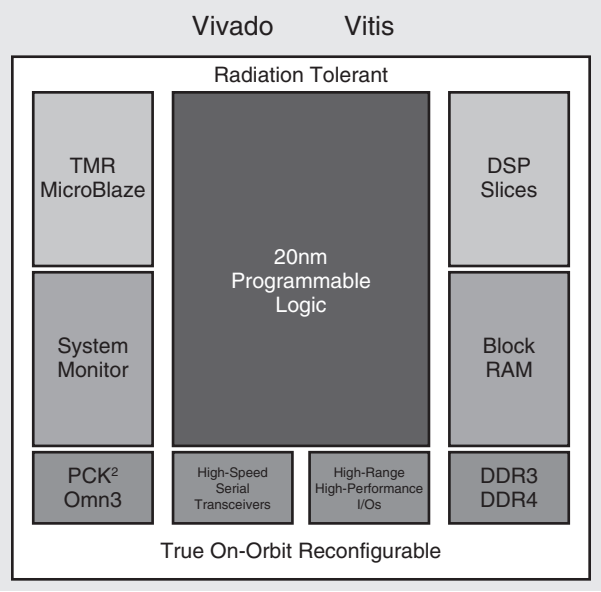

Figure 2: **RT Kintex UltraScale Platform Block Diagram**

Next-Generation Routing for Utilization, Performance, and Run Time

With conventional FPGA architectures, logical resources are laid out in a matrix with rows and columns of interconnect. As FPGA device density increases into the multi-million logic cell capacity (multi-tens-of-millions of equivalent ASIC gates), the disparity between the logic (increasing by a factor of N^2) and the number of interconnect tracks (increasing by a factor of N), becomes a limiting factor in successfully routing a design at the required system performance level.

The UltraScale architecture addresses this challenge by increasing the interconnect track count in all devices, providing more direct routes from A to B and giving the software tools more options to connect logic resources in the fastest, lowest-power configuration.

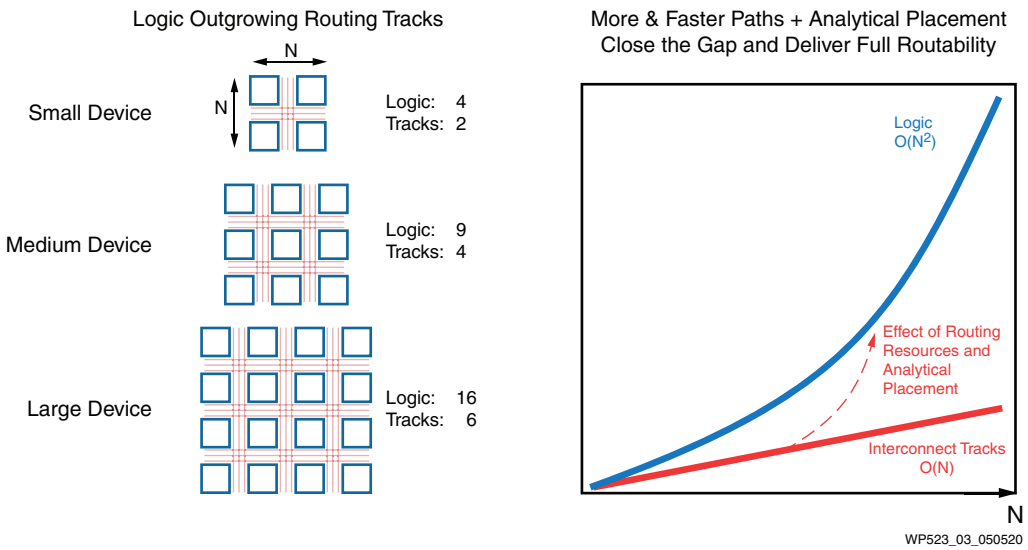

Figure 3: **Adding Routing in the UltraScale Architecture**

ASIC-Like Clocking Maximizes Performance

FPGA architectures prior to the UltraScale architecture relied on a fan-out of a geometrically-centered clocking scheme with global resources in the middle of the device. These were fanned out to the extremities of the FPGA, which accumulates skew. With increasing capacity and system performance, chip-wide, clock skew can have a detrimental impact on the overall timing budget of a design.

The clock routing and buffers within the UltraScale architecture have been entirely redesigned to provide vastly more flexibility than competing FPGA fabrics. With an abundance of clock routing and distribution tracks in both the horizontal and vertical direction, the UltraScale architecture provides 20X the number of global clock buffers than previous generations. In essence, the center of the clock network, i.e., from where skew starts to accumulate, can be placed in any clock region within the FPGA. This enables clock networks to only span where they are needed, consuming only the power needed to get clock signals from their source to all their destinations just like an ASIC.

From the system designer's perspective, the placement of a large number of independent, high-performance clock sources eliminates the skew problem. This removes the need for extensive pipelining and the associated latency that comes with it. See Figure 4.

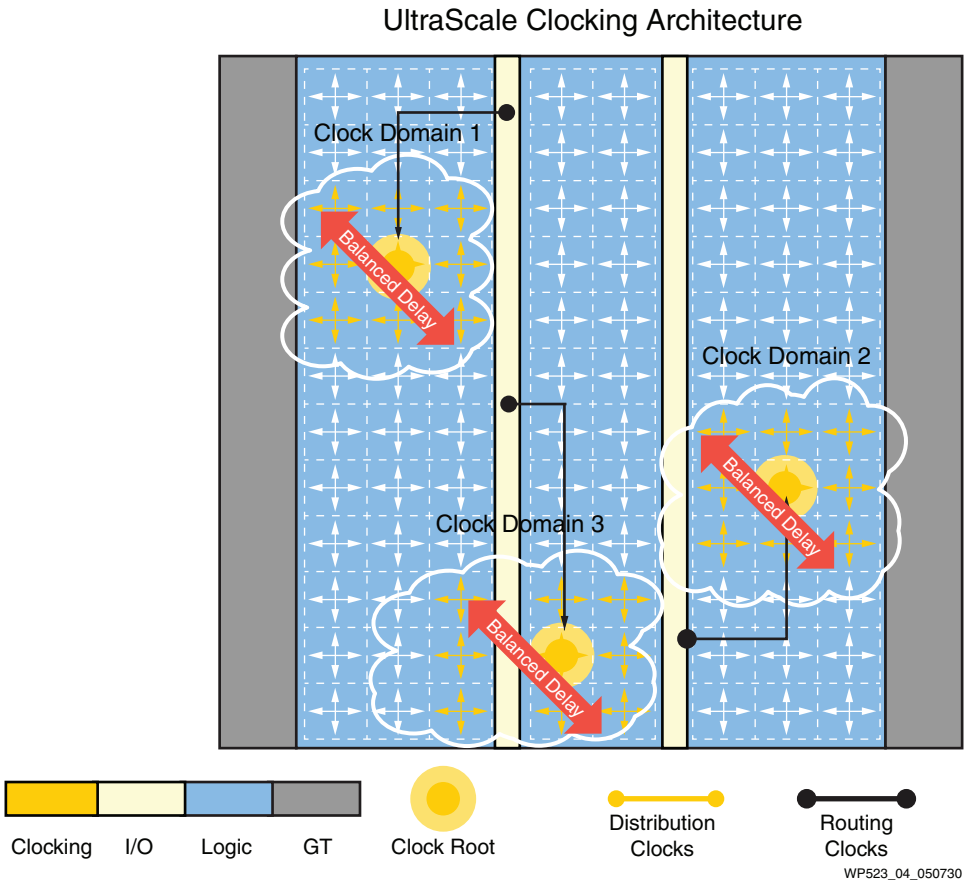

Figure 4: **UltraScale Clocking Architecture**

Designs Use Fewer CLBs Resulting in Shorter Wire Length

After the clock and data signals arrive at the logic resources, the UltraScale architecture provides an enhanced CLB to make the most efficient use of its available resources, with the goal of reducing interconnect, i.e., the total wire length. Every aspect of the existing CLB structure was analyzed to explore how its components can be used more efficiently. The resulting enhancements collectively enable the Vivado® Design Suite to place many more, often unrelated, components in a CLB to achieve tighter placement. Operating at high performance, such designs consume the lowest possible power by achieving the best overall device utilization.

Numerous changes within the CLB structure have added flexibility to the possible packing options: every 6-input LUT is combined with two flip-flops with each having dedicated inputs and outputs, enabling all the components to be used together or completely independent of one another. The flip-flops benefit from the increased quantity and flexibility of their control signals, with double the number of available clock-enable signals, optional "ignore" on the clock enable and reset ports, reset inversion allowing both active-High and active-Low reset flip-flops in the same CLB, and an additional clock signal for shift registers and distributed-RAM functions.

Together with the UltraScale architecture's improvement in routing resources and a highly flexible clocking architecture, the dramatic increase in CLB connectivity enables high-performance designs

that are tightly packed together, improving FPGA utilization and lowering total device power. See Figure 5.

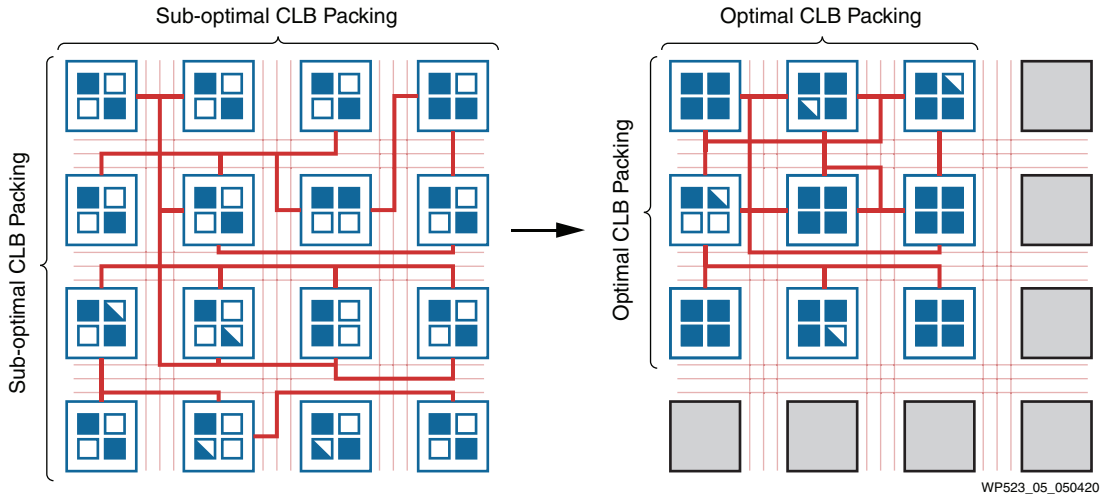

Figure 5: **Efficient Placement of Logic Resources**

Vivado Design Suite

The RT Kintex UltraScale XQRKU060 FPGA implements IP using the Vivado® Design Suite, which has been developed to optimize the physical realization of large, Tb/s, low-latency, ultra high-throughput I/O, wide bus, massive memory-bandwidth applications. Competing place and routing tools use simulated-annealing algorithms, which do not scale for million-LUT designs nor account for total wire length or congestion. The Vivado Design Suite uses analytical place and route technology to find a routable solution at device utilizations of greater than 90% without impacting performance.

The Vivado Design Suite was created specifically to analyze designs to determine where bottlenecks and problems can occur and solve these issues before they arise. By packing logic close together, the wire length between elements is reduced, resulting in shorter routing delays and lower power consumption. Additionally, the clock signals driving these closer elements have less distance to travel to span the design, yielding less clock skew. The Vivado Design Suite provides higher device utilization and improves user productivity.

The XQRKU060 is supported in Vivado Design Suite 2019.1 (or later), which is capable of programming the FPGA and also storing device configuration in supported, external nonvolatile memories.

Xilinx's XQRKU060 UltraScale Radiation-Tolerant FPGA

Compared to previous space-grade FPGAs from Xilinx, the RT Kintex UltraScale XQRKU060 FPGA offers a major increase in processing resources. For the first time, the space industry can exploit the advantages of 20nm fabrication and implement logic optimized for the highest on-board performance together with low power consumption. See Table 1.

Table 1: **Comparison of Xilinx Space-Grade FPGAs**

	Virtex-4QV XQRV4QV	Virtex-5QV XQRV5QV	RT Kintex UltraScale XQRKU060
Radiation Hardness	Tolerant	Hard	Tolerant
Process (nm)	90	65	20
Memory (Mb)	4.1 to 9.9	12.3	38
System Logic Cells (K)	55 to 200	131	726
CLB Flip-Flops (K)	49.1 to 178.1	81.9	663
CLB LUTs (K)	49.1 to 178.1	81.9	331
Transceivers	None	18 at 3.125Gb/s	32 at 12.5Gb/s
User I/O	640 to 960	836	620
DSP Slices	32 to 192	320	2,760

In comparison with previous generation 65nm FPGAs, the XQRKU060 has a reduced power budget of 70%, while delivering a 12X increase in transceiver capability and 5X increase in logic cells. This decrease in dynamic and static power dissipation is achieved by applying power reduction strategies at every level.

Radiation-Effects Mitigation and Hardness

CMOS scaling of planar transistor technology has intrinsically made the XQRKU060 FPGA less susceptible to total-dose and latch-up effects. The layout of the configuration memory cells has been optimized using SEU design rules to protect against multiple-bit upsets together with the use of innovative circuit techniques to reduce soft-error rates. Users can triplicate logic and add EDAC to the FPGA's memory to bolster overall radiation hardness, manually or automatically, using industry-standard tools from Mentor Graphics or Synopsys. Xilinx's SEM IP offers further mitigation and can be used to detect, correct, and classify SEUs in configuration memory. For upsets, the SEM IP uses the Readback CRC feature to locate and correct errors. For SEU classification, the SEM IP uses Xilinx's Essential Bits technology to further increase system availability allowing users to manage a system-level response to reduce downtime.

Scrubbing can also be used to improve reliability, ranging from periodic device re-configuration during each orbit for LEO spacecraft to transparently checking and re-writing individual frames in the background throughout FPGA operation for GEO missions. Xilinx is providing an external RTL solution to configure the XQRKU060 FPGA, scrub the device to prevent the accumulation of SEUs, as well as detect and correct upsets. See Figure 6.

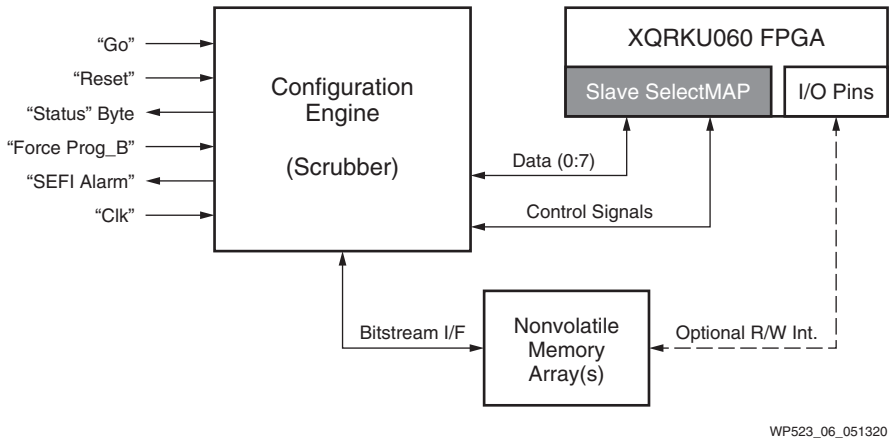

Figure 6: **External Scrubber**

The first phase of static and dynamic heavy-ion testing has been completed on the most critical blocks identified by users and no destructive SEEs were observed. Further testing on the remaining blocks is planned and the latest results will be posted on Xilinx's Space Lounge: https://www.xilinx.com/member/space.html.

Total-dose, SEL, and SEU responses have been measured from a 1MeV Co60 gamma, proton, and heavy-ion sources. No latch-up was observed up to 80MeV-cm2/mg at 125°C with elevated supply voltages. This includes the high-range I/Os up to 3.3V. Competing, ultra deep-submicron, flash-based space-grade FPGAs are known to have increased SEL sensitivity for 2.5 and 3.3V I/O.

Further testing presented at RADECS 2019 reported a total dose tolerance of 120 krad(Si). These results show a maximum of 7% increase in fabric core leakage and <2% for the block RAM, GTM transceiver, I/O, and DSP blocks. The maximum propagation delay is <1% with all devices passing parametric AC and functionality tests within one week of annealing under bias conditions at room temperature. SEL and SEU data from heavy-ion and proton testing of the configuration memory and block RAM were also presented.

Using the CREME96 Solar Minimum Model with 100mils of aluminum shielding, the calculated CRAM sensitivity is 2.4E-7 upsets/bit/day for LEO and 1E-8 upsets/bit/day for GEO. The estimated block RAM sensitivity is 4.7E-7 upsets/bit/day for LEO and 2E-8 upsets/bit /day for GEO.

The results presented at RADECS 2019 reported that the use of Xilinx's SEM IP improved reliability and availability by 3X. This resource occupies approximately 4% of the XQRKU060 FPGA's total configuration memory.

Heavy-ion and total-dose test reports, together with all other relevant documents related to the XQRKU060, can be downloaded from Xilinx's Space Lounge.

In-Orbit Re-Configurability

The XQRKU060 is an SRAM-based FPGA allowing it to be re-programmed during hardware development in the lab and in-orbit after launch. Competing space-grade, anti-fuse FPGAs can only be configured once, which makes prototyping impossible and timing verification difficult and costly.

There are no limitations on the number of times the XQRKU060 FPGA can be re-configured in-orbit, while competing flash-based FPGAs do have constraints. The functionality of competing 90nm and 45nm space-grade ASICs are fixed and cannot be re-programmed at all!

The ability to re-configure the XQRKU060 FPGA in-orbit offers operators maximum flexibility, allowing new and better communications standards to be uploaded to improve system performance, enabling multiple experiments to be prototyped from a single payload for technology demonstrator satellites, and allowing missions to be launched early with the knowledge that the FPGA firmware can be deployed when needed. On-board re-programming reduces the size of the payload hardware, enabling the use of various algorithms to improve applications, system security, and fault tolerance.

The XQRKU060 FPGA's configuration bank supports multiple memory interfaces as well as various serial and parallel modes. An alternative option to in-orbit re-configuration is to use a large nonvolatile memory capable of storing multiple bitsteams. Other methods include the use of an on-board computer to locally control the SelectMap and JTAG ports in slave mode or uploading new functionality via the TT&C carrier or the main uplink.

In-orbit re-programming can also occur dynamically in real-time while the XQRKU060 FPGA is in use, e.g., partial re-configuration allows the modification of a specific active region implemented within the FPGA without comprising the integrity of the applications running elsewhere within the device that use the imported logic. Re-configurable modules can be swapped in and out from a single FPGA as needed using the ICAP or SelectMAP. See Figure 7.

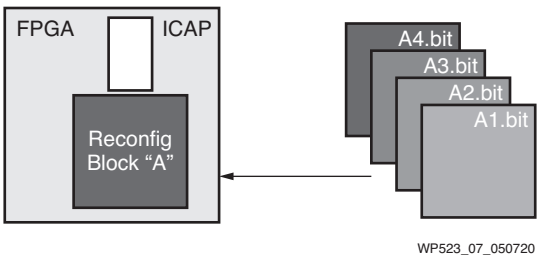

Figure 7: **Partial Re-Configuration of Specific User Logic Blocks**

Device Availability and Qualification

The XQRKU060 FPGAs are designed for Xilinx Class B (QMLB compliant) and Xilinx Class Y (QMLY equivalent) qualification and DLA certification. All reliability grades have a -1M speed rating, a specified temperature range from –55°C to +125°C, and an export status of ECCN 9A515.e.1.

Package

Both the plastic industrial (XCKU060) and the ceramic radiation-tolerant (XQRKU060) versions of the FPGA can be designed-in to have the same PCB footprint. For the latter, 40 x 40mm 1509-pin CGA or LGA packages are available for both qualification flows, compatible with the commercial A1517 pin-out.

Daisy-chain packages are available to assist with reliability and environmental testing.

Fault-Tolerant CPU

To complement the XQRKU060 FPGA, Xilinx also offers its MicroBlaze™ processor technology, fault-tolerant, fail-safe, 32-bit RISC CPU, which can be instantiated within the FPGA. This soft IP achieves a performance above 300MHz, requires approximately 7,400 LUTs and 6,400 flip-flops, and has been implemented using a TMR scheme as shown in Figure 8:

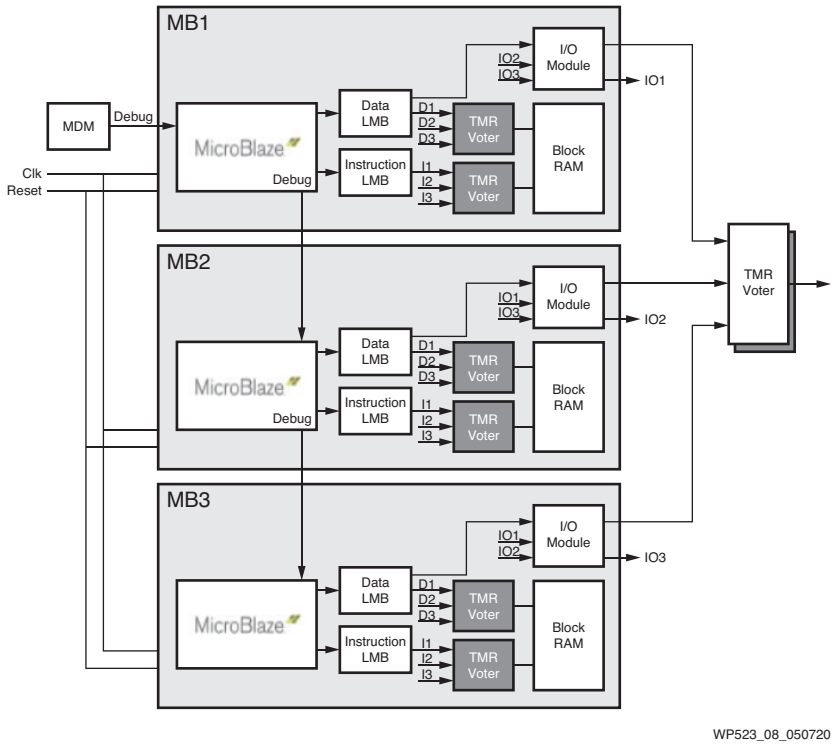

Figure 8: **Fault-Tolerant, Fail-Safe, TMR MicroBlaze Processor Block Diagram**

Flexible, Digital-Beamforming Telecommunication Satellites

Operators of telecommunication satellites want to offer their mobile customers flexible data and broadcast communication anywhere in the world, anytime, adaptable to real-time user needs and changing traffic requirements. Rapidly changing global events and needs, such as the continuous monitoring of aircraft, place live, daily, or seasonal demands on communication, e.g., the coverage, shape, size, and power of the signals transmitted by satellites, and the bandwidth and capacity of channels contained with these.

Telecommunication satellites are increasingly using phased-array antennas and digital beamforming techniques to combine multiple individual antenna elements to improve overall performance, increase gain, cancel out interference, and steer the array so it is most sensitive in a particular direction. This allows operators to change and optimize reception and transmission in response to changing link requirements in real-time. Flexible payloads allow operators to change and adapt frequency plans and channelization bandwidths and offer a 'communication exchange in the sky,' routing uplinks to specific downlinks.

Regenerative payloads demodulate on-board recovering the uplink losses, improving overall system performance and reducing the size of the downlink antenna.

The on-board processing capability of the XQRKU060 FPGA allows satellite manufacturers to offer operators flexible payloads with digital beamforming. Furthermore, because the FPGA is re-configurable, re-generative DSP slices can adapt to different carrier and de-modulation standards. A block diagram of a multi-channel, high-throughput telecommunication payload exploiting the on-board processing capacity of the XQRKU060 FPGA is in Figure 9:

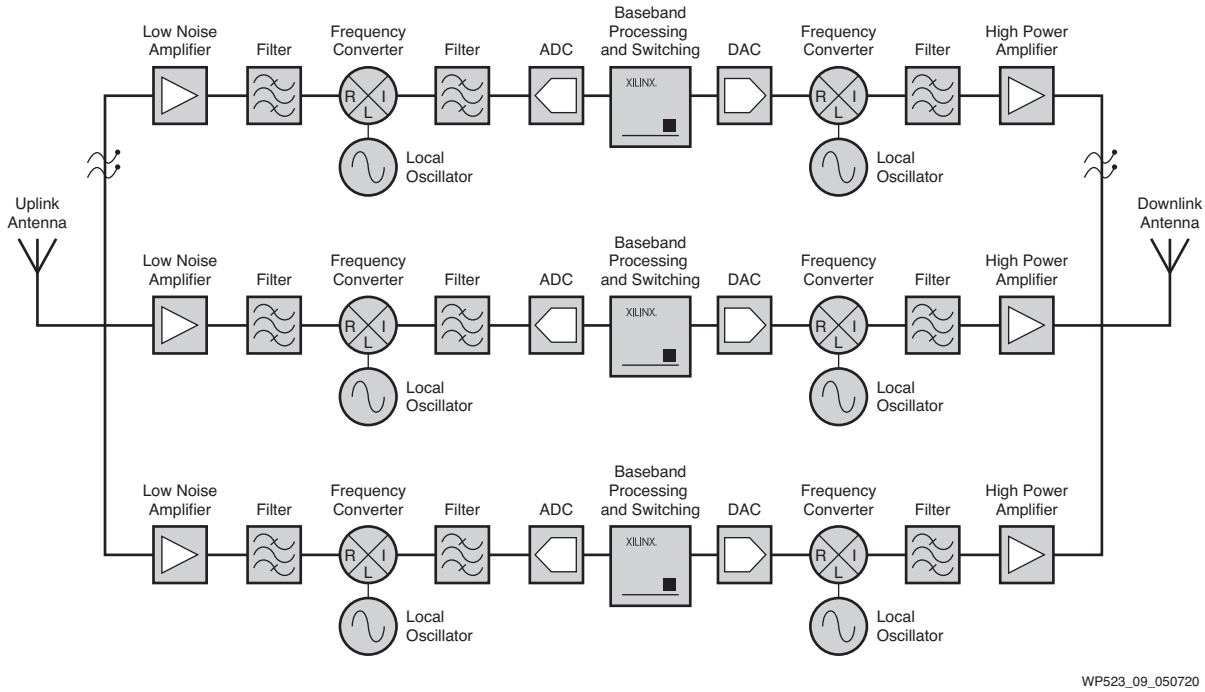

Figure 9: **Block Diagram of a High-Throughput Telecommunication Payload**

Real-Time Streaming of Earth-Observation, Remote-Sensing Video

To deliver added value over competitors, owners of Earth-Observation satellites want to be able to offer their customers real-time 4K UHD and 8K super high-resolution streaming video to enable novel remote-sensing applications. Traditional and Space 2.0 commercial operators are targeting the lucrative data analytics market and need to offer users enabling services such as:

- High-resolution, streaming video SAR and LIDAR
- On-board processing to detect and identify moving targets in real-time
- Calculation of the moving targets' velocities
- Advanced tracking, intelligence, surveillance, and reconnaissance

Developing countries want to exploit the benefits of very high spatial and spectral resolution contiguous-band imaging in the visible, near-infrared, and short-wave infrared bands to address societal needs. High re-visit rates and high-throughput optical efficiency with real-time live streaming is desired to maximize SNR to allow environmental monitoring when solar illumination is low and/or to distinguish specific spectral wavelengths, e.g., over-water remote sensing. Xilinx's XQRKU060 FPGA offers huge I/O and memory bandwidths together with the on-board processing capability to enable future Earth-Observation applications. See Figure 10.

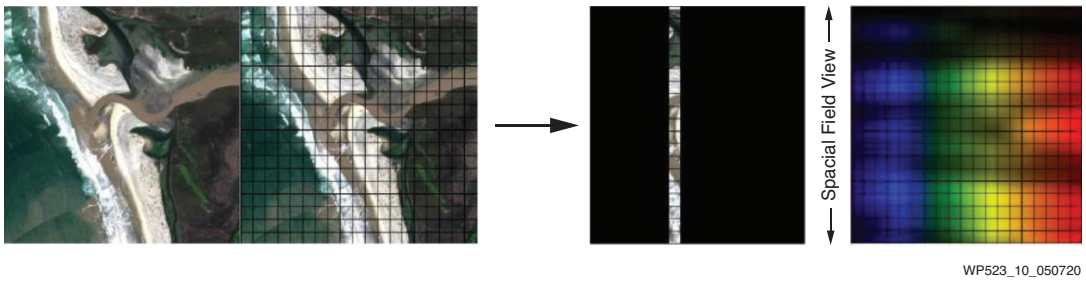

Figure 10: **Hyperspectral Earth-Observation Imaging**

A block diagram of a high-throughput Earth-Observation payload exploiting the on-board processing capability of the XQRKU060 FPGA is illustrated in Figure 11:

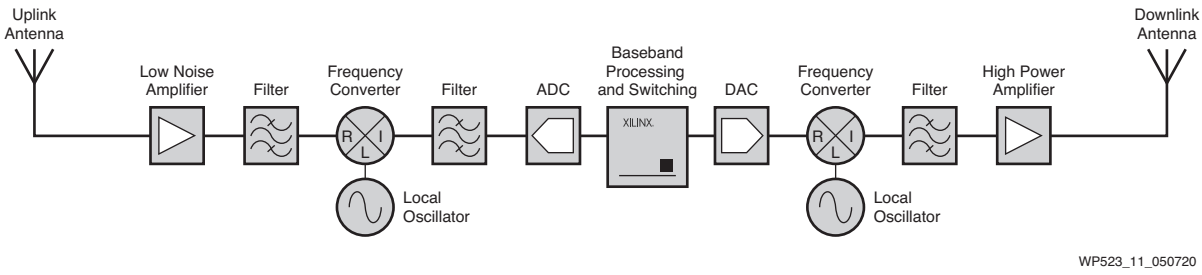

Figure 11: **Block Diagram of a High-Throughput Earth-Observation Payload**

On-Board AI for Autonomous Space Exploration

Agencies operating robotic landers and rovers want to deliver a new experience, increase public engagement, and deliver 'live science.' Future space exploration will require significantly more on-board processing to stream images back to Earth in super high-resolution.

The distance to other planets introduces a significant communication delay. Consequently, the efficient operation of a robot system requires a high level of autonomy. Landers and rovers have to manage local environmental conditions, and future robots will use AI to explore, map, and navigate terrain to avoid hazards, pick-up objects, and collect and analyze samples. All of these activities will be streamed 'live' to Earth.

Future robotic subsystems will require a significant increase in image processing, autonomous navigation, reading telemetry data from sensors, and controlling actuators. All of this information will have to be processed in real-time to enable remote space exploration. In the future, students at schools will be able to directly command rovers to experience 'live science.'

Xilinx's Virtex-4QV FPGA was used by NASA's 'Spirit' and 'Opportunity' rovers to explore the Martian surface and the V5QV space-grade device will be used for off-line processing on the MARS2020 mission. See Figure 12.

Xilinx's XQRKU060 FPGA offers huge I/O and memory bandwidth together with the on-board processing capability to enable the next generation of remote and autonomous space exploration.

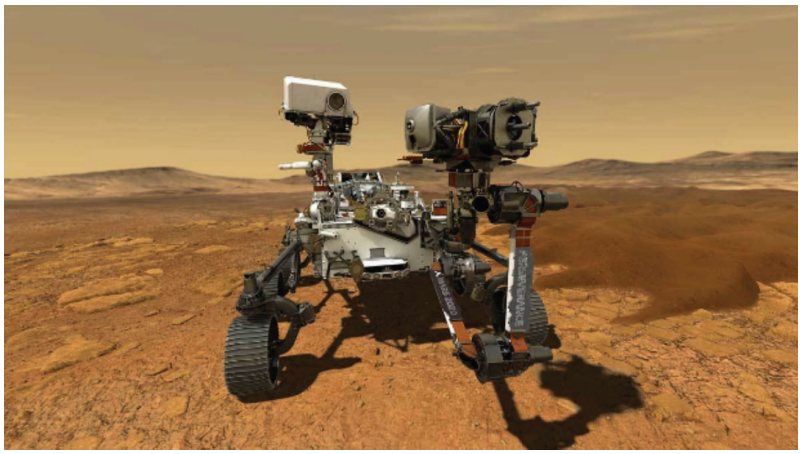

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Figure 12: **Future Martian Rover (Source: NASA)**

Conclusion

Xilinx's UltraScale architecture extends FPGA capability for space applications, delivering a step-function increase in I/O bandwidth, capacity, performance, and in-orbit re-configurability. For the first time, the RT Kintex UltraScale XQRKU060 FPGA enables the satellite industry to access hundreds of Gb/s of ultra high-throughput on-board processing. This capability allows spacecraft operators to offer new applications such as real-time streaming of Earth-Observation remote sensing in super high-resolution, space-based internet, satellite M2M, and broadband mobile telecommunication with the ability to optimize and re-deploy in-orbit payload resources in response to real-time user needs.

Previous and competing space-grade FPGAs suffer from architectural bottlenecks, severely limiting their use for ultra high-throughput on-board processing. Xilinx's RT Kintex UltraScale FPGA fabric has innovative on-chip communication, I/O and memory bandwidth, DSP capability, clocking, critical paths and interconnect, using 20nm technology to deliver best-in-class, ASIC-level system performance for the most demanding of space missions.

Radiation testing has confirmed that the XQRKU060 FPGA is suitable for all orbits as well as deep space exploration. Prototyping, QMLB, and QMLY-grade parts can be procured with the -1M speed and temperature rating and an export status of ECCN 9A515.e.1.

Xilinx's RT Kintex UltraScale XQRKU060 FPGA, radiation-tolerant FPGA delivers a 'giant leap' for on-board reconfigurable processing, enabling many novel, massive-bandwidth satellite applications to deliver the new Space Age!

More Information

Visit the RT Kintex UltraScale FPGA product page at: https://www.xilinx.com/products/silicon-devices/fpga/rt-kintex-ultrascale.html

Acknowledgment

We would like to thank Dr. Rajan Bedi for his collaboration on this white paper. Dr. Bedi is the CEO and founder of Spacechips, which designs and builds a range of advanced, award-winning, L to Ku-band, ultra high-throughput on-board processors and transponders for telecommunication, Earth-Observation, navigation, internet, and M2M/IoT satellites. (www.spacechipsllc.com)

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/19/2020	1.0	Initial Xilinx release.

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