

Vivado Tutorial

Introduction

This tutorial guides you through the design flow using Xilinx Vivado software to create a simple digital circuit using Verilog HDL. A typical design flow consists of creating model(s), creating user constraint file(s), creating a Vivado project, importing the created models, assigning created constraint file(s), optionally running behavioral simulation, synthesizing the design, implementing the design, generating the bitstream, and finally verifying the functionality in the hardware by downloading the generated bitstream file. You will go through the typical design flow targeting the Artix-100 based Nexys4 board. The typical design flow is shown below. The circled number indicates the corresponding step in this tutorial.

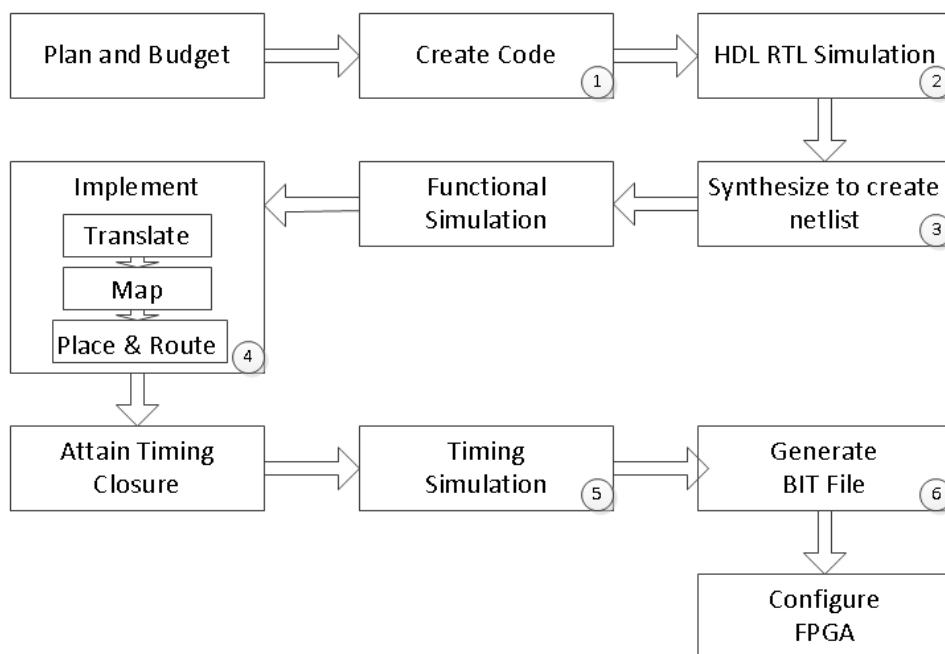


Figure 1. A typical design flow

Objectives

After completing this tutorial, you will be able to:

- Create a Vivado project sourcing HDL model(s) and targeting a specific FPGA device located on the Nexys4 board
- Use the provided partially completed Xilinx Design Constraint (XDC) file to constrain some of the pin locations
- Add additional constraints using the Tcl scripting feature of Vivado
- Simulate the design using the XSim simulator
- Synthesize and implement the design
- Generate the bitstream
- Configure the FPGA using the generated bitstream and verify the functionality
- Go through the design flow in batch mode using the Tcl script

Procedure

This tutorial is broken into steps that consist of general overview statements providing information on the detailed instructions that follow. Follow these detailed instructions to progress through the tutorial.

Design Description

The design consists of some inputs directly connected to the corresponding output LEDs. Other inputs are logically operated on before the results are output on the remaining LEDs as shown in **Figure 1**.

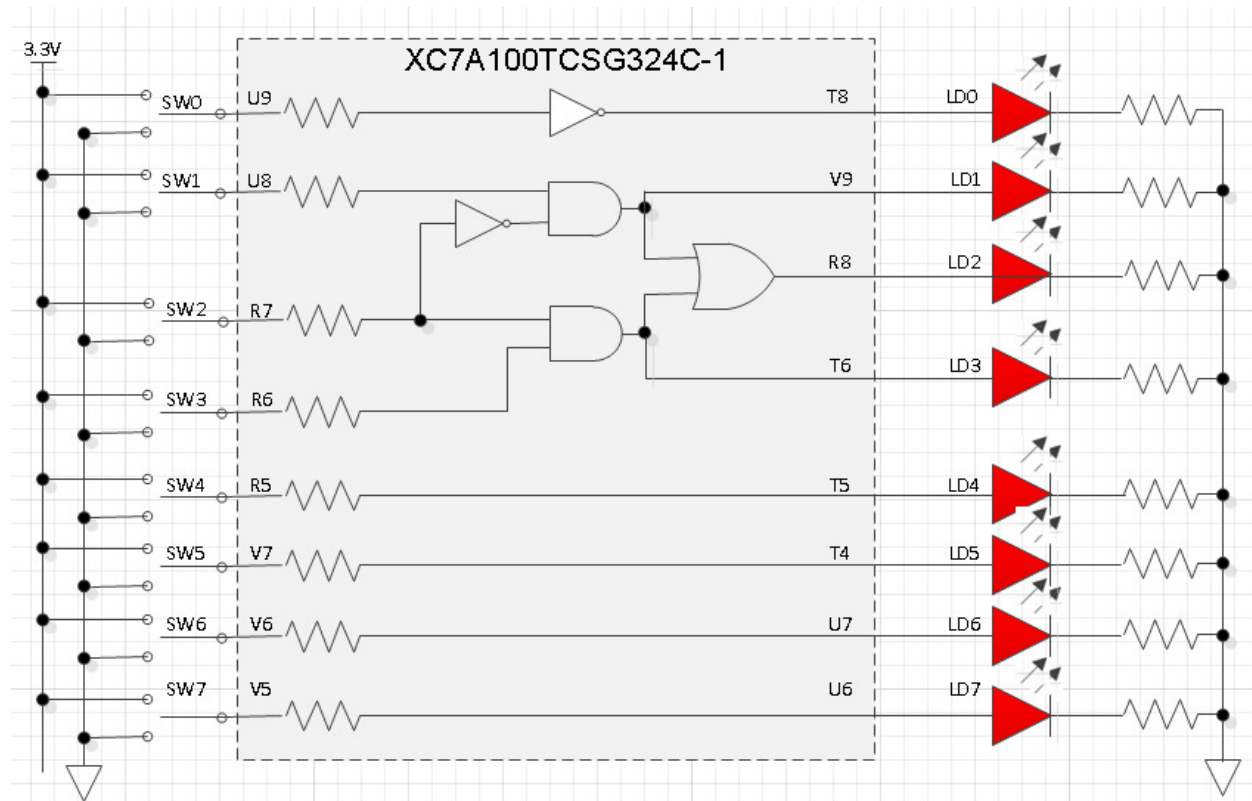


Figure 2. Completed Design

General Flow for this tutorial

- Create a Vivado project and analyze source files
- Simulate the design using XSim simulator
- Synthesize the design
- Implement the design
- Perform the timing simulation
- Verify the functionality in hardware using the Nexys4 board
- Run the tools in batch mode using the provided Tcl script

Create a Vivado Project using IDE

Step 1

1-1. Launch Vivado and create a project targeting the XC7A100TCSG324C-1 device and using the Verilog HDL. Use the provided tutorial.v and tutorial.xdc files from the *sources* directory.

1-1-1. Open Vivado by selecting **Start > All Programs > Xilinx Design Tools > Vivado 2013.3 > Vivado 2013.3**

1-1-2. Click **Create New Project** to start the wizard. You will see *Create A New Vivado Project* dialog box. Click **Next**.

1-1-3. Click the Browse button of the *Project location* field of the **New Project** form, browse to **c:\xup\digital**, and click **Select**.

1-1-4. Enter **tutorial** in the *Project name* field. Make sure that the *Create Project Subdirectory* box is checked. Click **Next**.

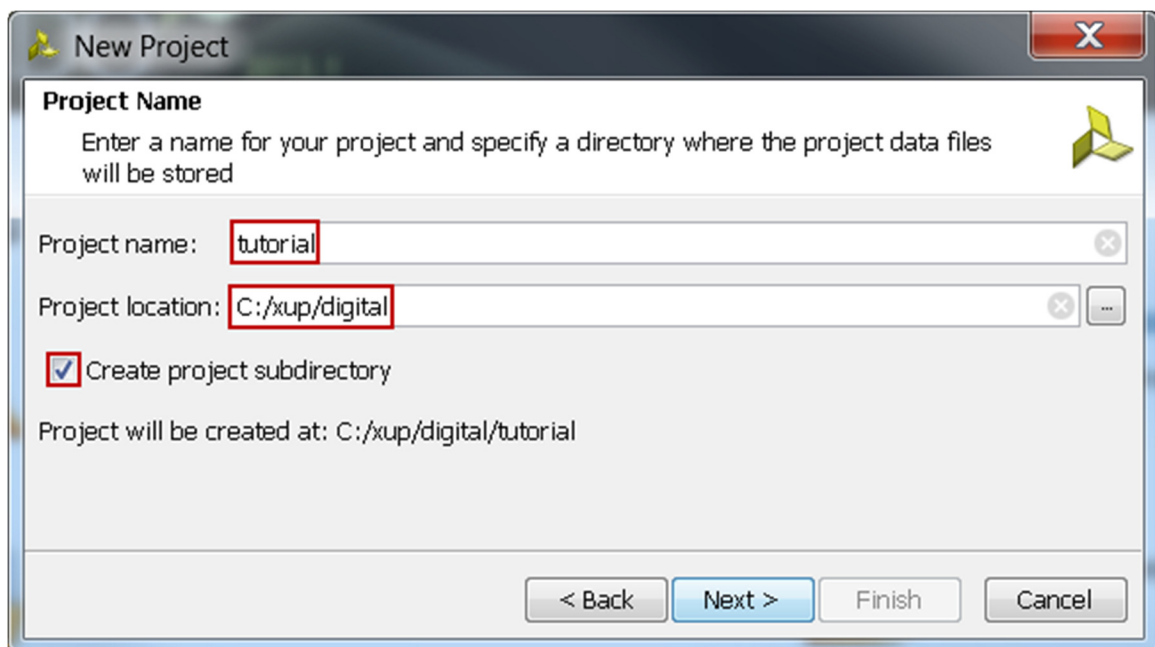


Figure 3. Project Name and Location entry

1-1-5. Select **RTL Project** option in the *Project Type* form, and click **Next**.

1-1-6. Select **Verilog** as the *Target language* and *Simulator language* in the *Add Sources* form.

1-1-7. Click on the **Add Files...** button, browse to the **c:\xup\digital\sources\tutorial** directory, select *tutorial.v*, click **Open**, and then click **Next**.

1-1-8. Click **Next** to get to the *Add Constraints* form.

1-1-9. Click **Next** if the entry is already auto-populated, otherwise click on the **Add Files...** button, browse to the **c:\xup\digital\sources\tutorial** directory and select *tutorial.xdc*, and click **Open**.

This Xilinx Design Constraints file assigns the physical IO locations on FPGA to the switches and LEDs located on the board. This information can be obtained either through a board's schematic or board's user guide.

- 1-1-10. In the *Default Part* form, using the **Parts** option and various drop-down fields of the **Filter** section, select the **XC7A100TCSG324-1** part. Click **Next**.

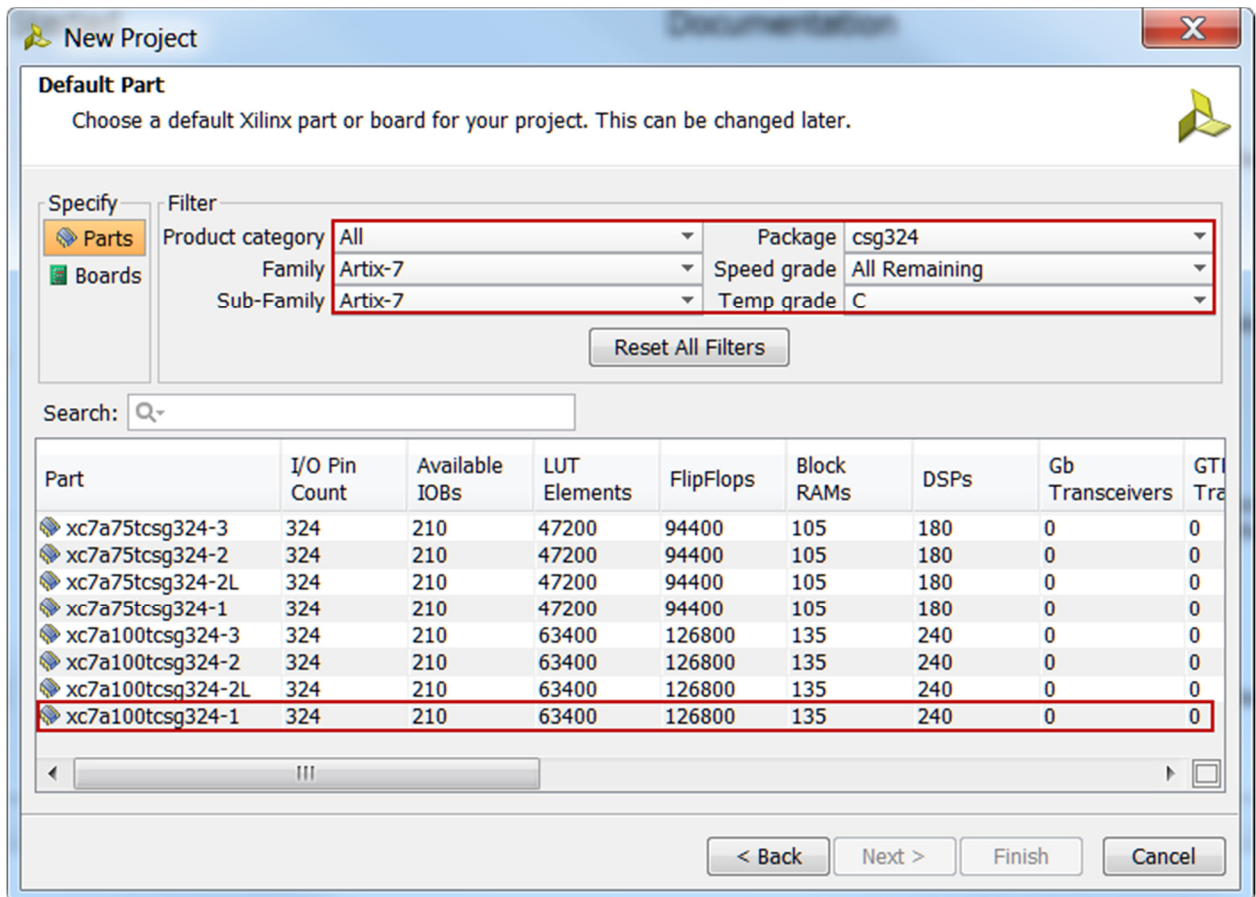


Figure 4. Part Selection

- 1-1-11. Click **Finish** to create the Vivado project.

Use the Windows Explorer and look at the `c:\xup\digital\tutorial` directory. You will find that the **tutorial.data** and **tutorial.srcs** directories and the **tutorial.xpr** (Vivado) project file have been created. The **tutorial.data** directory is a place holder for the Vivado program database. Two more directories, **constrs_1** and **sources_1**, are created under the **tutorial.srcs** directory; deep down under them, the copied **tutorial.xdc** (constraint) and **tutorial.v** (source) files respectively are placed.

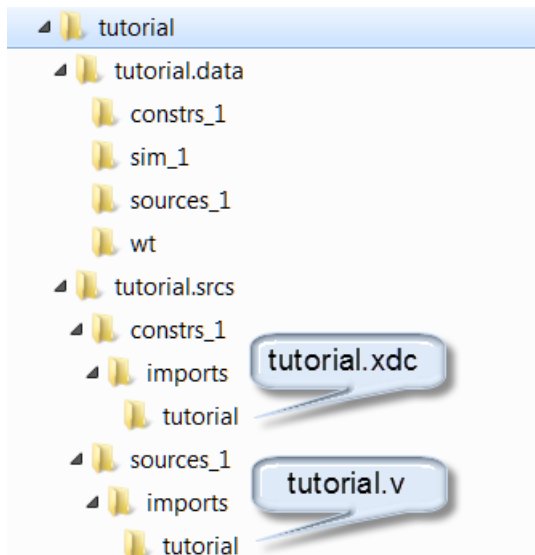


Figure 5. Generated directory structure

1-2. Open the tutorial.v source and analyze the content.

1-2-1. In the *Sources* pane, double-click the **tutorial.v** entry to open the file in text mode.

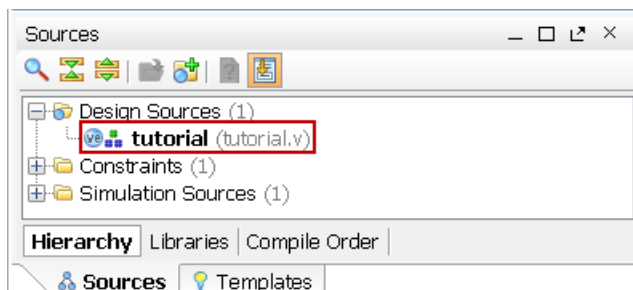


Figure 6. Opening the source file

1-2-2. Notice in the Verilog code that the first line defines the timescale directive for the simulator. Lines 2-5 are comment lines describing the module name and the purpose of the module.

1-2-3. Line 7 defines the beginning (marked with keyword **module**) and Line 19 defines the end of the module (marked with keyword **endmodule**).

1-2-4. Lines 8-9 define the input and output ports whereas lines 12-17 define the actual functionality.

1-3. Open the tutorial.xdc source and analyze the content.

1-3-1. In the *Sources* pane, expand the *Constraints* folder and double-click the **tutorial.xdc** entry to open the file in text mode.

1-5. Add I/O constraints for the missing LED and switch pins.

1-5-1. Once RTL analysis is performed, another standard layout called the *I/O Planning* is available. Click on the drop-down button and select the *I/O Planning* layout.

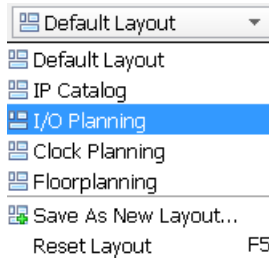


Figure 9. I/O Planning layout selection

Notice that the Package view is displayed in the Auxiliary View area, Device Constraints tab is selected, and I/O ports tab is displayed in the Console View area. Also notice that design ports (led and swt) are listed in the I/O Ports tab with both having multiple I/O standards.

Move the mouse cursor over the Package view, highlighting different pins. Notice the pin site number is shown at the bottom of the Vivado GUI, along with the pin type (User IO, GND, VCCO...) and the I/O bank it belongs to.

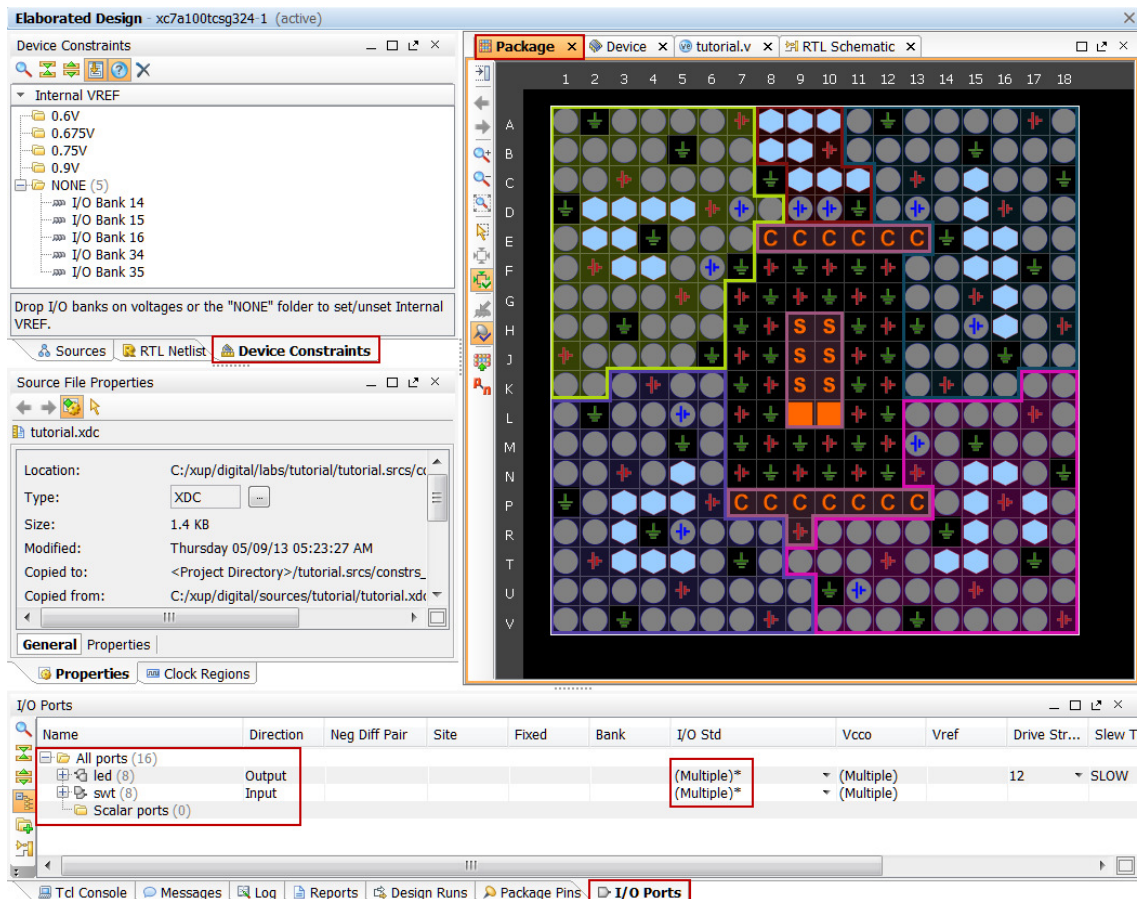


Figure 10. I/O Planning layout view

- 1-5-2. Expand the **led** and **swt** ports by clicking on the + box and observe that led [6:0] and swt[6:0] use the LVCMOS33 I/O standard whereas led[7] and swt[7] use defaults to LVCMOS18; hence you can see *multiple* I/O standard in the collapsed view.

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco
All ports (16)							
led (8)	Output					(Multiple)*	(Multiple)
led[7]	Output					default (LVCMOS18)	1.800
led[6]	Output					LVCMOS33*	3.300
led[5]	Output					LVCMOS33*	3.300
led[4]	Output					LVCMOS33*	3.300
led[3]	Output					LVCMOS33*	3.300
led[2]	Output					LVCMOS33*	3.300
led[1]	Output					LVCMOS33*	3.300
led[0]	Output					LVCMOS33*	3.300
swt (8)	Input					(Multiple)*	(Multiple)
swt[7]	Input					default (LVCMOS18)	1.800
swt[6]	Input					LVCMOS33*	3.300
swt[5]	Input					LVCMOS33*	3.300
swt[4]	Input					LVCMOS33*	3.300
swt[3]	Input					LVCMOS33*	3.300
swt[2]	Input					LVCMOS33*	3.300
swt[1]	Input					LVCMOS33*	3.300
swt[0]	Input					LVCMOS33*	3.300
Scalar ports (0)							

Figure 11. I/O Ports tab

- 1-5-3. Click under the *I/O Std* column across the **led[7]** row and select *LVCOMS33*. This assigns the LVCMOS33 standard to the site.

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std
All ports (16)						
led (8)	Output					LVCMOS18
led[7]	Output					LVCMOS18
led[6]	Output					LVCMOS12
led[5]	Output					LVCMOS15
led[4]	Output					LVCMOS18
led[3]	Output					LVCMOS25
led[2]	Output					LVCMOS33
led[1]	Output					LVTTTL
led[0]	Output					MOBILE_DDR
swt (8)	Input					PCI33_3
swt[7]	Input					

Figure 12 Assigning I/O standard

- 1-5-4. Similarly, click under the *Site* column across **led[7]** row to see a drop-down box appear. Type **U** in the field to jump to Uxx pins, scroll-down until you see U6, select U6 and hit the *Enter* key to assign the pin. Notice after selecting the pin U6, the *Site* column automatically places **led[7]** lower down in the column since it alphabetically arranges the site/pin names.
- 1-5-5. You can also assign the pin constraints using tcl commands. Type in the following two commands in the Tcl Console tab to assign the V5 pin location and the *LVCSMOS33* I/O standard to **swt[7]** hitting the *Enter* key after each command.

```
set_property package_pin V5 [get_ports {swt[7]}]
set_property iostandard LVCMOS33 [get_ports [list {swt[7]}]]
```

Observe the pin and I/O standard assignments in the I/O Ports tab.

You can also assign the pin by selecting its entry (swt[7]) in the I/O ports tab, and dragging it to the Package view, and placing it at the V5 location. You can assign the LVCMOS33 standard by selecting its entry (swt[7]), selecting Configure tab of the I/O Port Properties window, followed by clicking the drop-down button of the I/O standard field, and selecting LVCMOS33.

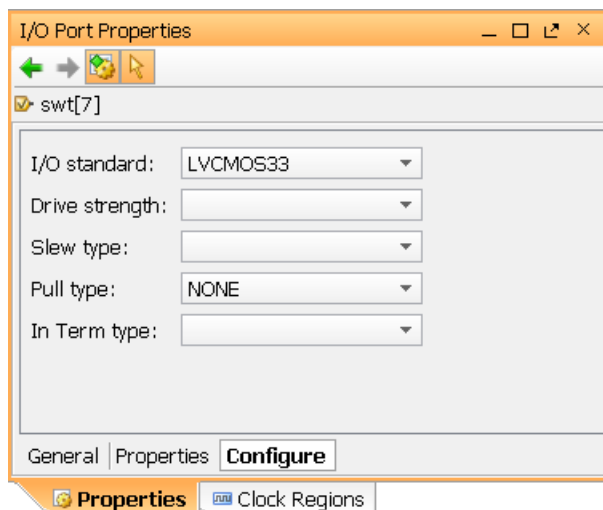


Figure 13. Assigning I/O standard through the I/O Port Properties form

1-5-6. Select **File > Save Constraints** and click **OK** to save the constraints in the **tutorial.xdc** file.

1-5-7. Click **Update** followed by **OK** to update the existing constraint file.

Note that the constraints are updated in the tutorial.xdc file under the tutorial project directory and not under the sources directory.

Simulate the Design using the XSim Simulator

Step 2

2-1. Add the tutorial_tb.v testbench file.

2-1-1. Click **Add Sources** under the *Project Manager* tasks of the *Flow Navigator* pane.



Figure 14. Add Sources

2-1-2. Select the *Add or Create Simulation Sources* option and click **Next**.

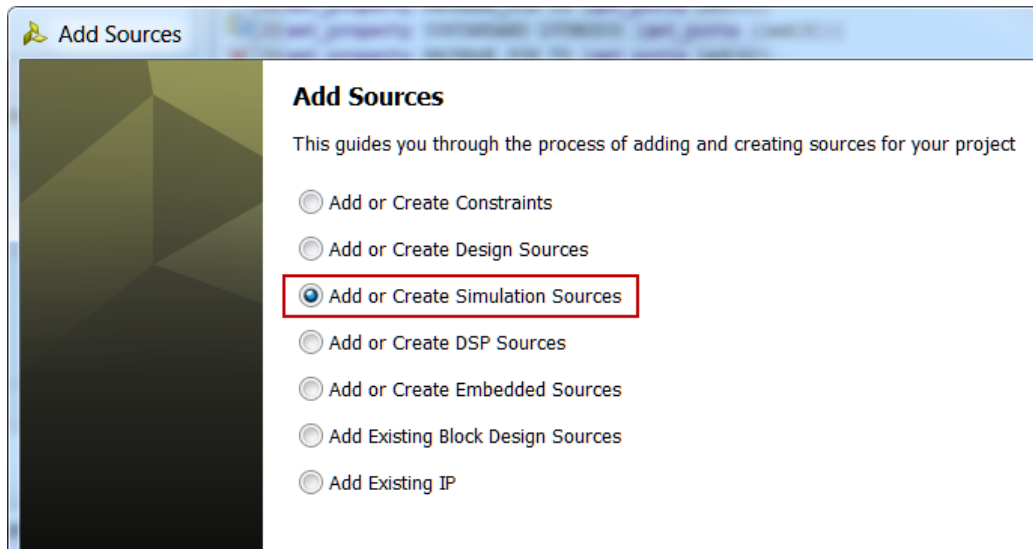


Figure 15. Selecting Simulation Sources option

- 2-1-3. In the *Add Sources Files* form, click the **Add Files...** button.
- 2-1-4. Browse to the **c:\xup\digital\sources** folder and select *tutorial_tb.v* and click **OK**.
- 2-1-5. Click **Finish**.
- 2-1-6. Select the *Sources* tab and expand the *Simulation Sources* group.

The *tutorial_tb.v* file is added under the *Simulation Sources* group, and **tutorial.v** is automatically placed in its hierarchy as a *tut1* instance.

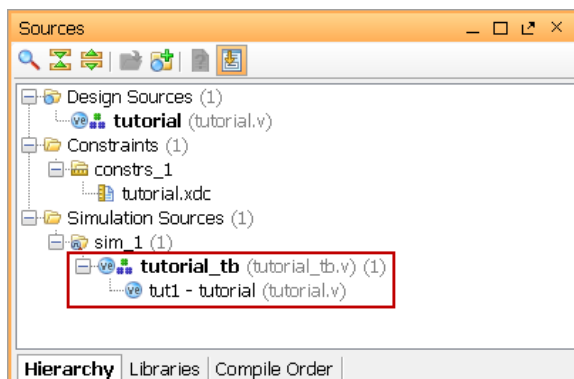


Figure 16. Simulation Sources hierarchy

- 2-1-7. Using the Windows Explorer, verify that the **sim_1** directory is created at the same level as **constrs_1** and **sources_1** directories under the **tutorial.srcs** directory, and that a copy of *tutorial_tb.v* is placed under **tutorial.srcs > sim_1 > imports > sources**.
- 2-1-8. Double-click on the **tutorial_tb** in the *Sources* pane to view its contents.

```

1 `timescale 1ns / 1ps
2 ////////////////////////////////////////////////////////////////////
3 // Module Name: tutorial_tb
4 ////////////////////////////////////////////////////////////////////
5 module tutorial_tb(
6
7     );
8
9     reg [7:0] switches;
10    wire [7:0] leds;
11    reg [7:0] e_led;
12
13    integer i;
14
15    tutorial tut1(.led(leds),.swt(switches));
16
17    function [7:0] expected_led;
18        input [7:0] swt;
19    begin
20        expected_led[0] = ~swt[0];
21        expected_led[1] = swt[1] & ~swt[2];
22        expected_led[3] = swt[2] & swt[3];
23        expected_led[2] = expected_led[1] | expected_led[3];
24        expected_led[7:4] = swt[7:4];
25    end
26    endfunction
27
28    initial
29    begin
30        for (i=0; i < 255; i=i+2)
31            begin
32                #50 switches=i;
33                #10 e_led = expected_led(switches);
34                if(leds == e_led)
35                    $display("LED output matched at", $time);
36                else
37                    $display("LED output mis-matched at ", $time, ": expected: %b, actual: %b", e_led, leds);
38            end
39        end
40
41 endmodule

```

Figure 17. The self-checking testbench

The testbench defines the simulation step size and the resolution in line 1. The testbench module definition begins on line 5. Line 15 instantiates the DUT (device/module under test). Lines 17 through 26 define the same module functionality for the expected value computation. Lines 28 through 39 define the stimuli generation and compares the expected output with what the DUT provides. Line 41 ends the testbench. The \$display task will print the message in the simulator console window when the simulation is run.

2-2. Simulate the design for 200 ns using the XSim simulator.

2-2-1. Select **Simulation Settings** under the *Project Manager* tasks of the *Flow Navigator* pane.

A **Project Settings** form will appear showing the **Simulation** properties form.

2-2-2. Select the **Simulation** tab, and set the **Simulation Run Time** value to 200 ns and click **OK**.

2-2-3. Click on **Run Simulation > Run Behavioral Simulation** under the *Project Manager* tasks of the *Flow Navigator* pane.

The testbench and source files will be compiled and the XSim simulator will be run (assuming no errors). You will see a simulator output similar to the one shown below.

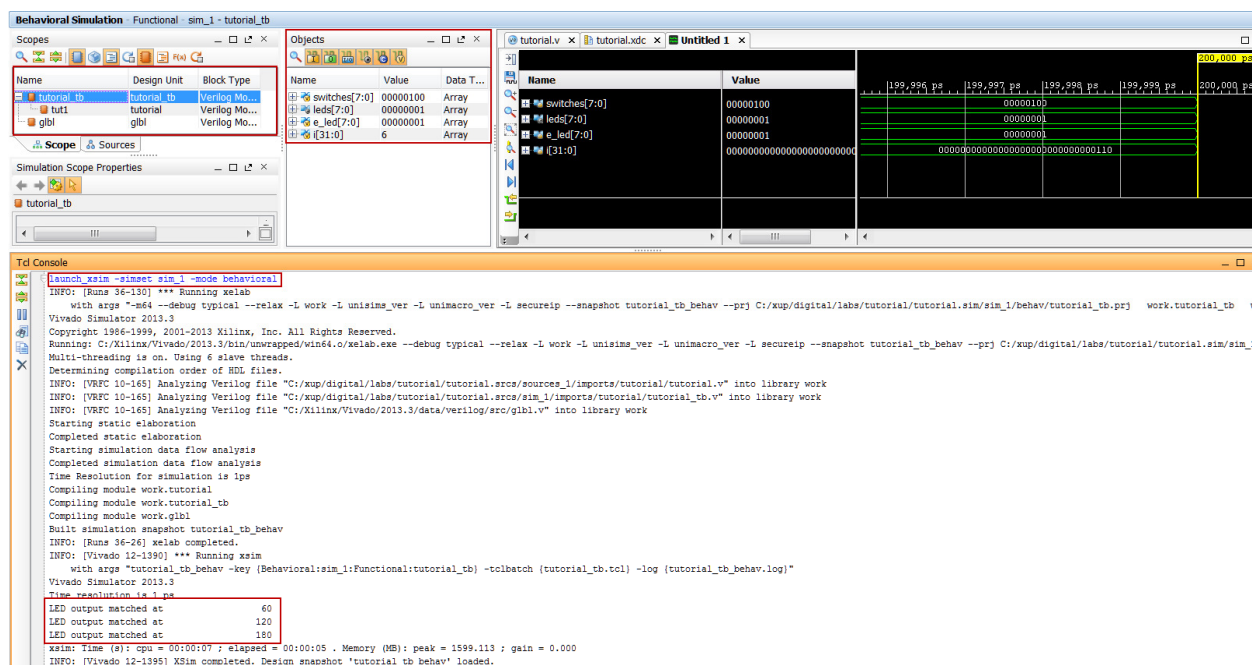


Figure 18. Simulator output

You will see four main views: (i) *Scopes*, where the testbench hierarchy as well as `gbl1` instances are displayed, (ii) *Objects*, where top-level signals are displayed, (iii) the waveform window, and (iv) *Tcl Console* where the simulation activities are displayed. Notice that since the testbench used is self-checking, the results are displayed as the simulation is run.

Notice that the **tutorial.sim** directory is created under the **tutorial** directory, along with several lower-level directories.

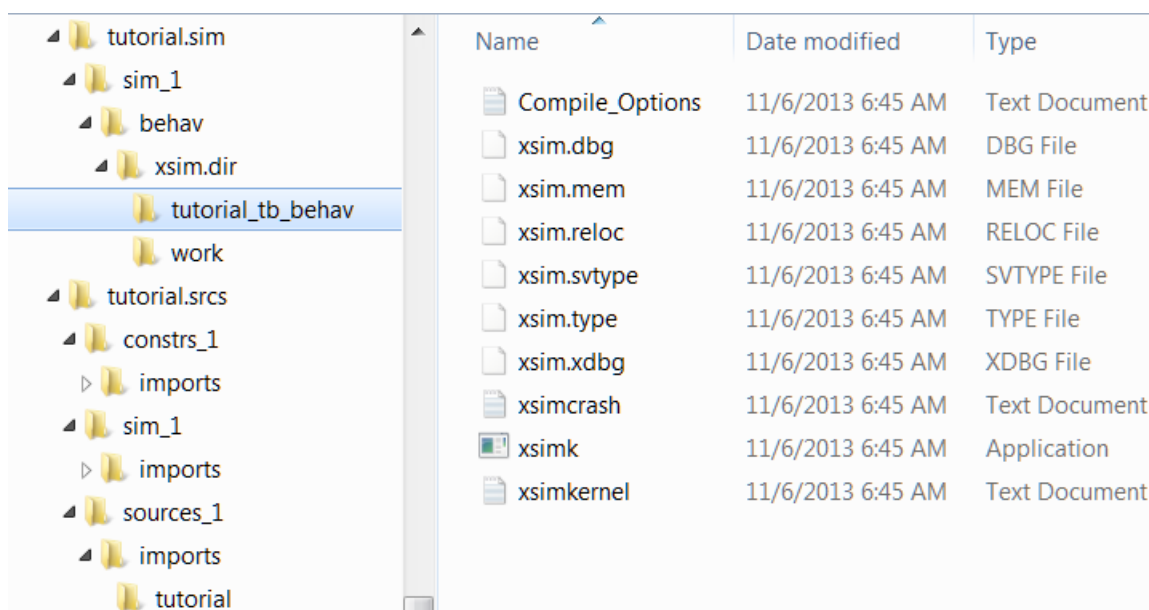



Figure 19. Directory structure after running behavioral simulation

- 2-2-4.** Click on the *Zoom Fit* button () located left of the waveform window to see the entire waveform.

Notice that the output changes when the input changes.

You can also float the simulation waveform window by clicking on the *Float* button on the upper right hand side of the view. This will allow you to have a wider window to view the simulation waveforms. To reintegrate the floating window back into the GUI, simply click on the *Dock Window* button.

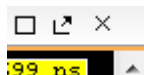


Figure 20. Float Button



Figure 21. Dock Window Button

2-3. Change display format if desired.

- 2-3-1.** Select **i[31:0]** in the waveform window, right-click, select *Radix*, and then select *Unsigned Decimal* to view the for-loop index in *integer* form. Similarly, change the radix of **switches[7:0]** to *Hexadecimal*. Leave the **leds[7:0]** and **e_led[7:0]** radix to *binary* as we want to see each output bit.

2-4. Add more signals to monitor lower-level signals and continue to run the simulation for 500 ns.

- 2-4-1.** Expand the **tutorial_tb** instance, if necessary, in the *Scopes* window and select the **tut1** instance.

The **swt[7:0]** and **led[7:0]** signals will be displayed in the *Objects* window.

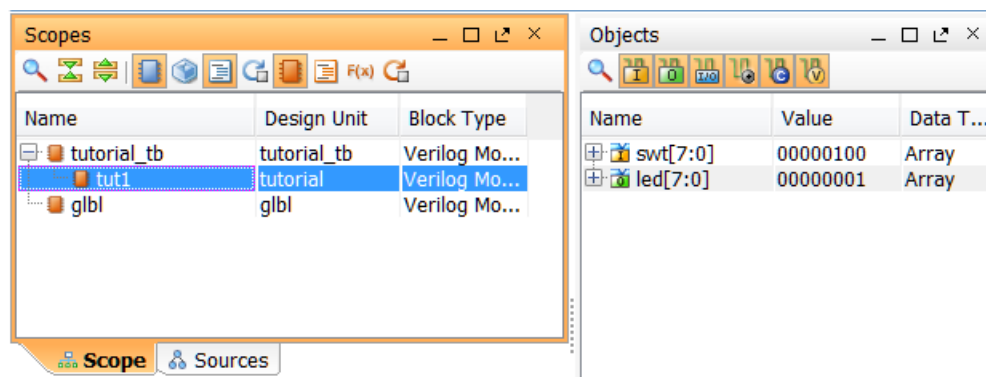



Figure 22. Selecting lower-level signals

- 2-4-2.** Select **swt[7:0]** and **led[7:0]** and drag them into the waveform window to monitor those lower-level signals.

- 2-4-3.** On the simulator tool buttons ribbon bar, type 500 in the time window, click on the drop-down button of the units field and select **ns**, and click on the () button.

The simulation will run for an additional 500 ns.

- 2-4-4. Click on the *Zoom Fit* button and observe the output.

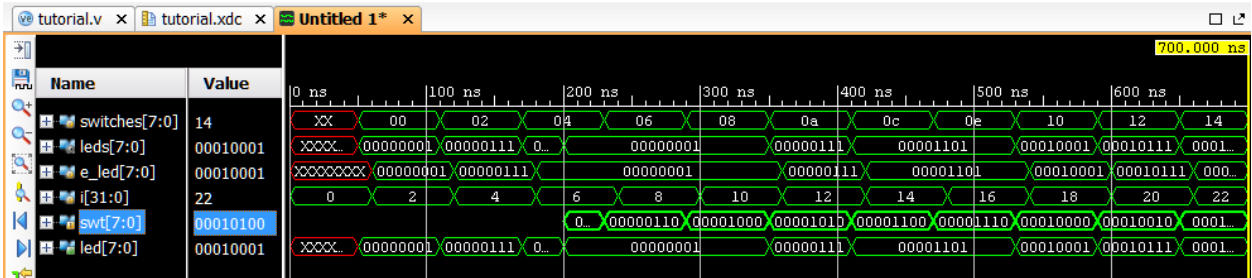


Figure 23. Running simulation for additional 500 ns

- 2-4-5. Close the simulator by selecting **File > Close Simulation**.
- 2-4-6. Click **OK** and then click **No** to close it without saving the waveform.

Synthesize the Design

Step 3

- 3-1. **Synthesize the design with the Vivado synthesis tool and analyze the Project Summary output.**

- 3-1-1. Click on **Run Synthesis** under the *Synthesis* tasks of the *Flow Navigator* pane.

The synthesis process will be run on the tutorial.v file (and all its hierarchical files if they exist). When the process is completed a *Synthesis Completed* dialog box with three options will be displayed.

- 3-1-2. Select the *Open Synthesized Design* option and click **OK** as we want to look at the synthesis output before progressing to the implementation stage.

Click **Yes** to close the elaborated design if the dialog box is displayed.

- 3-1-3. Select the **Project Summary** tab (Select default layout if the tab is not visible) and understand the various windows.

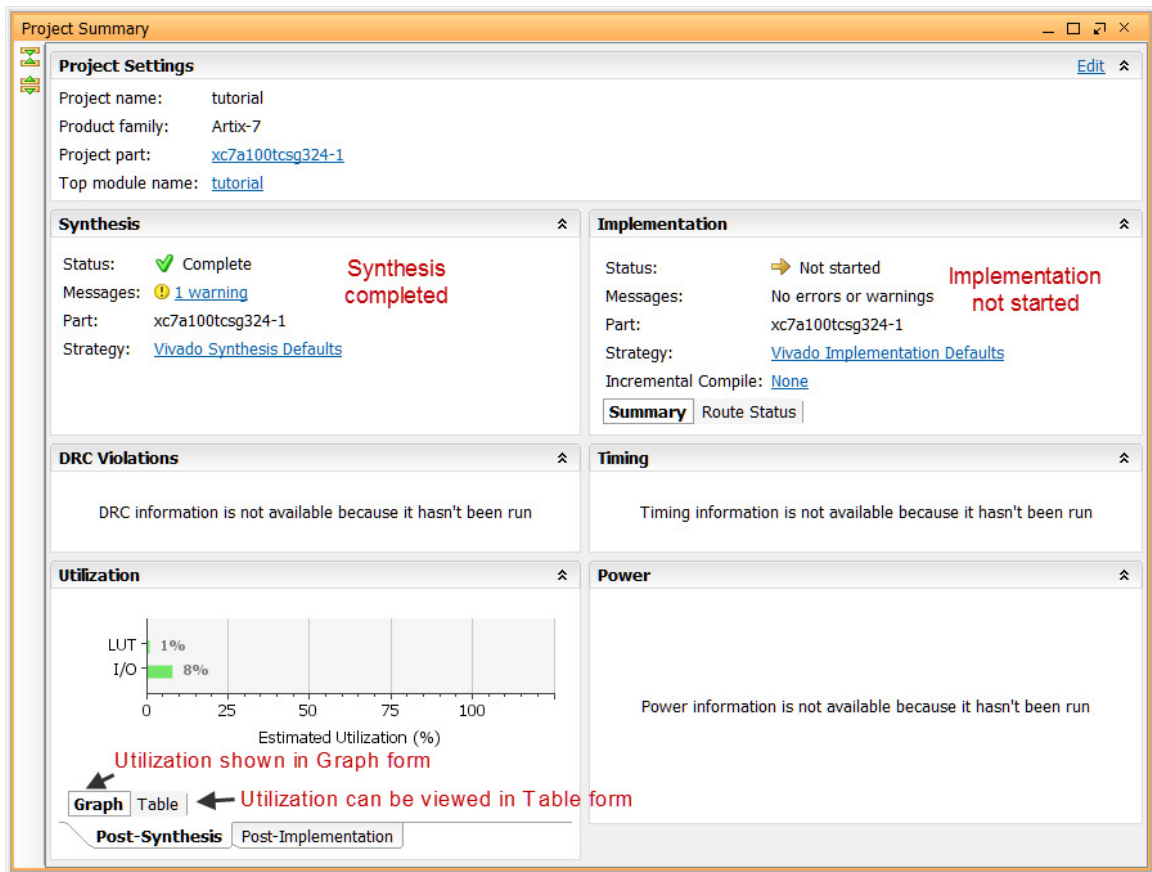


Figure 24. Project Summary view

Click on the various links to see what information they provide and which allows you to change the synthesis settings.

3-1-4. Click on the **Table** tab in the **Project Summary** tab.

Notice that there are an estimated three LUTs and 16 IOs (8 input and 8 output) that are used.

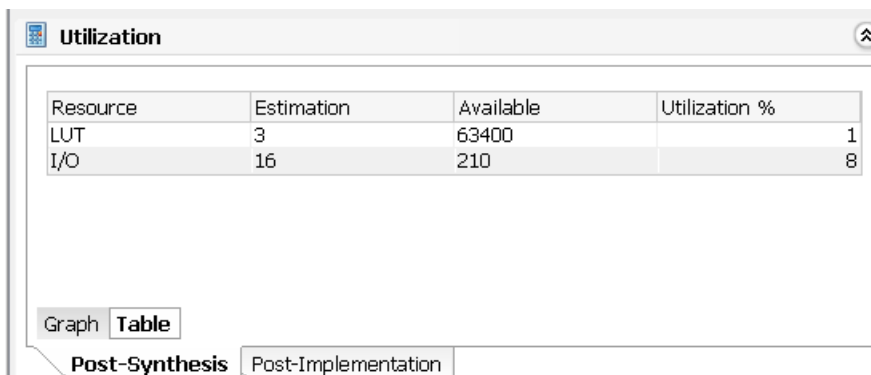


Figure 25. Resource utilization estimation summary

3-1-5. Click on **Schematic** under the *Open Synthesized Design* tasks of *Synthesis* tasks of the *Flow Navigator* pane to view the synthesized design in a schematic view.

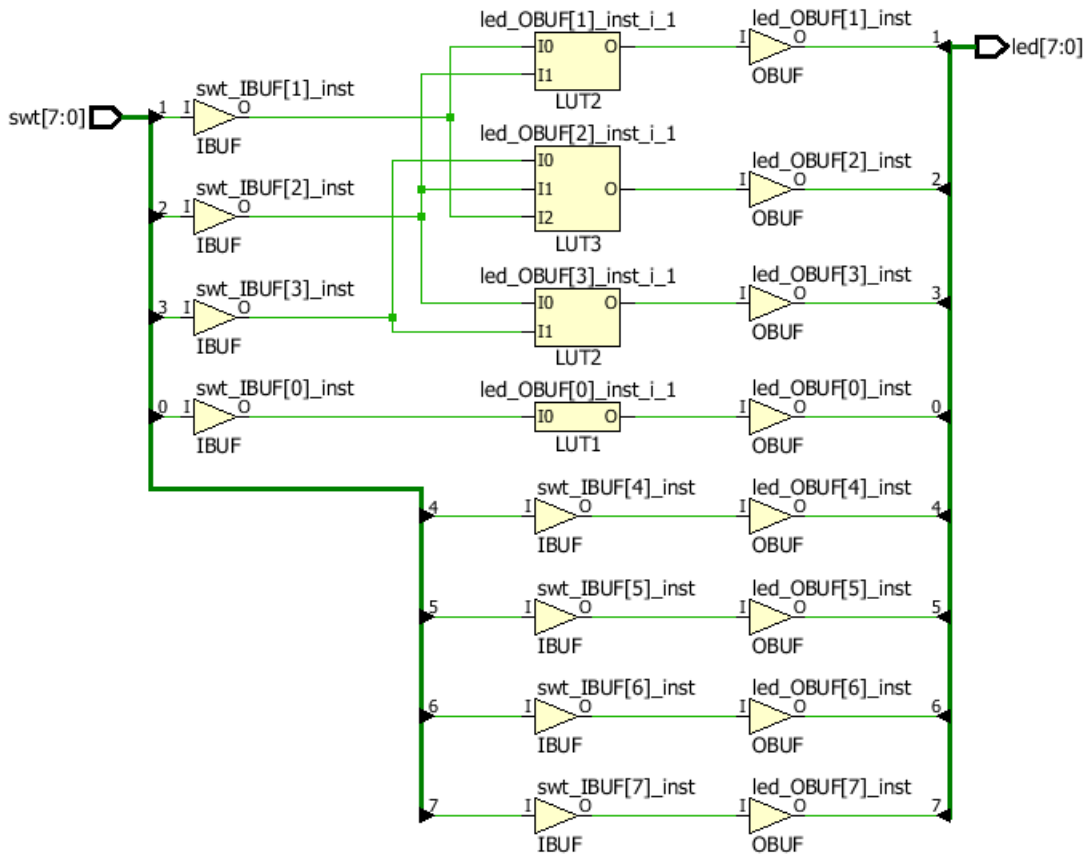


Figure 26. Synthesized design's schematic view

Notice that IBUF and OBUF are automatically instantiated (added) to the design as the input and output are buffered. The logical gates are implemented in LUTs (1 input is listed as LUT1, 2 input is listed as LUT2, and 3 input is listed as LUT3). Four gates in RTL analysis output is mapped into four LUTs in the synthesized output.

Using the Windows Explorer, verify that **tutorial.runs** directory is created under **tutorial**. Under the **runs** directory, **synth_1** directory is created which holds several temporary sub-directories.

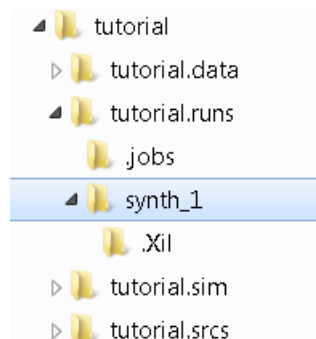


Figure 27. Directory structure after synthesizing the design

Implement the Design

Step 4

4-1. Implement the design with the Vivado Implementation Defaults (Vivado Implementation 2013) settings and analyze the Project Summary output.

4-1-1. Click on **Run Implementation** under the *Implementation* tasks of the *Flow Navigator* pane.

The implementation process will be run on the synthesis output files. When the process is completed an *Implementation Completed* dialog box with three options will be displayed.

4-1-2. Select **Open implemented design** and click **OK** as we want to look at the implemented design in a Device view tab.

4-1-3. Click **Yes** to close the synthesized design.

The implemented design will be opened.

4-1-4. In the *Netlist* pane, select one of the nets (e.g. `n_0_led_OBUF[1]_inst_i_1`) and notice that the net displayed in the X1Y1 clock region in the Device view tab (you may have to zoom in to see it).

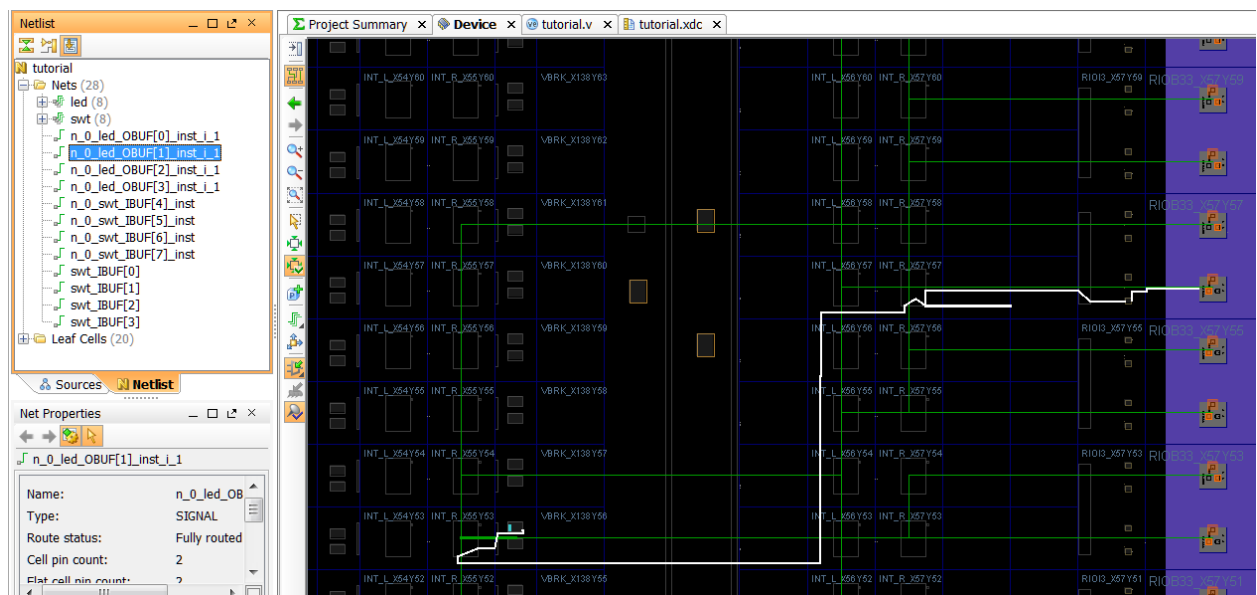


Figure 28. Viewing implemented design

4-1-5. Close the implemented design view and select the **Project Summary** tab (you may have to change to the Default Layout view) and observe the results.

Notice that the actual resource utilization is three LUTs and 16 IOs. Also, it indicates that no timing constraints were defined for this design (since the design is combinatorial). Select the **Post-implementation** tabs under the *Timing* and *Utilization* windows.

Project Summary

Project Settings

Project name: tutorial
 Product family: Artix-7
 Project part: xc7a100tcsq324-1
 Top module name: tutorial

Synthesis

Status: ✔ Complete
 Messages: ⚠ 1 warning
 Part: xc7a100tcsq324-1
 Strategy: [Vivado Synthesis Defaults](#)

Implementation

Status: ✔ Complete
 Messages: ⚠ 1 warning
 Part: xc7a100tcsq324-1
 Strategy: [Vivado Implementation Defaults](#)
 Incremental Compile: None
 Summary Route Status

DRC Violations

Summary: ❌ 0 errors
⚠ 0 critical warnings
⚠ 3 warnings
ℹ 0 advisories

Timing

Worst Negative Slack (WNS): 0 ns
 Total Negative Slack (TNS): 0 ns
 Number of Failing Endpoints: 0
 Total Number of Endpoints: 0
 Setup Hold Pulse Width
 Post-Synthesis Post-Implementation

Utilization

Resource	Utilization	Available	Utilization %
LUT	3	63400	1
I/O	16	210	8

Graph Table
 Post-Synthesis Post-Implementation

Power

Total On-Chip Power: **0.097 W**
 Junction Temperature: **25.4 °C**
 Thermal Margin: 59.6 °C (12.9 W)
 Effective θJA: 4.6 °C/W
 Power supplied to off-chip devices: 0 W
 Confidence level: [Low](#)
 Summary On-Chip
 Power supplied to off-chip de

Figure 29. Implementation results

Using the Windows Explorer, verify that **impl_1** directory is created at the same level as **synth_1** under the **tutorial_runs** directory. The **impl_1** directory contains several files including the report files.

- 4-1-6.** Select the **Reports** tab, and double-click on the *Utilization Report* entry under the *Place Design* section. The report will be displayed in the auxiliary view pane showing resources utilization. Note that since the design is combinatorial no registers are used.

Perform Timing Simulation


Step 5

5-1. Run a timing simulation.

- 5-1-1.** Select **Run Simulation > Run Post-Implementation Timing Simulation** process under the *Simulation* tasks of the *Flow Navigator* pane.

The XSim simulator will be launched using the implemented design and **tutorial_tb** as the top-level module..

Using the Windows Explorer, verify that **timing** directory is created under the **tutorial.sim > sim_1 > impl** directory. The **timing** directory contains generated files to run the timing simulation.

- 5-1-2. Click on the **Zoom Fit** button to see the waveform window from 0 to 200 ns.
- 5-1-3. Right-click at 50 ns (where the switch input is set to 0000000b) and select **Markers > Add Marker**.
- 5-1-4. Similarly, right-click and add a marker at around 55.000 ns where the **leds** changes.
- 5-1-5. You can also add a marker by clicking on the Add Marker button (). Click on the **Add Marker** button and left-click at around 60 ns where **e_led** changes.

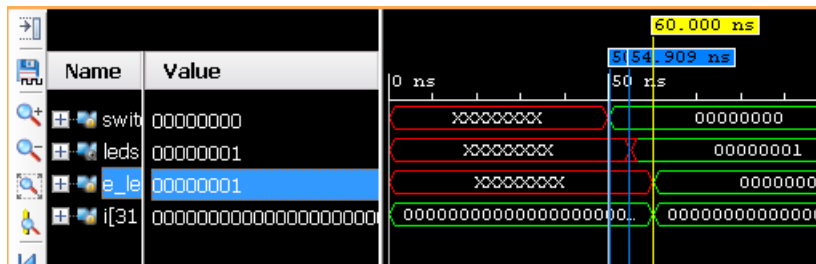


Figure 30. Timing simulation output

Notice that we monitored the expected led output at 10 ns after the input is changed (see the testbench) whereas the actual delay is about 5.000 ns.

- 5-1-6. Close the simulator by selecting **File > Close Simulation** without saving any changes.

Generate the Bitstream and Verify Functionality

Step 6

- 6-1. **Connect the board and power it ON. Generate the bitstream, open a hardware session, and program the FPGA.**

- 6-1-1. Click on the **Generate Bitstream** entry under the *Program and Debug* tasks of the *Flow Navigator* pane.

The bitstream generation process will be run on the implemented design. When the process is completed a *Bitstream Generation Completed* dialog box with three options will be displayed.

This process will have **tutorial.bit** file generated under **impl_1** directory which was generated under the **tutorial.runs** directory.

- 6-1-2. Make sure that the power supply source is jumper to *USB* and the provided Micro-USB cable is connected between the board and the PC. Note that you do not need to connect the power jack and the board can be powered and configured via USB alone

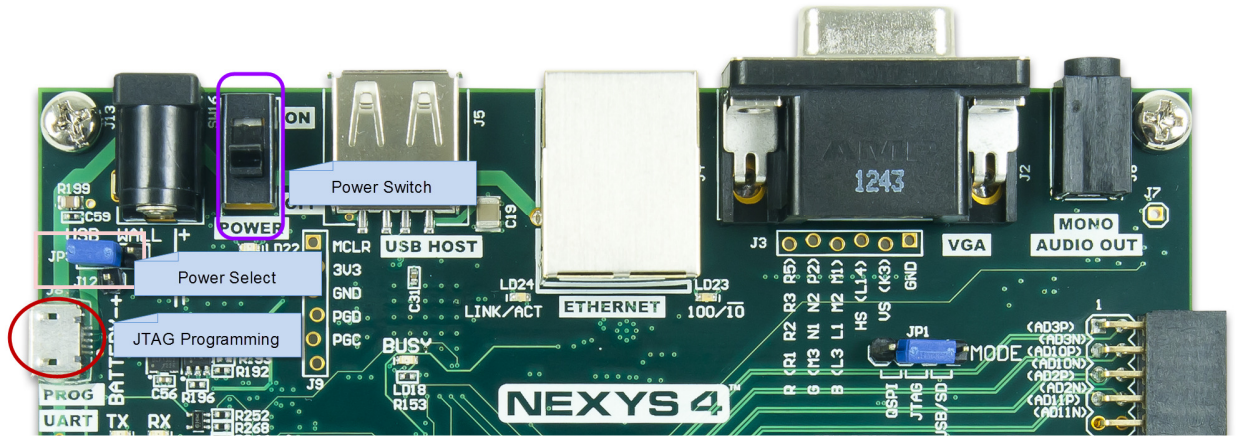


Figure 31. Board settings

6-1-3. Power **ON** the switch on the board.

6-1-4. Select the *Open Hardware Manager* option and click **OK**.

The Hardware Session window will open indicating “unconnected” status.

6-1-5. Click on the **Open a new hardware target** link.

You can also click on the Open Recent Hardware Target link if the board was already targeted before.

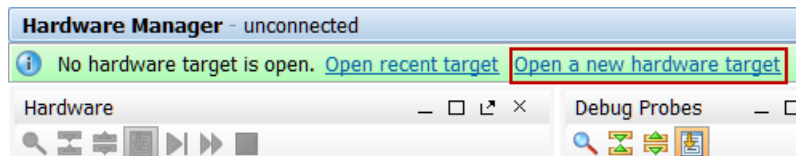


Figure 32. Opening new hardware target

6-1-6. Click **Next** to see the Vivado CSE Server Name form.

6-1-7. Click **Next** with the localhost port selected.

The JTAG cable will be searched and the Xilinx_tcf should be detected and identified as a hardware target. It will also show the hardware devices detected in the chain.

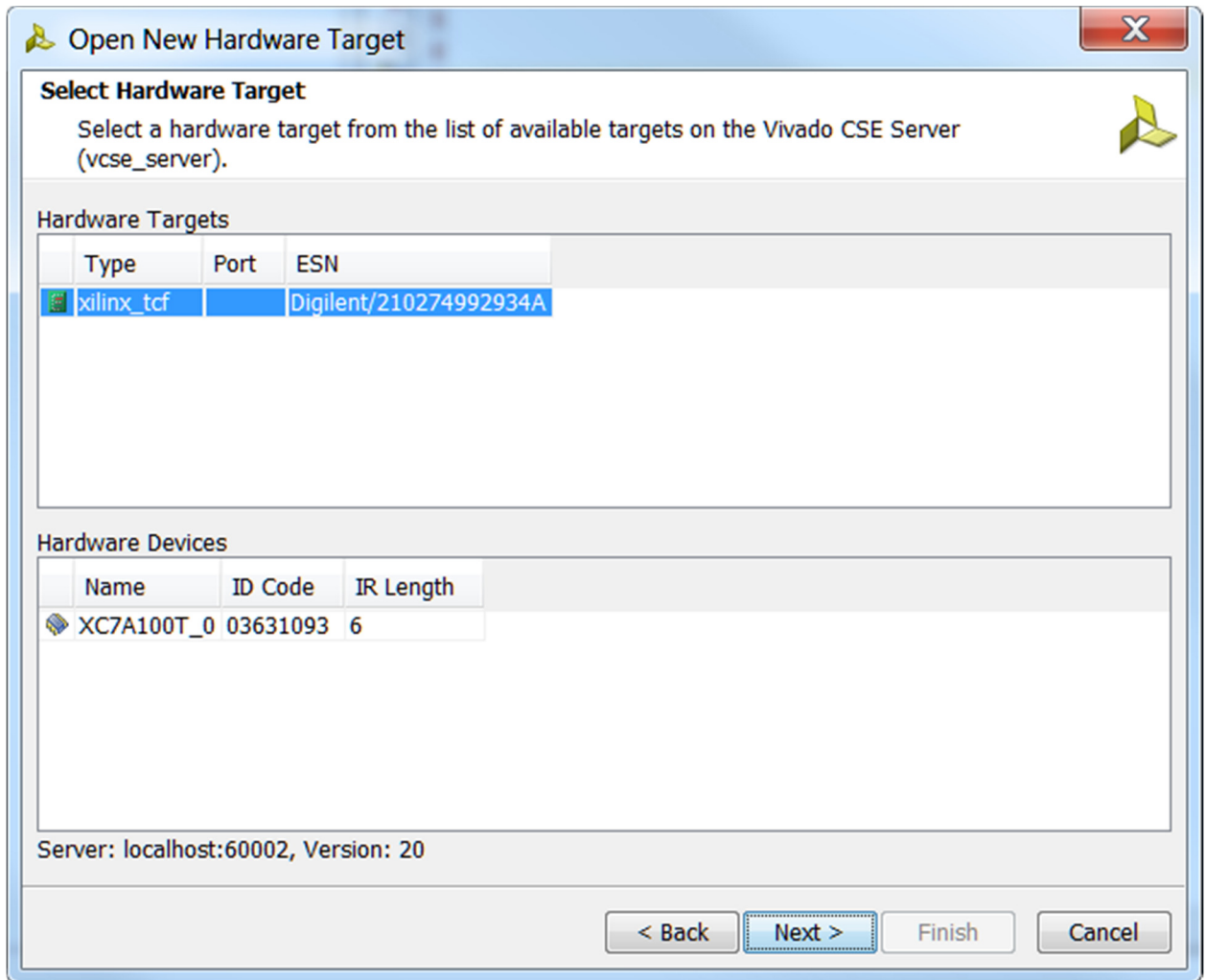


Figure 33. New hardware target detection

6-1-8. Click **Next** twice and **Finish**.

The Hardware Session status changes from Unconnected to the server name and the device is highlighted. Also notice that the Status indicates that it is not programmed.

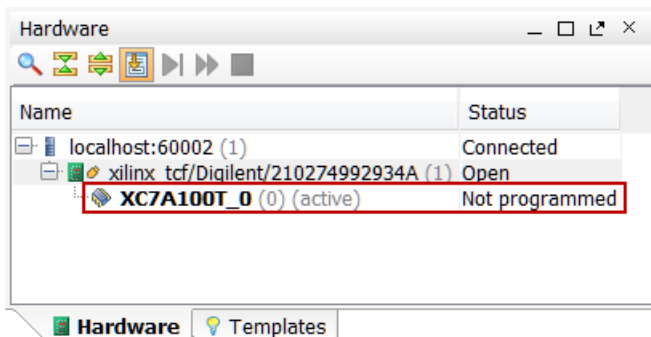


Figure 34. Opened hardware session

6-1-9. Select the device and verify that the tutorial.bit is selected as the programming file in the General tab.

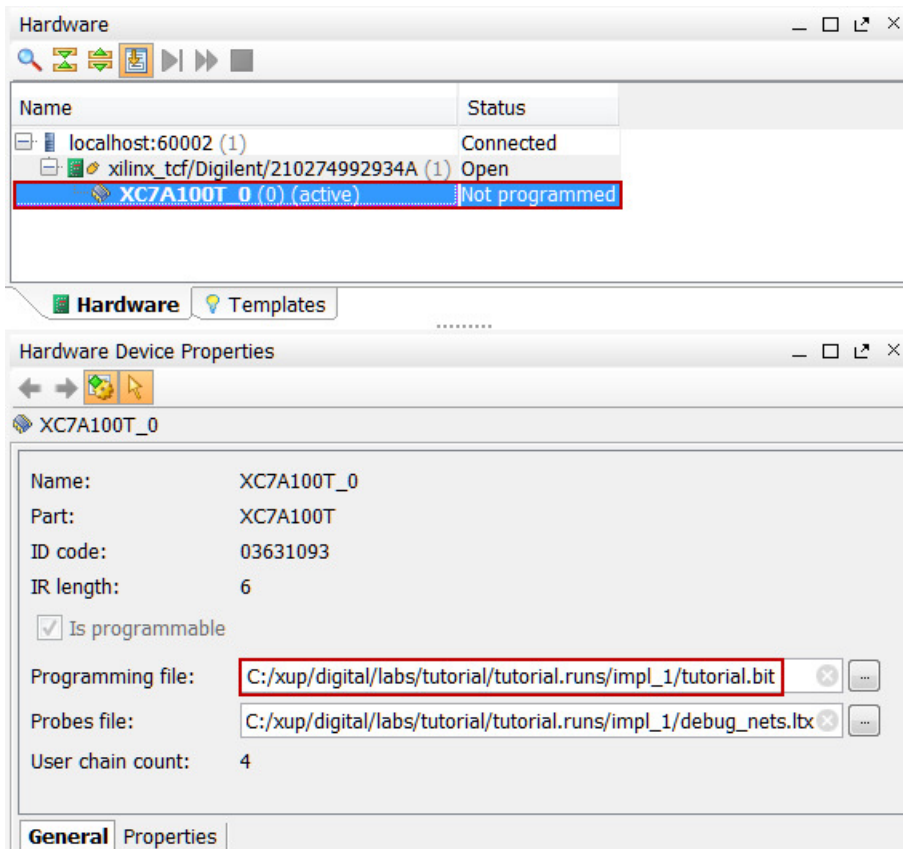


Figure 35. Programming file

6-1-10. Right-click on the device and select *Program Device...* to program the target FPGA device.

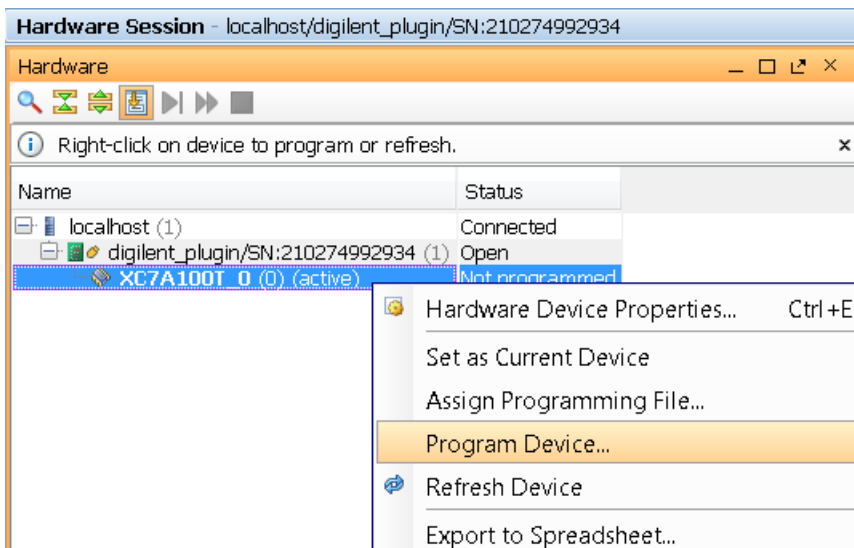


Figure 36. Selecting to program the FPGA

6-1-11. Click OK to program the FPGA with the selected bitstream.

The DONE light will lit when the device is programmed. You may see some LEDs lit depending on the switches position.

6-1-12. Verify the functionality by flipping switches and observing the output on the LEDs.

6-1-13. Close the hardware session by selecting **File > Close Hardware Manager**.

6-1-14. Click **OK** to close the session.

6-1-15. Power **OFF** the board.

6-1-16. Close the **Vivado** program by selecting **File > Exit** and click **OK**.

Run the Tools in Batch Mode Using Tcl Script

Step 7

7-1. Open a Vivado 2013.3 Tcl Shell window, Change the directory to **c:\xup\digital\sources\tutorial** (using **cd: /xup/digital/sources/tutorial** command). Run the tools in a batch mode using the provided tcl script file by executing the following command.

```
source tutorial_tcl_with_sim.tcl
```

7-1-1. Select **Start > All Programs > Xilinx Design Tools > Vivado 2013.3 > Vivado 2013.3 Tcl Shell** to open the Tcl shell.

7-1-2. In the Tcl prompt window, change the working directory to **c:\xup\digital\sources\tutorial** by executing the following command.

```
cd c:/xup/digital/sources/tutorial
```

7-1-3. Run the provided Tcl script in the batch mode by executing the following command

```
source tutorial_tcl_with_sim.tcl
```

The tools will be run and various directories will be created.

The Tcl script file is shown below.

```

1 set outDir ../../labs/tutorial/.
2 create_project tutorial_tcl_with_sim $outDir/tutorial_tcl_with_sim -part xc7a100tcsg324-1
3 add_files -norecurse ../../sources/tutorial/tutorial.v
4 import_files -fileset constrs_1 -force -norecurse ../../sources/tutorial/tutorial.xdc
5 update_compile_order -fileset sources_1
6 synth_design -rtl -name rtl_1
7 set_property package_pin U6 [get_ports {led[7]}]
8 set_property iostandard LVCMOS33 [get_ports {list {led[7]}]}]
9 set_property package_pin V5 [get_ports {swt[7]}]
10 set_property iostandard LVCMOS33 [get_ports {list {swt[7]}]}]
11 set_property target_constrs_file \
12 $outDir/tutorial_tcl_with_sim/tutorial_tcl_with_sim.srcs/constrs_1/imports/tutorial/tutorial.xdc [current_fileset -constrset]
13 save_constraints -force
14 set_property SOURCE_SET sources_1 [get_filesets sim_1]
15 import_files -fileset sim_1 -norecurse ../../sources/tutorial/tutorial_tb.v
16 update_compile_order -fileset sim_1
17 set_property runtime 200ns [get_filesets sim_1]
18 launch_xsim -simset sim_1 -mode behavioral
19 launch_runs synth_1
20 wait_on_run synth_1
21 launch_runs impl_1
22 wait_on_run impl_1
23 launch_runs impl_1 -to_step write_bitstream

```

Figure 37. The Tcl source file

Line 1 sets the output directory path

Line 2 creates the project directory `tutorial_tcl_with_sim` under the `c:\xup\digital\($outDir)` directory targeting Artix-7 100 part.

Line 3 adds the source file.

Line 4 imports the constraints files in which all except two I/O pins are defined

Line 5 sets the top module file

Line 6 executes the `rtl analysis` command

Lines 7 through 10 adds the missing I/O pins constraints

Lines 11 through 13 saves the constraints in the target xdc file located under the created project directory

Line 14 through 17 sets up, reads, and compiles the testbench

Line 18 runs the behavioral simulation

Line 19 through 22 synthesizes and implements the design

Line 23 generates the bitstream

Note that `wait_on_run` on lines 20 and 22 are essential as the tools run in multi-thread mode, and since the following command uses the results generated by the previous command, the previous command should be completed.

- 7-1-4. Close the Tcl Shell window when the execution is completed.
- 7-1-5. Using the Windows Explorer, browse through the generated project directory and verify that the bitstream file is generated in the `impl_1` directory.
- 7-1-6. Go to the `tutorial_tcl_with_sim.sim > sim_1 > behave` directory and view the content of the `tutorial_tb_behav.log` file. Note that it contains the simulator output.

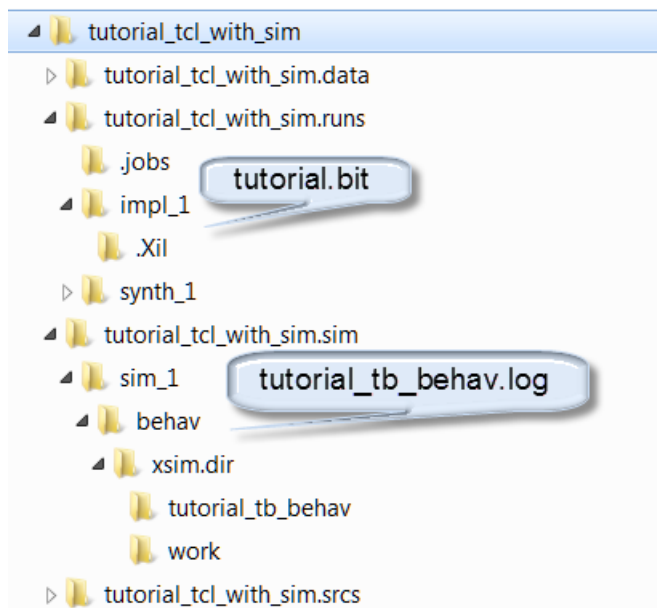


Figure 38. Generated directory structure

7-1-7. Close the command window.

Conclusion

The Vivado software tool can be used to perform a complete design flow. The project was created using the supplied source files (HDL model and user constraint file). A behavioral simulation was done to verify the model functionality. The model was then synthesized, implemented, and a bitstream was generated. The timing simulation was run on the implemented design using the same testbench. The functionality was verified in hardware using the generated bitstream. The design flow was also carried out in the batch mode using the provided Tcl script.