Power Design Manager

User Guide

UG1556 (v2020.2) November 19, 2021

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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
11/19/2021 Version 2020.2	
Initial release.	N/A

Table of Contents

Introduction

This document describes the power design manager (PDM) usage based on the Kria™ K26 system-on-module (SOM). The PDM enables you to estimate complete power requirements for the K26 SOM main 5V power supply and the six VCCO PL I/O bank supplies based on your application. For the current release, PDM 2020.2.2 only supports the Kria K26 production SOM K26C and K26I (commercial and industrial grade). Support for the KV260 Vision AI Starter Kit is planned for a future release of the PDM.

For technical support on the PDM, see Xilinx Support. Additional Kria SOM resources can be found here.

Additional documentation on power analysis for various platforms is as follows:

- *Kria K26 SOM Data Sheet* (DS987).
- When using the power design manager for estimating power based on the K26 SOM resource usage and toggle rates, see *Xilinx Power Estimator User Guide* (UG440) for additional details on how these inputs can be modeled.
- When using the Vivado® report power to estimate the power of an implemented design, see *Vivado Design Suite User Guide: Power Analysis and Optimization* (UG907).

  Note: The Vivado report power reports only the Zynq® UltraScale+™ MPSoC device power and it is not the same as the board level power estimated by the PDM.

Chapter 2

Installing Power Design Manager

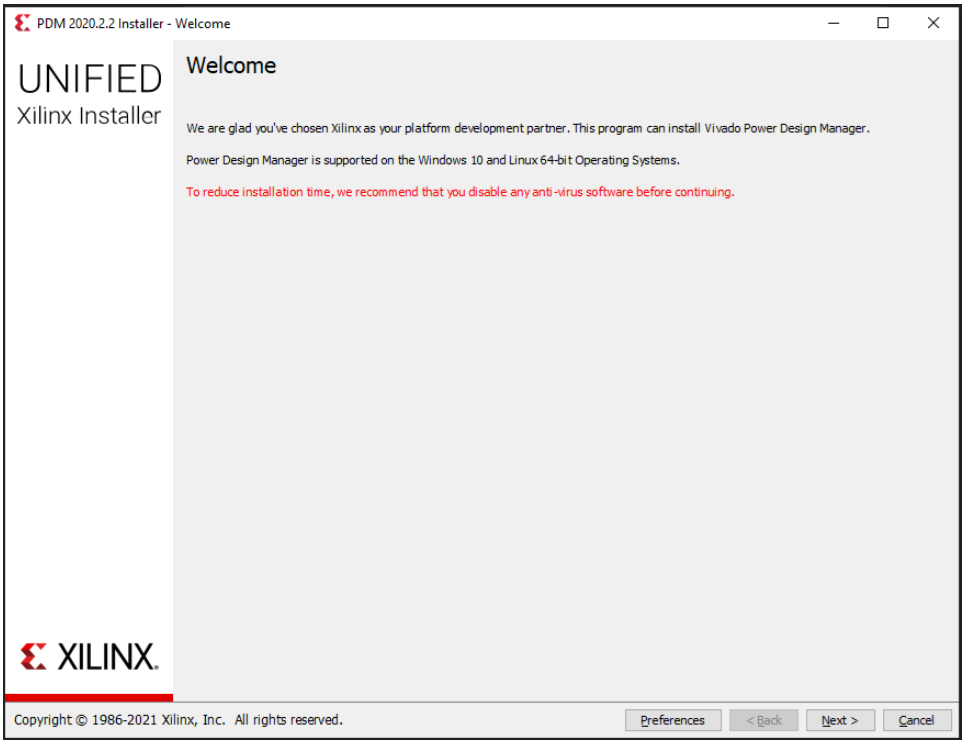
The standalone PDM installer is available on the Kria™ SOM Power and Thermal Resources page.

OS Requirement

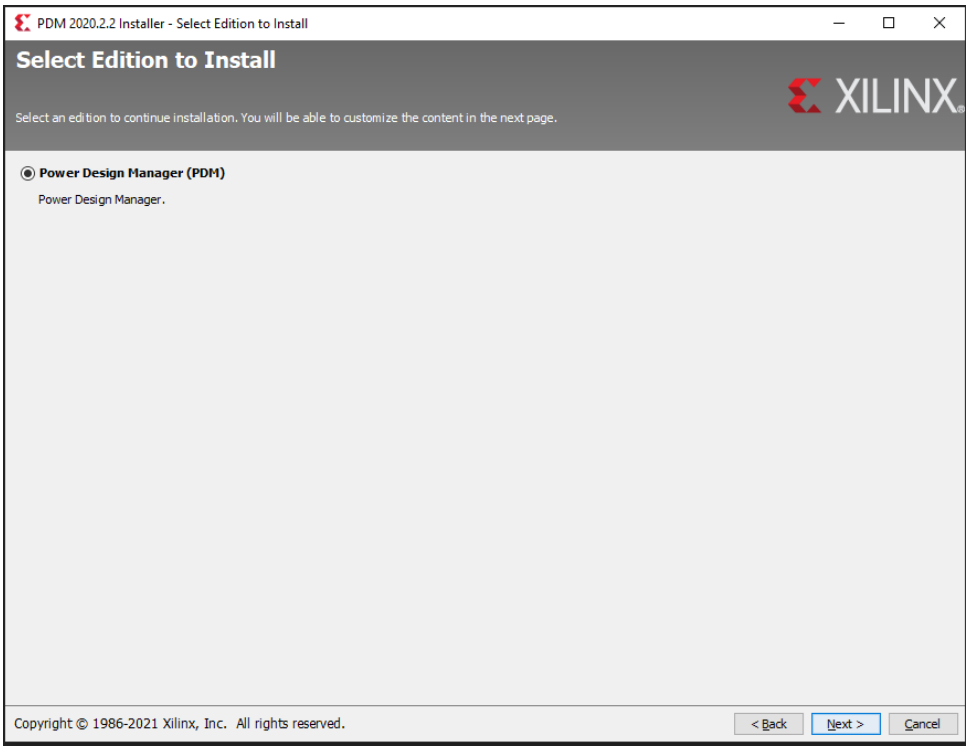
The PDM is currently supported on Windows 10 and Linux (CentOS7) operating systems only.

Installation Steps

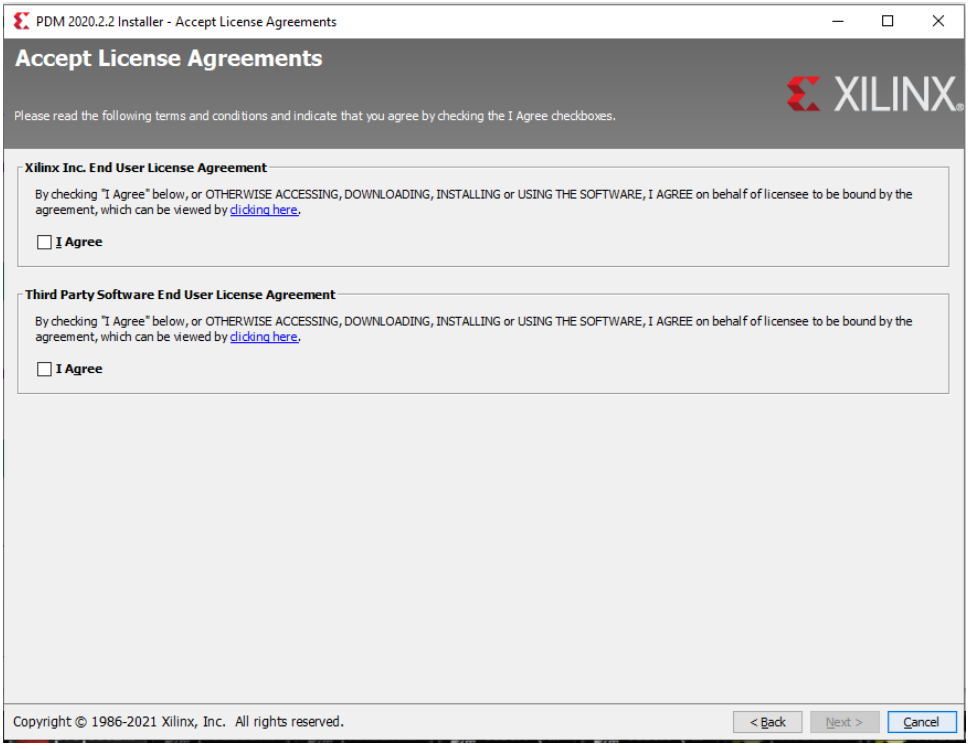
1. Download the installation file from Power and Thermal Resources page.
2. Launch the installer.
3. Follow the installation wizard. Click **Next**.



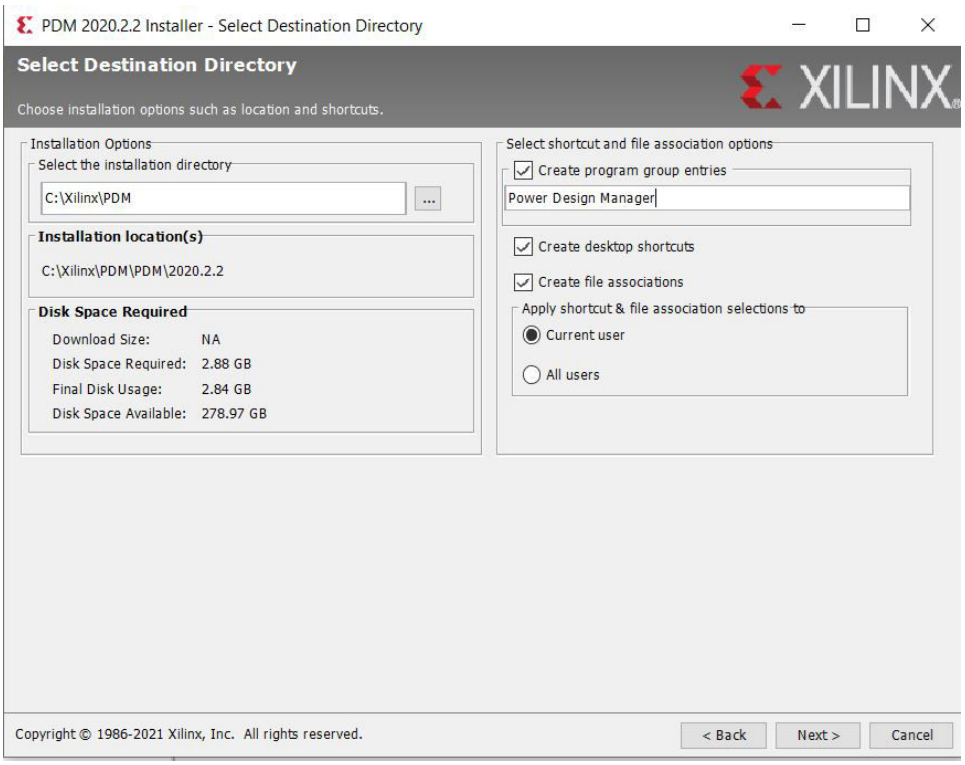
4. Click **Next**.



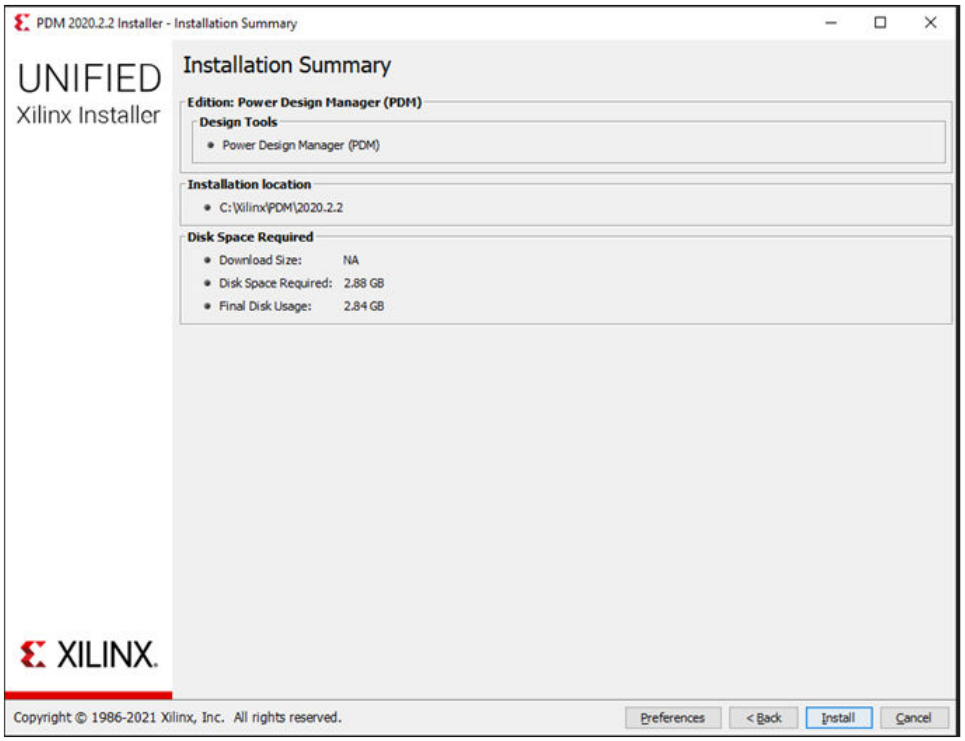
5. Agree to all the License Agreements and click **Next**.



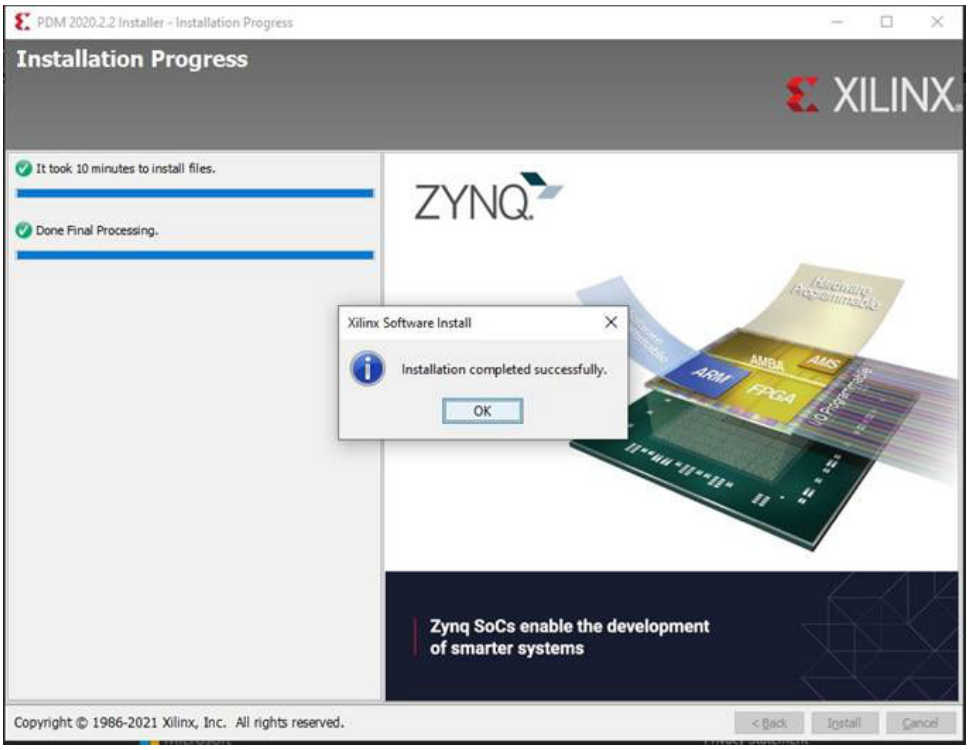
6. Enter the destination directory and shortcut option and click **Next**.



7. Review the Installation Summary page and click **Install**. It takes few minutes to complete the installation.



8. Click **OK** to finish the PDM installation.

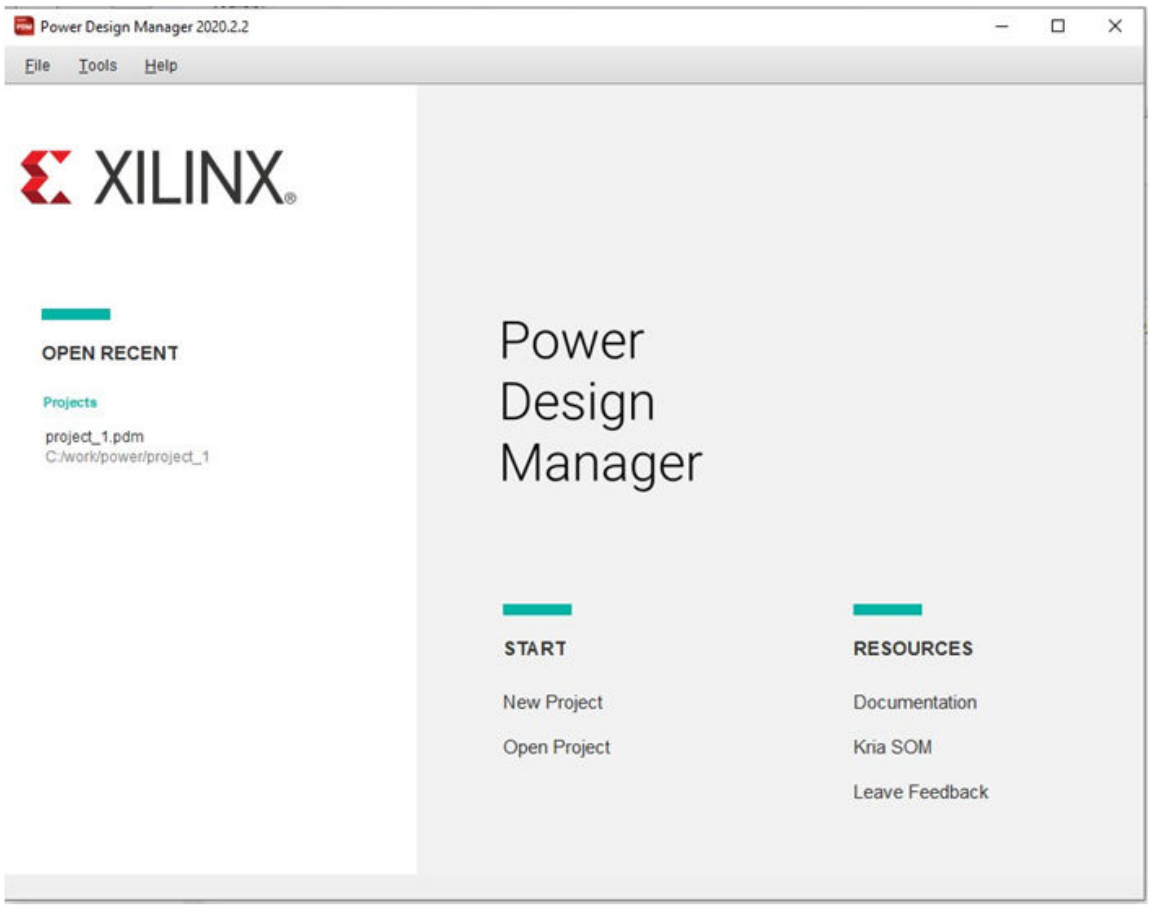

PDM 2020.2.2 Installer - Installation Progress
Installation Progress
XILINX
It took 10 minutes to install files.
Done Final Processing.
ZYNQ
Xilinx Software Install
Installation completed successfully.
OK
Zynq SoCs enable the development
of smarter systems
Copyright © 1986-2021 Xilinx, Inc. All rights reserved.
< Back
Install
Cancel

Chapter 3

Using Power Design Manager

When the PDM is installed on Windows 10/Linux OS, launch PDM from the Start menu or double-click the PDM desktop icon. The Getting Started screen appears when the PDM is launched.

Figure 1: **Power Design Manager**



Design Flows

The PDM supports two major design flows:

- **Manual estimation flow:** Use this flow when evaluating the Kria™ K26 SOM for total power based on the planned K26 design to be implemented.

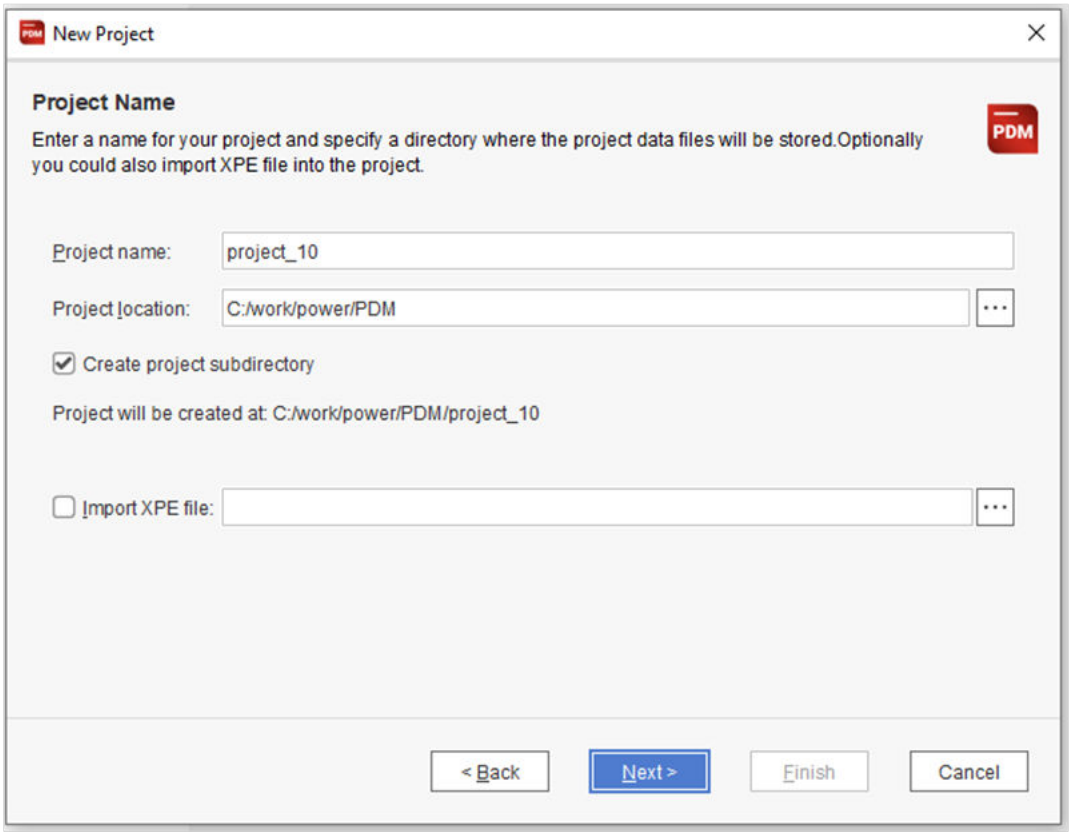
  In the manual estimation flow, PDM is used very similar to how the legacy device focused Xilinx® Power Estimator (XPE) tool is used is used. When starting a new PDM project, a new project wizard guides you through the project setup.

- **Import flow:** For this flow, you can import the file generated from Vivado® power into the PDM while creating a new project.

Creating New Project

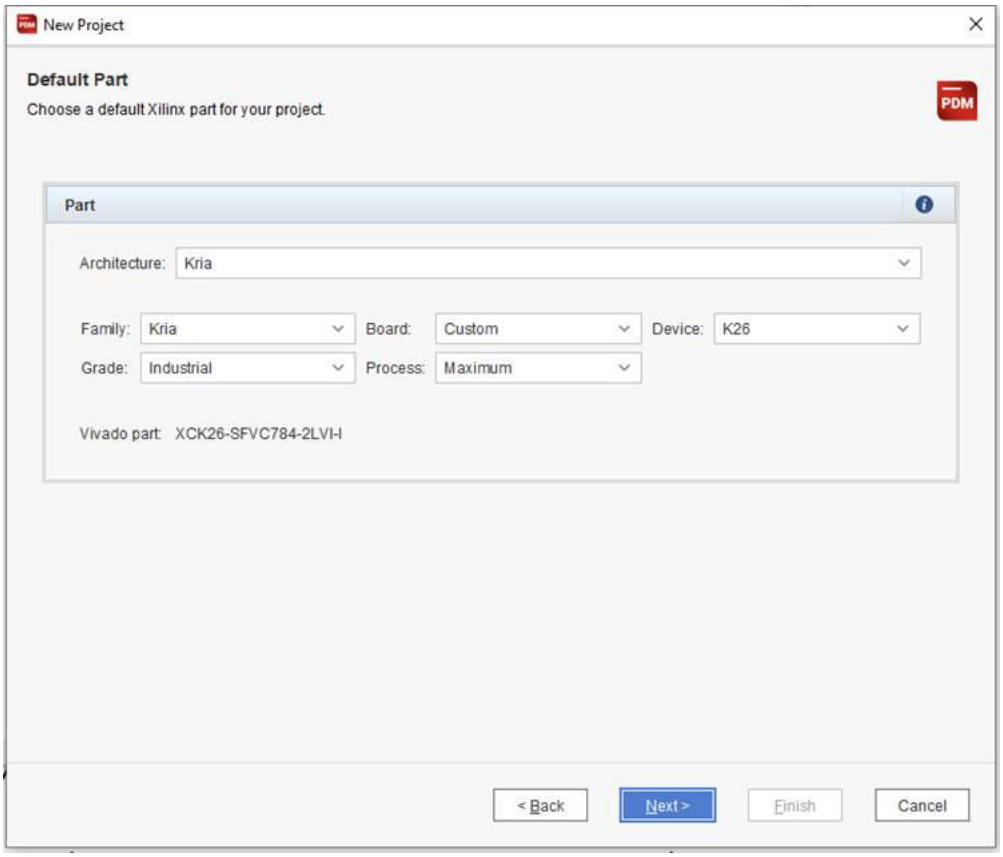
1. Click **New Project** on the Getting Started screen and click **Next**.
2. Enter the project name and project location.

   You can also select the `.xpe` file generated from Vivado for the import flow.



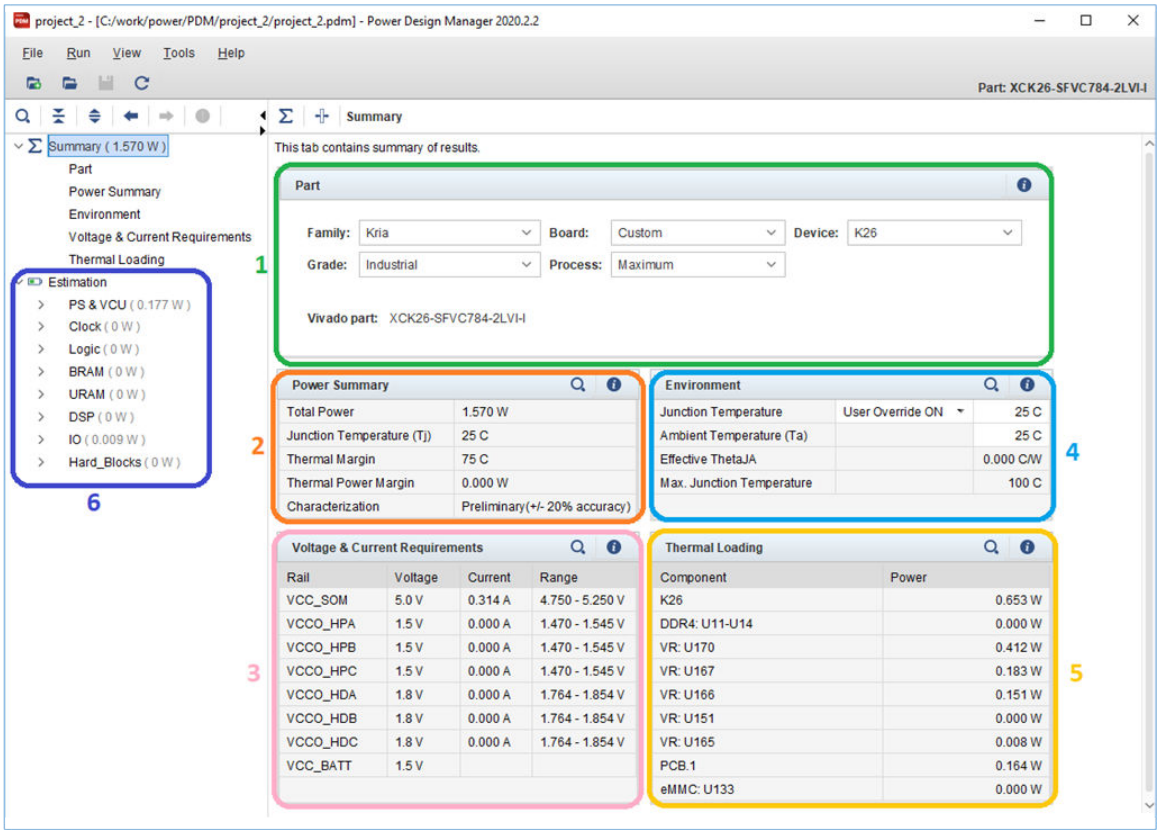
3. Clicking **Next** takes you to the part selection wizard. Select the temperature grade as commercial or industrial and process as typical or maximum and click **Next**.

   Note: If `*.xpe` import flow is selected, then architecture and device details are populated automatically from `*.xpe` file.



***Note*:** In the initial PDM 2020.2.2 release, only Kria SOM is supported and the K26C / K26I can be selected.

4. Click **Next** and the click **Finish** on the New Project Summary page. Your new project with all the default values will be created and ready to use.
5. Following is the summary sheet view in PDM after the new project is created.



On the left panel, there are summary and other blocks tab for the device. The Summary tab has following sections:

- **Part:** This panel is the summary of device selection and process setting for power estimation. You can change them in real time to see the impact on total power.

  TIP: *For worst-case power estimation, use the maximum process. This process applies only for MPSoC devices as remaining on-board components always have worst case estimation.*

- **Power Summary:** This read-only table shows the total power estimation, junction temperature (Tj) and margin based on the environment table.
- **Voltage & Current Requirements:** This table lists all the power rail requirements for the carrier card. Both current and voltage requirements are specified.

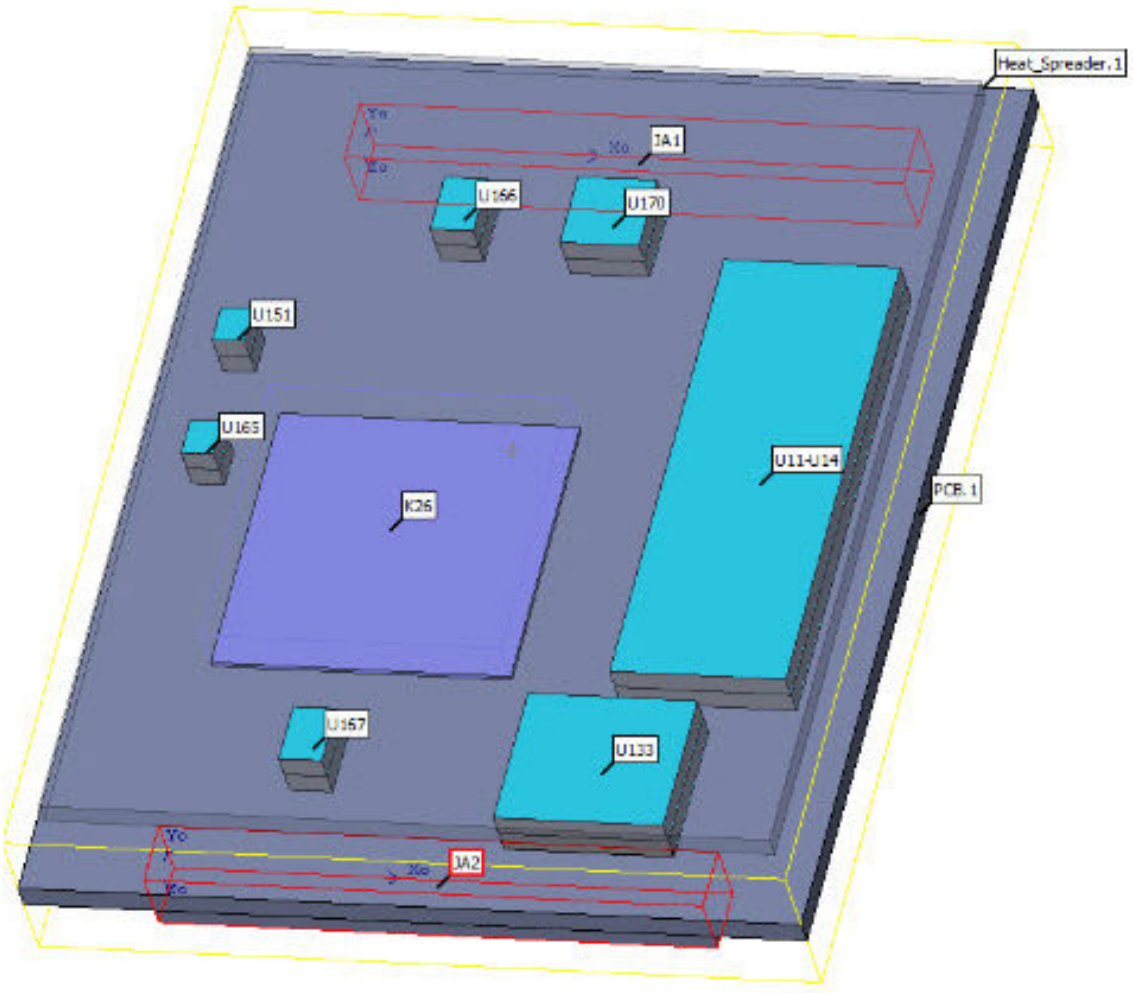
  TIP: *This is a departure for a typical power estimation where the MPSoC rails would be displayed. The SOM has a pre-connected power delivery and so PDM simply shows the required inputs. PDM also has DRCs to ensure that the estimated power does not exceed the current limits of the K26 SOM power delivery.*

- **Environment:** Allows the user to either force the Junction temperature to a fixed value or specify the maximum ambient and effective ThetaJA for the thermal solution (obtained from thermal simulation).

  RECOMMENDED: *Worst case junction temperature must be used until ThetaJA is obtained from thermal simulations. For more details see Kria K26 SOM Thermal Design Guide (UG1090).*

- **Thermal Loading:** This table lists out the power dissipated on the device, as well as on other external peripherals such as DDRs, power regulators, and boot devices available on SOM. The values in the thermal loading table must be used as inputs to a third-party thermal simulation.

Figure 2: **K26 SOM Flotherm Compact Model**

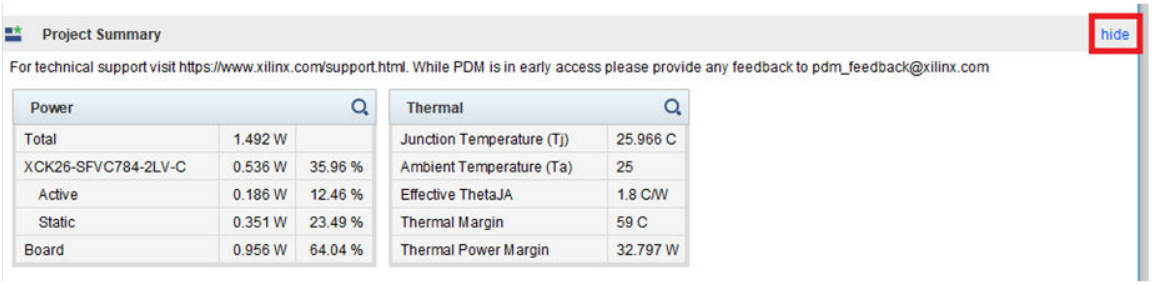


- **Estimation Section:** Under the estimation section on the left panel, there are device resources where you can provide input to the PDM about their usage, enable, and toggle rates.

At the bottom of the page, there is a Project Summary status which remains visible while viewing all of the PDM sheets. This information is added to provide a quick summary of the power distribution, thermal setting, and margin for the design.

Click on the **show/hide** button at the bottom right corner to hide this dialog box as needed.

Figure 3: **Project Summary Status**

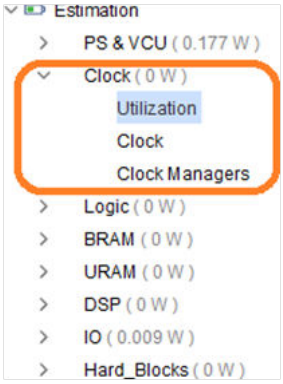


Creating Clock

When starting a manual estimation flow, it is recommended to create and generate the required clocks for the design. This will enable the clocks to be selected from the other resources tabs.

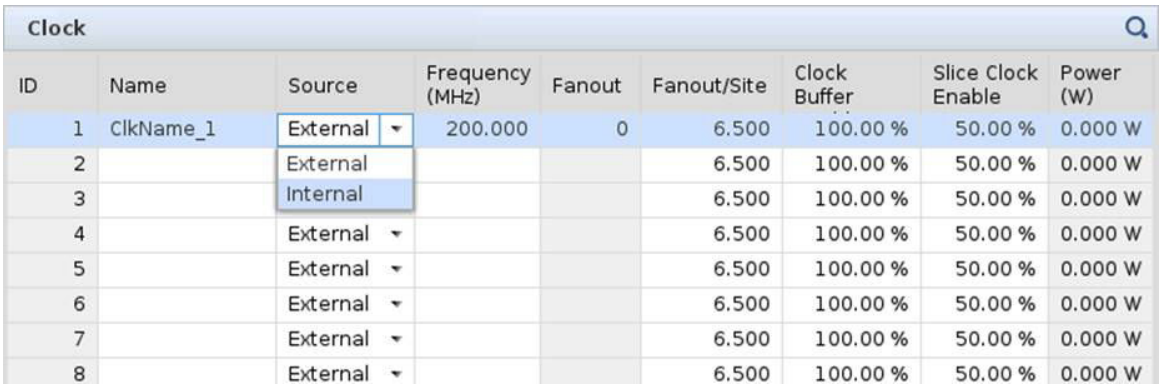
This clock creation can be performed using the Clock tab under the Estimation section.

Figure 4: **Estimation Section**



Fill in the details on the Clock tab to create a clock. Select if it is an external (coming from an I/O pin) or internal, from another block, such as the processing subsystem (PS) or a GT recovered clock for example.

Figure 5: **Clock Tab**

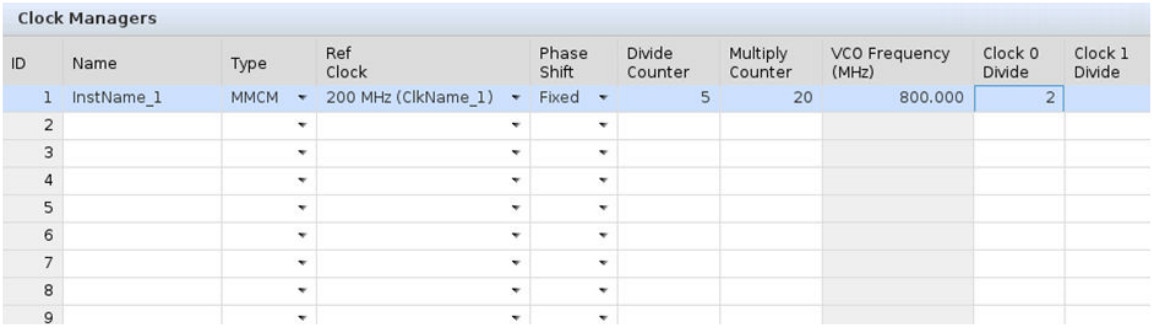


The fanout field for that clock will get populated automatically based on how many registers, block RAM, URAMs, and other resources are connected to that clock on their respective tabs.

POWER TIP: *Using this approach for the clock entry, PDM can more accurately estimate the clock power as the clock fanout is updated every time a clock is used in a Resources tab.*

If power estimation is required for an MMCM or PLL, these can be specified in the Clock Managers table on the Clock tab.

Figure 6: **Clock Managers**

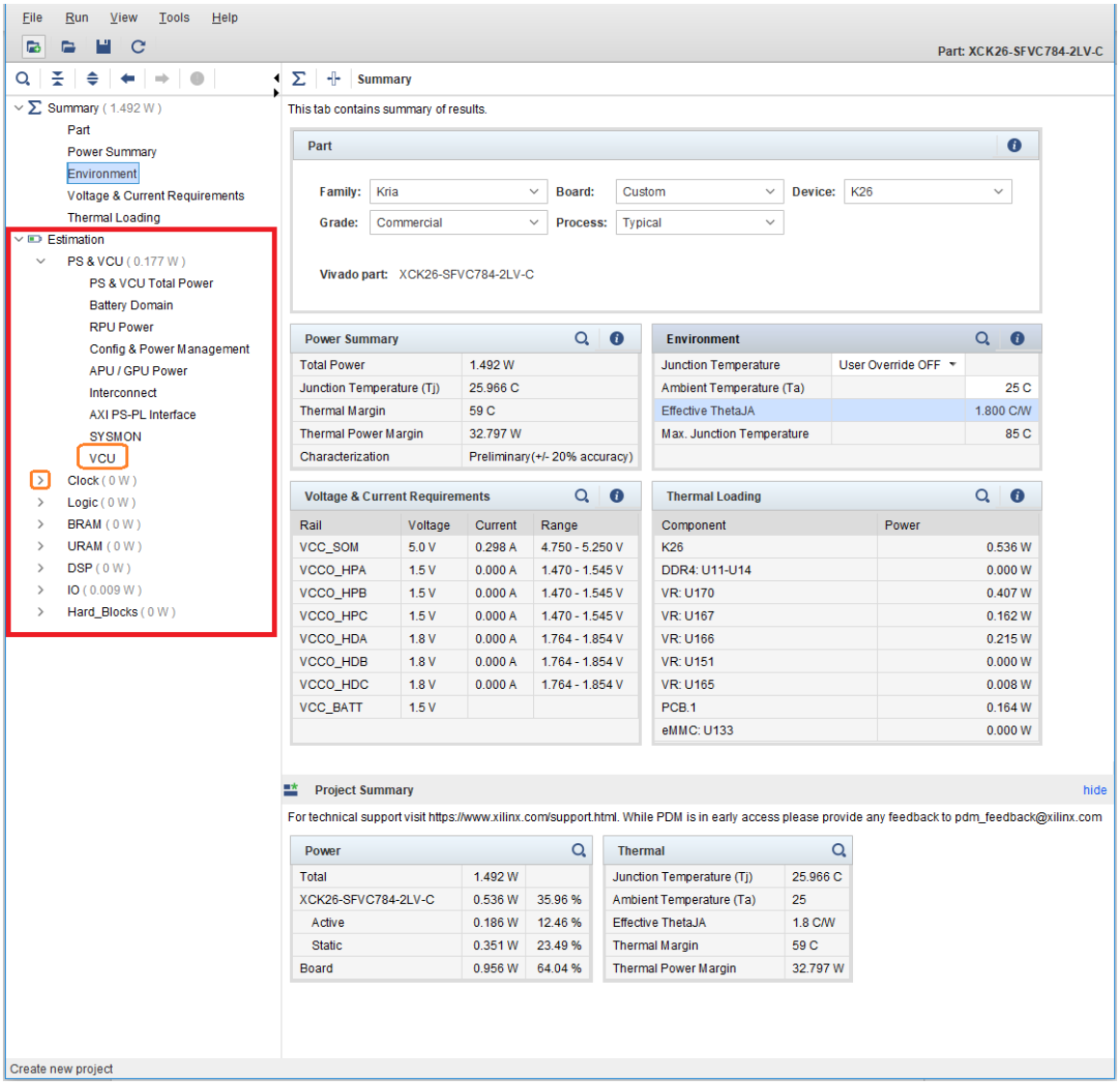


The reference clock is selected from one of the user-entered clocks in the Clock table. The multiply (M) and divide (D) can be specified as well as the output dividers. When this is entered, the output clock becomes available in the Clock table and is selectable on the other resource tabs such as Logic, DSP, URAM, block RAM, and I/O tabs to estimate the power of these blocks and the power of the clock network.

Power Design Manager Resource Tabs

After you have entered the required clock for the design, the remaining resources must be estimated. PDM displays the available resources in a tab on the slide view under the Estimation section.

Figure 7: **Power Design Manager Resources**



POWER TIP: *For fast navigation, each tab can be expanded using the > icon and you can jump to the desired table by selecting from the displayed list. For example, clicking to select VCU automatically jumps to the PS & VCU tab to display the VCU table.*

PDM organizes resources into the following categories:

- **PS & VCU :** This shows the Processing Subsystem with the MPSoC Processing Subsystem (PS) which has quad-core Arm® Cortex-A53 and dual-core Arm Cortex®-R5F along with a Mali 400 MP GPU. The Video Codec Unit (VCU) and System Monitors can be configured on this tab.
- **Clock:** As described above, this allows you to enter external and internal clocks as well as the PLL and MMCMs that will be used. All clocks generated on this tab can be selected from the other tabs to ensure the clock fanout and therefore power estimation is accurate.
- **Logic:** This tab allows you to enter the logic resource usage and toggle rates. The available K26 SOM resources and usage are displayed in the utilization table.

Figure 8: **Logic**

Utilization

Type	Avail	Used	Utilization
Registers	234240	100000	42.69 %
LUTs	117120	75000	64.04 %
Combinatorial	117120	50000	42.69 %
Shift Registers	57600	10000	17.36 %
Distributed RAMs	57600	15000	26.04 %

- **Block RAM and URAM:** Allows the block RAM and URAM utilization to be entered.
- **DSP:** The K26 SOM has up to 1248 DSP slices available. The utilization along with the clock rate and expected toggle can be entered here.
- **I/O:** The I/O tab, lists all of the available interfaces from both the processing subsystem (DDR4, PSMIO, and GTR) and the PL (PL IOs, and GTHs). The Power Summary & Utilization table shows the available interfaces based on the Kria K26 SOM and the 2 x 240 pin connectors to ensure that designs are kept within the K26 SOM limits.

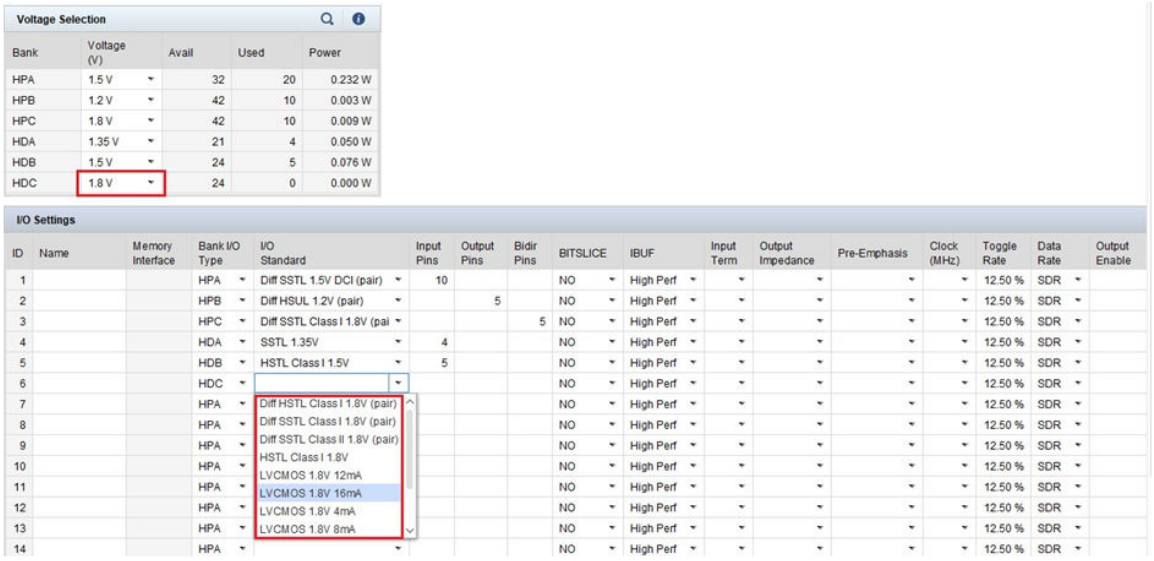
Figure 9: **IO Power Summary and Utilization**

Power Summary & Utilization

Type	Avail	Used	Utilization	Power
MIO	75	20	26.67 %	0.001 W
DDR4	9	0	0.00 %	0.009 W
GTR	4	0	0.00 %	0.006 W
GTH	4	2	50.00 %	0.373 W
PL GPIO	124	20	16.13 %	0.232 W
Total				0.620 W

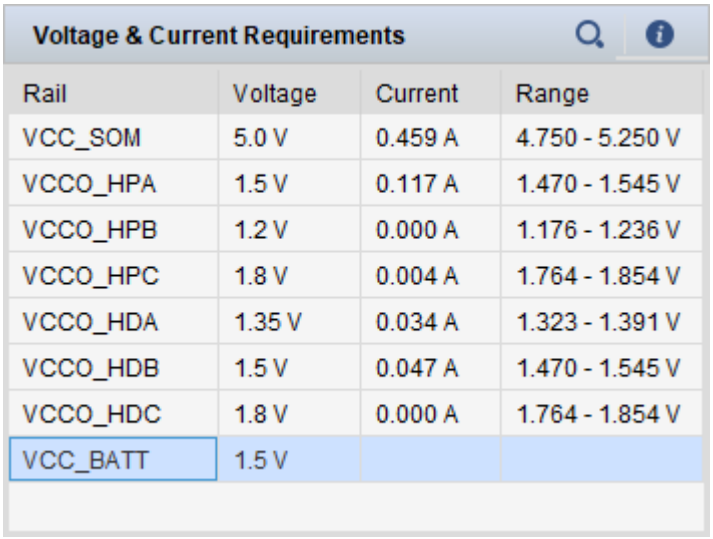
For the programmable logic (PL) I/Os, the Kria K26 SOM gives access to six banks 3x HD and 3x HP. PDM allows selection of both VCCO voltage for each of these banks as well as the supported I/O standards that correspond to the VCCO voltage selected.

Figure 10: **Programmable Logic for IOs**



The previous image shows that you can only select 1.8V IOSTANDARDs based on the 1.8V entered for the HDC VCCO. The power estimated for the PL I/Os will also be reflected as a carrier card current and voltage requirement as these VCCOs need to be provided by the user. The VCCO voltage range is also displayed.

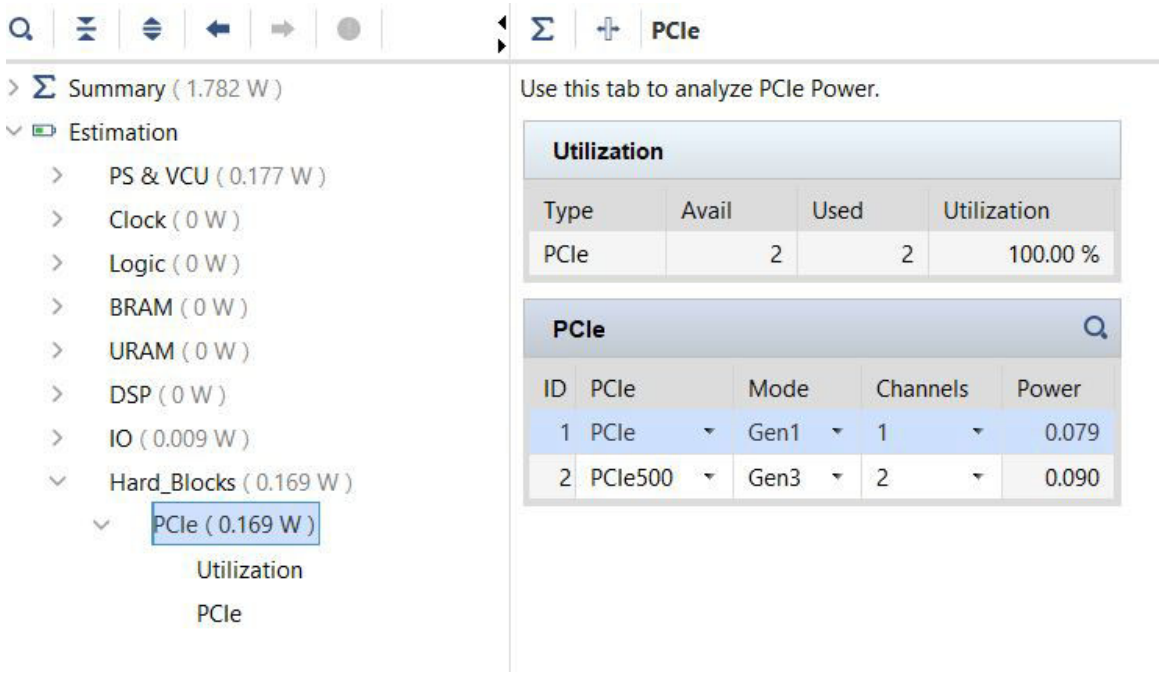
Figure 11: **Voltage and Current Requirements**



Rail	Voltage	Current	Range
VCC_SOM	5.0 V	0.459 A	4.750 - 5.250 V
VCCO_HPA	1.5 V	0.117 A	1.470 - 1.545 V
VCCO_HPB	1.2 V	0.000 A	1.176 - 1.236 V
VCCO_HPC	1.8 V	0.004 A	1.764 - 1.854 V
VCCO_HDA	1.35 V	0.034 A	1.323 - 1.391 V
VCCO_HDB	1.5 V	0.047 A	1.470 - 1.545 V
VCCO_HDC	1.8 V	0.000 A	1.764 - 1.854 V
VCC_BATT	1.5 V		

- **Hard Blocks:** This tab allows definition of the desired PCIe setup.

Figure 12: **PCIe Block Power Estimation**

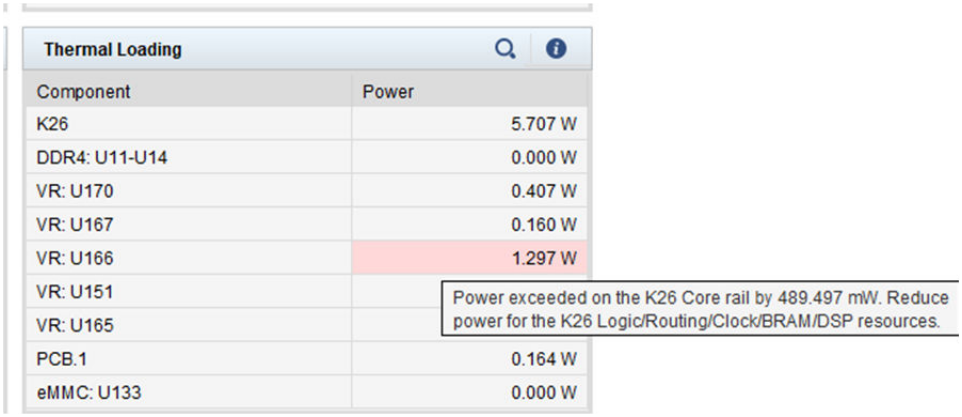


POWER TIP: *For drop-down selectable options, pressing the* ***Delete*** *key twice on the cell will reset it back to the default state.*

Kria K26 SOM Power Delivery

While the Kria™ K26 SOM comes with its own predefined power delivery network, power design manager has DRCs to ensure that each regulator does not exceed the maximum output current allowed. In the following figure, a DRC can be seen on U166. Hovering over it displays a tooltip suggesting to reduce power to bring the current within the maximum limit.

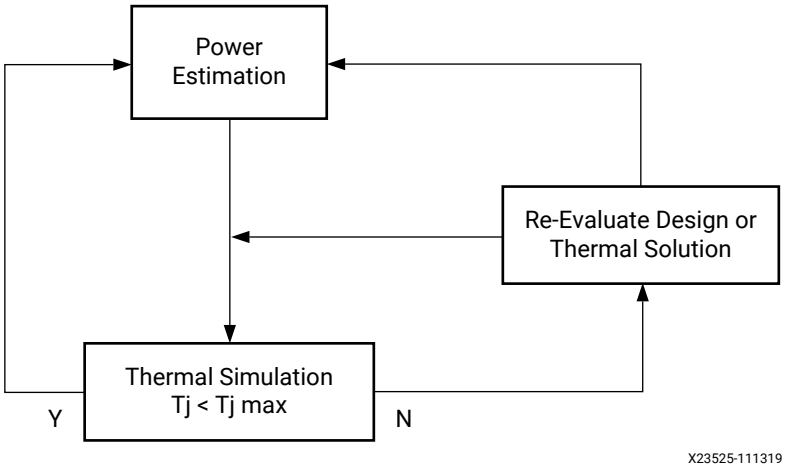
Figure 13: **Thermal Loading**



Thermal Simulation Results

After completing a thermal simulation and obtaining a Theta Ja (Θ_{JA}) value, power design manager estimation can be further refined using this information. When doing an initial thermal simulation, the worst case Tj should be assumed and the K26 SOM estimation can be refined once Θ_{JA} is calculated. For more information on this flow, see *UltraFast Design Methodology Guide for Xilinx FPGAs and SoCs* (UG949).

Figure 14: **Recommended Thermal Validation Flow**



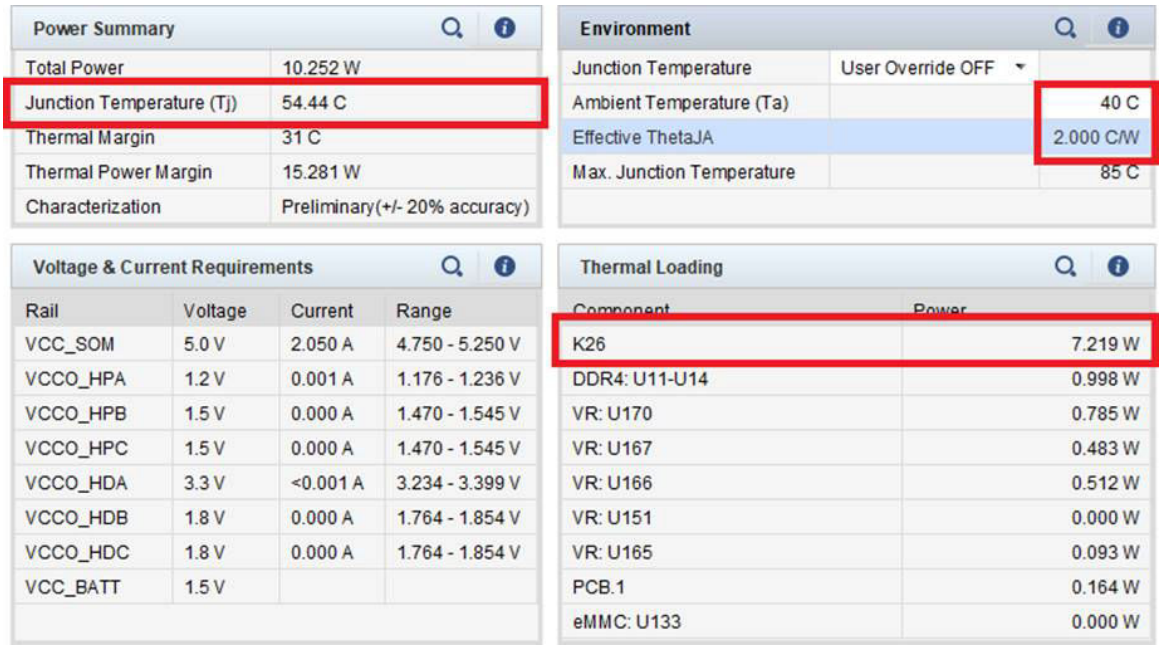
Θ_{JA} is a measure of how the junction temperature (Tj) raises above the ambient temperature (Ta) for every watt of power dissipated (Pd) in the device. The units are C/W and it is calculated using the following equation:

$$\Theta_{JA} = (Tj - Ta)/ Pd$$

In the Environment table, override the default Θ_{JA} with the Θ_{JA} from the thermal simulation results and specify the ambient temperature. PDM uses these values to calculate junction temperature and improve power estimation accuracy.

In the following example, Ta = 40°C with a Θ_{JA} of 2.0 C/W is entered when User Override OFF is selected. K26 power is estimated at 7.2W which results in an estimated Tj of 54.4°C. This ensures a more accurate static power estimate of the K26 Zynq® UltraScale+™ MPSoC device.

Figure 15: **Power Summary**



Power Summary

Total Power	10.252 W
Junction Temperature (Tj)	54.44 C
Thermal Margin	31 C
Thermal Power Margin	15.281 W
Characterization	Preliminary(+/- 20% accuracy)

Environment

Junction Temperature	User Override OFF	
Ambient Temperature (Ta)		40 C
Effective ThetaJA		2.000 C/W
Max. Junction Temperature		85 C

Voltage & Current Requirements

Rail	Voltage	Current	Range
VCC_SOM	5.0 V	2.050 A	4.750 - 5.250 V
VCCO_HPA	1.2 V	0.001 A	1.176 - 1.236 V
VCCO_HPB	1.5 V	0.000 A	1.470 - 1.545 V
VCCO_HPC	1.5 V	0.000 A	1.470 - 1.545 V
VCCO_HDA	3.3 V	<0.001 A	3.234 - 3.399 V
VCCO_HDB	1.8 V	0.000 A	1.764 - 1.854 V
VCCO_HDC	1.8 V	0.000 A	1.764 - 1.854 V
VCC_BATT	1.5 V		

Thermal Loading

Component	Power
K26	7.219 W
DDR4: U11-U14	0.998 W
VR: U170	0.785 W
VR: U167	0.483 W
VR: U166	0.512 W
VR: U151	0.000 W
VR: U165	0.093 W
PCB.1	0.164 W
eMMC: U133	0.000 W

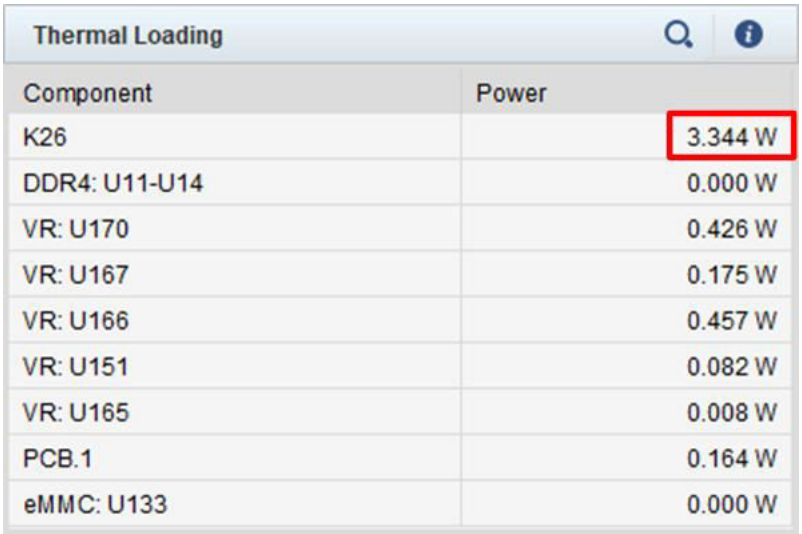
Constraining Vivado

When power estimation is completed by the PDM, the Vitis™ or Vivado® tools design should be properly constrained using Power Constraints. The following are considered the minimum requirements:

- `set_operating_conditions -design_power_budget <Power in Watts>`
- `set_operating_conditions -process maximum`
- `set_operating_conditions -ambient_temp <Max Supported by Application>`
- `set_operating_conditions -thetaja <Increase in Tj for every W dissipated C/W>`

TIP: *When constraining the Vivado tools design, the design power budget should be the K26 SOM power estimate and not the Kria™ K26 SOM 5V power estimate. Unlike PDM, Vivado report_power does not estimate the on-board components power.*

Figure 16: **Thermal Loading**

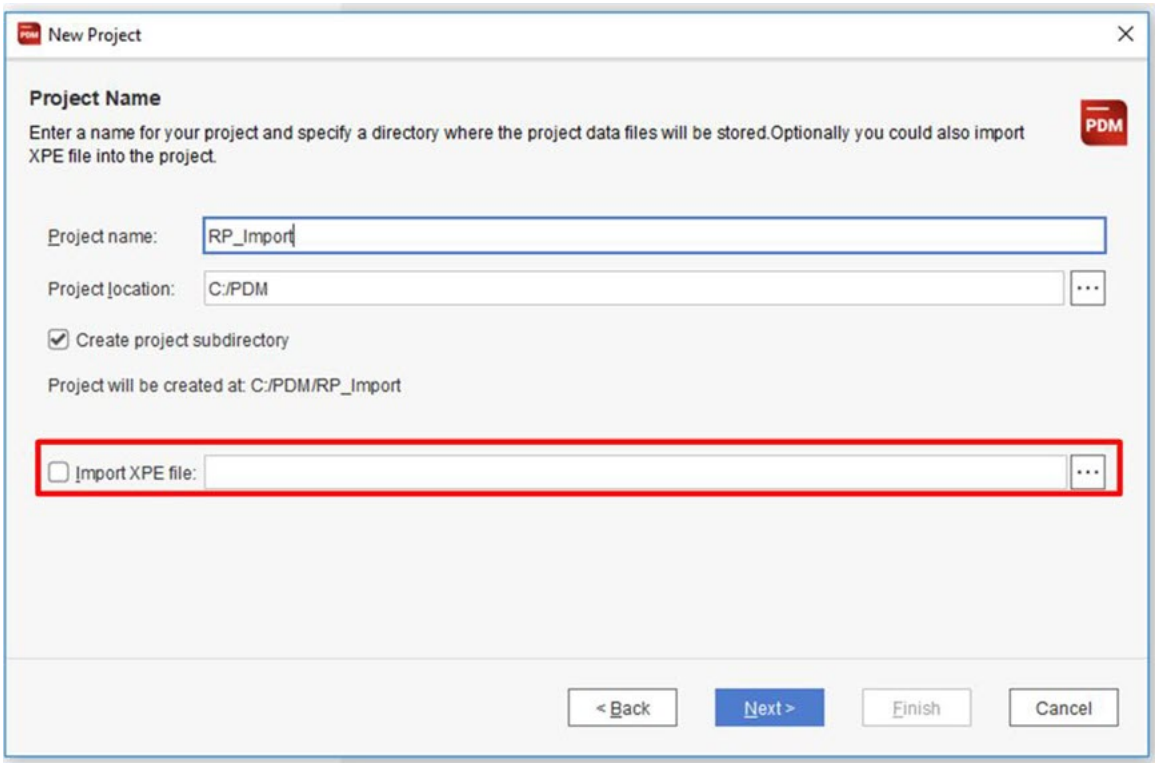


Report Power Import

While PDM estimates the total power of the Kria K26 SOM, Vivado® tools report power only estimates the K26 device power. To calculate total Kria K26 SOM power, export results from Vivado Report Power.

For details on how to run report power and generate the required `.xpe` file, see *Vivado Design Suite User Guide: Power Analysis and Optimization* (UG907). When creating a project in PDM, select the **Import XPE File** option and navigate to the `*.xpe` file as illustrated in following figure.

Figure 17: **Import XPE File**



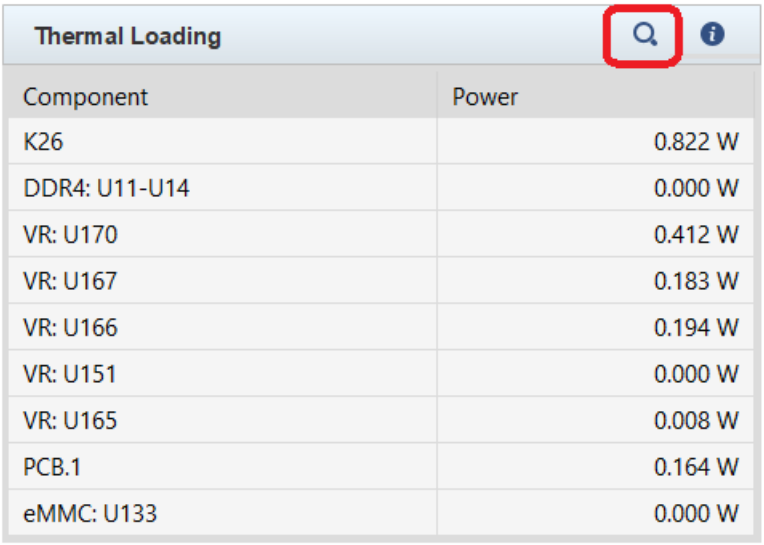
When imported, this updates the device resource usage based on the implemented design, the report_power toggle rates. PDM estimates power of the SOM resources external to the device and adds this to the device power to provide the total SOM power.

Additional Information

Search Within Table

For some of the tables which have many rows or columns, there is a search button added to quickly search the items in that table.

Figure 18: **Search Within Thermal Loading Table**

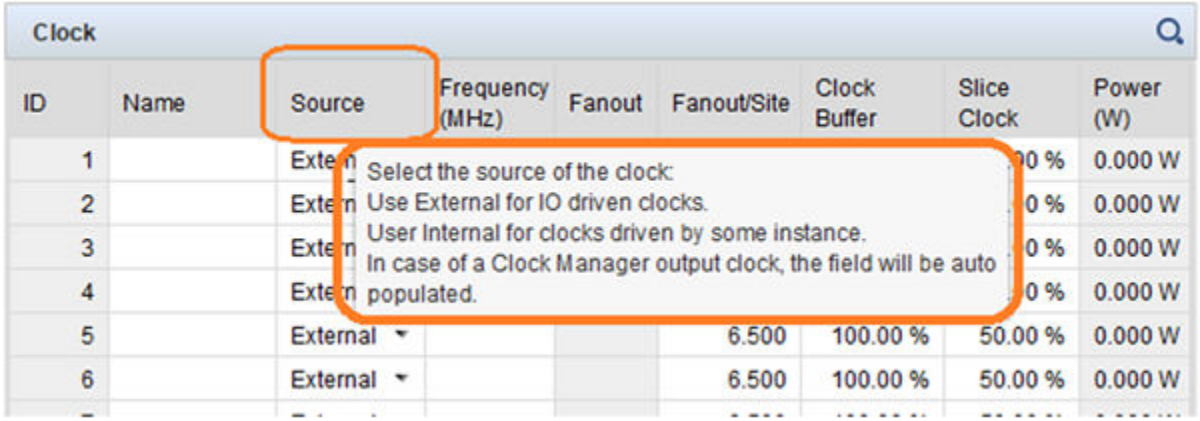


Tooltips

PDM has tooltips added to help users to quickly understand and get more information on each of the attributes. To view a tooltip, simply hover the cursor over the cell for the tooltip to display.

Here is an example of a tooltip for the clock source column:

Figure 19: **Tooltips**

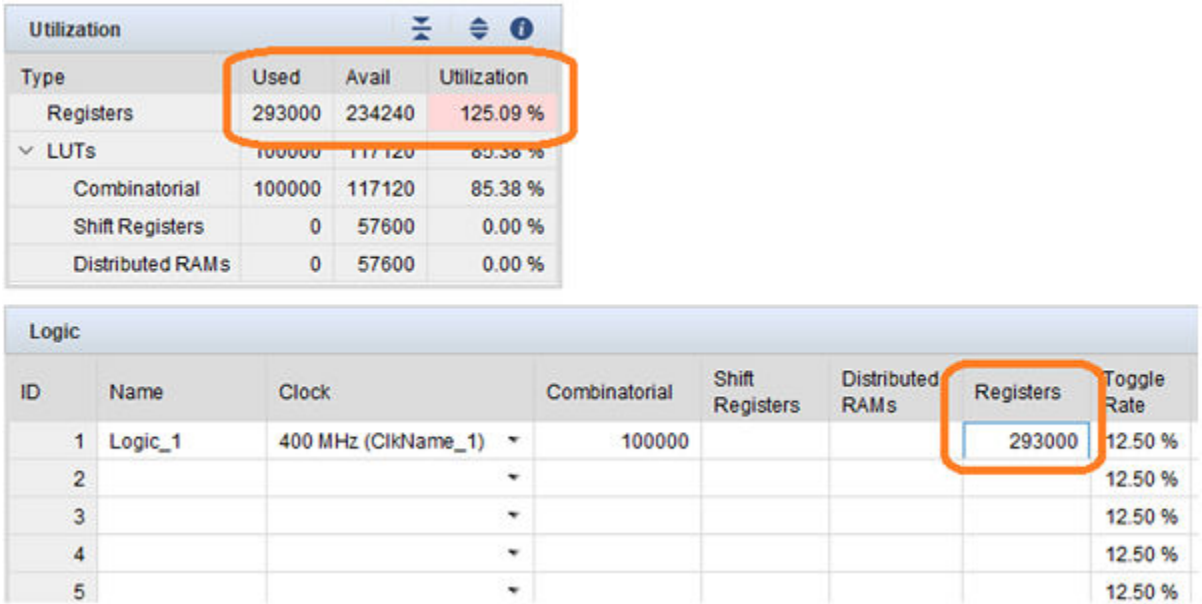


Design Rule Checks

The PDM user interface is designed to prevent invalid data entry but it is not possible to validate all the values. PDM performs design rule checks (DRCs) to bring attention to entries causing invalid results. DRCs run automatically as data is entered and calculations are updated.

A common DRC violation is resource over utilization. Following is an example showing a DRC violation on the logic sheet caused by the registers exceeding the available amount.

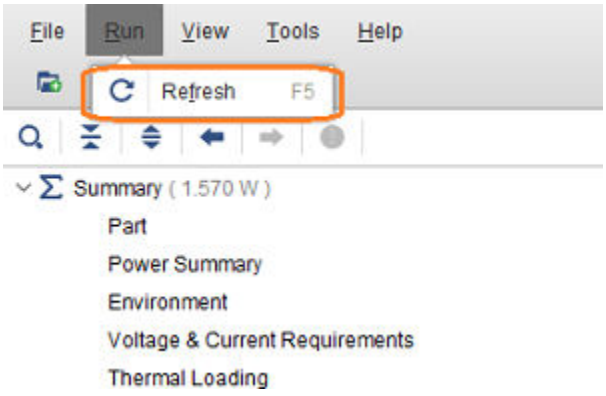
Figure 20: **Design Rule Checks**



Refresh

PDM performs incremental calculation and provide real-time update of power results as and when power numbers are populated. In few cases, when there are multiple inputs on different tab, there is also an option to perform Refresh or full calculation. This can be done either clicking the **Refresh** button on the menu bar or in the toolbar: **Run → Refresh**.

Figure 21: **Refresh**



Known Issues

Power Estimation

- **When the DDR interface is not used, there is no power associated with U11-U14:** When you add a DDR4 interface in the IO tab, the power for U11-U14 is estimated correctly. When the DDR4 interface is not used, the power dissipation for U11-14 is ~130 mW or 26 mA on the VCC_SOM 5V input.
- **Import Issues:** When importing a **.xpe** file, the following issues should be checked:
  - **Unassigned clocks and high fanout nets in the logic tab have no clocks:** When importing from Vivado® Report Power, logic that does not have an associated clock or any high fanout nets are listed separately. These typically are associated with the highest frequency clock in the design and typically there are very few of these resources. When importing to PDM, they will be listed in the logic tab but have no clocks associated with them as shown in the following figure:

Figure 22: **Logic Tab**

    To resolve, select the appropriate clock from the drop-down or create the required clock in the clock tab and select it for these entries. The power impact of these is typically very low <50 mW. To fully resolve this issue, you should refer to the implemented Vivado design and ensure that these nets are correctly constrained.

  - **Errors flagged in PDM:** Import issues are flagged as errors in the respective PDM tab, the most common import issue is the mismatch in the programmable logic IO settings. In the following figure, the IO tab has an error indicator beside it:

Figure 23: **Errors flagged in PDM**

In the IO tab the error is shown in the specific cell and can be corrected by selecting the correct setting:

Figure 24: **IO Tab**

IBUF Disable	Output Load(pF)	Signal Rate	Power (W)	External Termination	Offchip Vcco	User Comments
43.65 %		1199.761	0.004	None	-0.000	
80.73 %		25.000	0.014	None	-0.001	
0.00 %	0.000	0.051	0.000	100	0.000	
0.00 %	0.000	0.000	0.000	None	0.000	

- **DSP Slice Import Always has the Mult Enabled:** When importing a `.xpe` file, the MULT is also imported and this adds a small amount of power to the estimate, the range is up to 40 mW for every 100 DSP slices. This is dependent on the clock rate of the DSP slices and it is typically lower. The following figure shows an example of 100 DSP slices running at 450 MHz and 250 MHz, the power increase from the Mult being enabled is 40 mW@450 MHz → 18 mW@200 MHz.

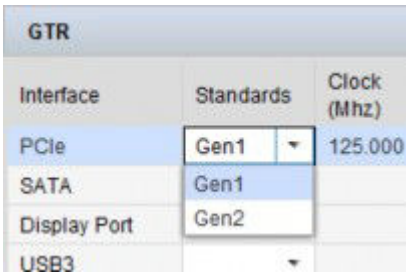
Figure 25: **DSP Slice Import**

DSP

ID	Name	DSP Slices	Clock	Toggle Rate	Mult Used ?	Mreg Used ?	Pre-add Used ?	Mtr/S	Power (W)	User Comments
1	DSP 100 Mult On	100	450 MHz (Cli	12.50 %	Yes	No	No	56.250	0.146	40mW power increase
2	DSP 100 Mult Off	100	450 MHz (Cli	12.50 %	No	No	No	56.250	0.106	
3				12.50 %	Yes	Yes	No	0.000	0.000	
4				12.50 %	Yes	Yes	No	0.000	0.000	
5	DSP 100 Mult On	100	200 MHz (CL	12.50 %	Yes	No	No	25.000	0.065	18mW power increase
6	DSP 100 Mult Off	100	200 MHz (CL	12.50 %	No	No	No	25.000	0.047	

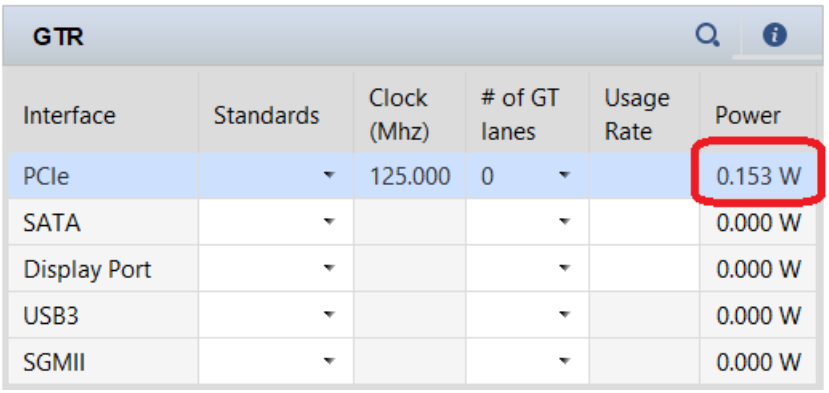
- **PDM does not allow deselection of an interface:** For example, when targeting PCIe® in the PS-GTR table, there is no empty option available to deselect an interface as shown in the following figure:

Figure 26: **PS-GTR Table**



Using the delete key twice removes an interface, however the power associated with it remains:

Figure 27: **Associated PS-GTR Power**



To correct this behavior, saving the PDM project and then reopening it allows you to remove power.

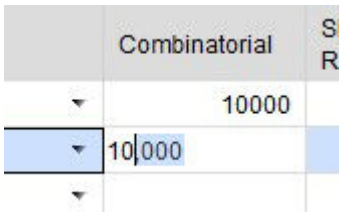
- **LVDS input supportability limitation:** LVDS input is currently supported only in 1.8V and 2.5V banks, though they can be placed in banks that are powered at voltage levels other than the nominal voltages required for the outputs of those standards (1.8V for LVDS outputs and 2.5V for LVDS_25 outputs) and based on the criteria mentioned in *UltraScale Architecture SelectIO Resources User Guide* (UG571). As a workaround, estimate power with LVDS 1.8 or LVDS 2.5 I/O standard in a 1.8V or 2.5V bank without DIFF_TERM setting.

Usability

- **Standard Excel type features and User tab are not supported:** PDM currently does not support multiple-row copy and paste or the standard Excel features where a cell can be based on a calculation of other cells. The User tab is currently not available.
- **Graphs and Snapshot tabs are not available:** These features will be added in a future release.

- **Quick estimate is not available:** This feature will be added in a future release.
- **Open recent design may not list the most recent PDM projects:** It will be fixed in a later version.
- **PDM does not allow the import of a .xpe file into an existing project:** For the initial release, a new project must be created to import a `.xpe` file.
- **Undo and redo options are not available:** Undo or redo option is not available currently. Delete option should be used instead.
- **Auto complete/auto correct issues:** When entering data, PDM tries to auto complete the entry. For example, if you have already entered 10000, and when you add 10 the next time, PDM tries to auto complete the entry to 10000 as shown in the following figure:

Figure 28: **Auto Complete Example**



Pressing spacebar or backspace prevents auto complete.

- **There are no export XDC constraints in the PDM:** The following options will be added in a later version of the PDM. Instead use the following constraints used to constrain Vitis™ or Vivado®:
  - `set_operating_conditions -design_power_budget <Power in Watts>`
  - `set_operating_conditions -process maximum`
  - `set_operating_conditions -ambient_temp <Max Supported by Application>`
  - `set_operating_conditions -thetaja <Increase in Tj for every W dissipated C/W>`

TIP: *When constraining the Vivado design, the design power budget should be the K26 SOM power estimate, it should not be the Kria K26 SOM 5V power estimate. The Vivado report power does not estimate the power of the on-board components as PDM does.*

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Xilinx Power Estimator User Guide* (UG440).
2. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
3. *Vivado Design Suite User Guide: Power Analysis and Optimization* (UG907).
4. *UltraFast Design Methodology Guide for Xilinx FPGAs and SoCs* (UG949).
5. *Kria K26 SOM Thermal Design Guide* (UG1090).
6. *Kria K26 SOM Data Sheet* (DS987).

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