

Vivado Design Suite Tutorial

Design Analysis and Closure Techniques

UG938 (v2020.1) September 4, 2020





Revision History

The following table shows the revision history for this document.

Section	Revision Summary						
09/04/2020 V	Version 2020.1						
General Updates	Updated design files.						
Lab 2: Increasing Design Performance Using Report QoR Suggestions	Updated the steps.Added Step 5: Accumulating Suggestions						
Lab 3: Running ML Strategies	Added lab.						



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Tutorial Overview

Introduction

This tutorial uses the Vivado[®] design rules checker (report_drc), clock domain crossing checker (report_cdc), and quality of results enhancer (report_qor_suggestions) to analyze example designs for issues, and shows you how to take corrective actions.

Tutorial Description

Lab 1 walks you through creating waivers for CDC, methodology, and DRC violations.

Lab 2 is a guide to using the report_qor_suggestions (RQS) command.

Note: The designs used in this tutorial are intended to exhibit issues for demonstration purposes, and should not be used as a reference for designs outside this tutorial.

Software Requirements

This tutorial requires that the 2020.1 Vivado[®] Design Suite software release or later is installed.

For a complete list of system and software requirements, see the Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973).

Locating Tutorial Design Files

- 1. Download the reference design files from the Xilinx[®] website.
- 2. Extract the ZIP file contents into any write-accessible location.

This tutorial refers to the location of the extracted ZIP file contents as <Extract_Dir>.



Lab 1

Setting Waivers with the Vivado IDE

Introduction

In the Vivado[®] Design Suite, you can use the waiver mechanism to waive clock domain crossing (CDC), design rule check (DRC), or methodology check violations. After a violation is waived, it is no longer reported by the <code>report_cdc</code>, <code>report_drc</code>, or <code>report_methodology</code> commands. Waived checks are also filtered out from the mandatory DRCs run at the start of the implementation commands, such as <code>opt_design</code>, <code>place_design</code>, and <code>route_design</code>. For more information, see this link in the Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906).

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IMPORTANT! The content of the waiver is built with the objects that exist when the waiver is created. However, if an instance referenced inside a waiver is replicated by Vivado[®], the replicated instance is automatically added to the waiver and saved in subsequent checkpoints and XDC.

This lab shows how to set waivers with the Vivado integrated design environment (IDE) using both menu commands and the Tcl Console. The lab focuses on CDC waivers, but the methods for waiving DRC and methodology violations are similar.

Step 1: Starting the Vivado IDE

This lab uses a Vivado design checkpoint (. dcp file), which is a snapshot of a design. When you launch the Vivado IDE using a design checkpoint, a subset of the Vivado IDE functionality is available.

TIP: To launch the Vivado Tcl Shell on Windows, select Start \rightarrow All Programs \rightarrow Xilinx Design Tools \rightarrow Vivado <version > \rightarrow Vivado <version > Tcl Shell.

1. From the command line or the Vivado Tcl Shell, change to the directory where the lab materials are stored:

```
cd <Extract_Dir>/src/Lab1
```

2. To start the Vivado IDE with the design checkpoint loaded, enter the following:

```
vivado my_ip_example_design_placed.dcp
```



0

TIP: You can disregard the critical warnings about the unbounded GT locations.

Step 2: Generating the CDC Report

In this step, you generate the CDC report to view the associated CDC violations.

- 1. Select **Reports** \rightarrow **Timing** \rightarrow **Report CDC**.
- 2. In the Report CDC dialog box, leave the default settings as-is, and click OK.

🝌 Report CDC 🛛 🗙
Report clock domain crossing (CDC) paths between clocks, even if set_false_path or set_clock_groups constraints have been applied.
Res <u>u</u> lts name: cdc_1
Clocks
<u>F</u> rom:
<u>I</u> o:
Report
Report from cells:
Waivers
Apply waivers
Report only waived paths
O Ignore all waivers
File Output
Export to file:
Overwrite Append
Options
Suspend message limits during command execution
Ignore command errors (quiet mode)
Command: report_cdc -name cdc_1
✓ Open in a new tab
Open in Timing Analysis layout
OK Cancel

The Summary (by clock pair) section of the CDC Report appears as follows.



Tcl Console Messages Timing ×											? _ 0	16
Q 素 ≑ C	★ ♦ C Summary (by clock pair)											۰
General Information	^	Severity ^1	Source Clock	Destination Clock	CDC Type	Exceptions	Endpoints	Safe	Unsafe	Unknown	No ASYNC_REG	
Summary (by clock pair)		Critical	my_ip_glblclk	my_ip_axi_aclk	No Common Primary Clock	False Path	2	1	1	0	C	ð
Summary (by type)		Oritical	my_ip_axi_aclk	my_ip_drpclk	No Common Primary Clock	False Path	2	0	2	0	C	ð
Summary (by waived endpoints)		Critical	my_ip_axi_aclk	my_ip_glblclk	No Common Primary Clock	False Path	942	12	351	579	185	5
V CDC Details (928)		Info	my_ip_drpclk	my_ip_axi_aclk	No Common Primary Clock	False Path	1	1	0	0	0	ð
my_ip_drpclk to my_ip_axi_aclk (1)		1 Info	input port clock	my_ip_drpclk	No Common Primary Clock	False Path	2	2	0	0	C	ð
my_ip_glblclk to my_ip_axi_aclk (2)		1 Info	my_ip_glblclk	my_ip_drpclk	No Common Primary Clock	False Path	6	6	0	0	0	ð
input port clock to my_ip_drpclk (2)		1 Info	my_ip_drpclk	my_ip_glblclk	No Common Primary Clock	False Path	2	2	0	0	0	0
my_ip_axi_aclk to my_ip_drpclk (2)	×.											
Report CDC - cdc_1 (928 violations)												

The Summary (by CDC type) section appears as follows.

Tcl Console Messages Timing ×											
Q X ♦ C Summary (by type)											
General Information	<u> </u>	Severity ^ 1	ID	Count	Description						
Summary (by clock pair)		Oritical	CDC-1	536	1-bit unknown CDC circuitry						
Summary (by type)		Oritical	CDC-4	4	Multi-bit unknown CDC circuitry						
Summary (by waived endpoints)		Oritical	CDC-10	187	Combinational logic detected before a synchronizer						
✓ CDC Details (928)		Oritical	CDC-11	2	Fan-out from launch flop to destination clock						
my_ip_drpclk to my_ip_axi_aclk (1)		Oritical	CDC-13	170	1-bit CDC path on a non-FD primitive						
my_ip_glblclk to my_ip_axi_aclk (2)		Oritical	CDC-14	5	Multi-bit CDC path on a non-FD primitive						
input port clock to my_ip_drpclk (2)		9 Warning	CDC-15	10	Clock enable controlled CDC structure detected						
my_ip_axi_aclk to my_ip_drpclk (2)		1nfo	CDC-3	9	1-bit synchronized with ASYNC_REG property						
my_ip_glblclk to my_ip_drpclk (6)		1 Info	CDC-9	5	Asynchronous reset synchronized with ASYNC_REG property						
my_ip_axi_aclk to my_ip_glblclk (913)	~										
Report CDC - cdc_1 (928 violations)											

Step 3: Waiving a Single CDC Violation

The $my_{ip_glblclk}$ to $my_{ip_axi_aclk}$ clock pair includes one Critical CDC-10 violation due to combinational logic on the CDC path. This step covers how to waive the CDC-10 violation.

Tcl Console Messages Timing ×								? _ 🗆
Q ¥ \$ C	Q H «	my_ip	_glbIclk to my_ip_axi_aclk	🖌 🌗 Critical warning (1)	Varning (0)	1) Hide Al		
General Information	Severity 🔨 1	ID	Description	Depth	Exception	Source (From)	Destination (To)	Category
Summary (by clock pair)	Critical	CDC-10	Combinatorial logic detected before a synchronizer	5	False Path	i_my_ip_supporysref_r_reg/C	i_my_ip_suppors_ff_reg[0]/D	Unsafe
Summary (by type)	Info	CDC-3	1-bit synchronized with ASYNC_REG property	5	False Path	i_my_ip_supporot_sync_reg/C	i_my_ip_suppos_ff_reg[0]/D	Safe
CDC Details (928)								
my_ip_drpclk to my_ip_axi_aclk (1)								
my_ip_glblclk to my_ip_axi_aclk (2)								
input port clock to my_ip_drpclk (2)								

1. To view a schematic of the violation, select the CDC-10 row in the CDC Report, and click the Schematic toolbar button 3.

Note: Alternatively, you can press **F4** to generate the schematic. However, using the toolbar button provides a more detailed schematic that includes all the levels of the downstream synchronizer.





- 2. To waive the violation, select the **CDC-10** row in the CDC Report, right-click, and select **Create Waiver**.
- 3. In the Create Waiver dialog box, enter a description, and click **OK**.

🝌 Create Wa	aiver	×
Create waiver f	for 1 cdc path	4
User:	Xilinx	\otimes
Description:	This is a safe CDC per review with the team	\otimes
Tags:		
Tcl Command	d Preview	
Q,		
create_waive	r -type CDC -id CDC-10 -from [get_pins i_my_ip_support_block/jesd204_i/inst/i_my_ip/i_tx/i_tx_cou	nters
?	OK Cano	> :el



IMPORTANT! A waiver tracks the date the waiver was added, the user that added the waiver, and a description of why the violation was waived. The date is automatically added by the system. The Tags field is an optional description or list of keywords that can be used for documentation purposes.

4. After the waiver is created, check the CDC Report.

To indicate that a waiver was created, the CDC-10 row is gray and disabled.

Note: Rows are only disabled in the Report CDC result window from which the waivers were created.



Tcl Console Messages Timing ×								? _	
Report is out of date because path waivers were characteristic and the second secon	anged. Rerun								
Q 素 ≑ C	<u>२</u> म -	≥_ my_ip_	glblclk to my_ip_axi_aclk	Y	🕐 🕛 Critical warning (1) 🛛 🖌 🕓	Varning (0) 🕑 📵 Info (1)	Hide All	•	
General Information	Severity ^1	ID	Description	Depth	Exception	Source (From)	Destination (To)	Category	
Summary (by clock pair)	Critical	CDC-10	Combinational logic detected before a synchronizer	5	False Path	i_my_ip_supportsysref_r_reg/C	i_my_ip_supportes_ff_reg[0]/D	Unsafe	
Summary (by type)	Info	CDC-3	1-bit synchronized with ASYNC_REG property	5	False Path	i_my_ip_supporot_sync_reg/C	i_my_ip_suppores_ff_reg[0]/D	Safe	
Summary (by waived endpoints)									
V CDC Details (928)									
my_ip_drpclk to my_ip_axi_aclk (1)									
my_ip_glblclk to my_ip_axi_aclk (2)									
input port clock to my_ip_drpclk (2)									
Report CDC - cdc_1 (928 violations)									

5. To see the impact of the CDC-10 waiver, select **Reports** → **Timing** → **Report CDC** to rerun Report CDC.

Note: When a waiver is created or deleted, you must rerun Report CDC, Report DRC, or Report Methodology to see the updated results.

6. See the CDC Report to view the updated information.

The differences from the previous Summary by clock pair and Summary by type sections are highlighted in red in the following figures.

Tcl Console Messages Timing ×												? _ 🗆 🖸
Q ≚ ≑ C	Q Summar	y (by clock pair)									•
General Information	Severity ^1	Source Clock	Destinatio	on Clock	CDC Type		Exceptions	Endpoints	Safe	Unsafe	Unknown	No ASYNC_REG
Summary (by clock pair)	Oritical	my_ip_axi_acl	k my_ip_dr	pclk	No Common Primary		False Path	2	0	2	0	0
Summary (by type)	Oritical	my_ip_axi_acl	k my_ip_gl	bicik	No Common Prin	nary Clock	False Path	942	12	351	579	185
Summary (by waived endpoints)	Info	my_ip_drpclk	my_ip_ax	i_aclk	No Common Prin	nary Clock	False Path	1	1	0	0	0
✓ CDC Details (928)	Info	my_ip_glblclk	my_ip_ax	i_aclk	No Common Prin	nary Clock	False Path	2	2	0	0	0
my_ip_drpclk to my_ip_axi_aclk (1)	Info	input port cloc	k my_ip_dr	pclk	No Common Prin	hary Clock	False Path	2	2	0	0	0
my_Ip_gibick to my_Ip_axi_ack (2)	 Info 	my_ip_glblclk	my_ip_dr	pclk	No Common Prin	nary Clock	False Path	6	6	0	0	0
my in axi ack to my in drock (2)	Info	my_ip_drpclk	my_ip_gl	bicik	No Common Prin	nary Clock	False Path	2	2	0	0	0
my_ip_akl_act to my_ip_dipcik (2)												
Report CDC - cdc_1 (928 violations) × Report	my ip, apackto my ip, anackto by important and the second se											
Tel Console Messages Tim	ina ×											
	•											
Q, X ♦ C		Q	Summa	ry (by typ	pe)							
General Information		Seve	erity 🗠 1	ID	Count	Desc	ription					
Summary (by clock pair)		9 C	Critical	CDC-1	536	1-bit unknown CDC circuitry						
Summary (by type)		<u> </u>	ritical	CDC-4	4	Multi-	Multi-bit unknown CDC circuitry					
Summary (by waived endpoints))	90	Critical	CDC-1	0 186	Com	binational	logic dete	cted b	efore a	synchror	izer
V CDC Details (928)		9 0	critical	CDC-1	1 2	Fan-o	out from la	unch flop t	o des	tination	clock	
my_ip_drpclk to my_ip_axi_	aclk (1)	9.0	ritical	CDC-1	3 170	1-bit (CDC path	on a non-f	D pri	mitive		
my_ip_glblclk to my_ip_axi_	_aclk (2)	9 0	ritical	CDC-1	4 5	Multi-	bit CDC p	ath on a no	on-FD	primiti	/e	
input port clock to my_ip_dr	pclk (2)	9 V	Varning	CDC-1	5 10	Clock	enable co	ontrolled C	DC s	tructure	detected	
my_ip_axi_aclk to my_ip_dr	pclk (2)	O Ir	nfo	CDC-3	10	1-bit s	synchroniz	ed with AS	SYNC	REGp	roperty	
my_ip_glblclk to my_ip_drp	afo.	CDC 0	-	Aouno	-	a a at a un a	-	o d with	ACYNIC	DEC property		
my_ip_axi_aclk to my_ip_gl	5	Asyno	unonousi	esetsynci	TOUL	eu with	ASTINC_	iteo property				
Depart CDC and a 1 (000 violation		M. CDC	odo 2 (0	20 viol-	tional							
Report CDC - cdc_1 (928 Violation	is) × R	eport CDC	- cac_z (9	za viola	uons) ×							

You can also view a summary with the list of waived endpoints.



Tcl Console Messages Timing x			
Q ¥ ≑ C	4	Q Sur	nmary (by waived endpoints)
General Information	^	ID	Waived Endpoints
Summary (by clock pair)		CDC-10	1
Summary (by type)			
Summary (by waived endpoints)			
V CDC Details (928)			
my_ip_drpclk to my_ip_axi_aclk (1)			
my_ip_glblclk to my_ip_axi_aclk (2)			
input port clock to my_ip_drpclk (2)			
my_ip_axi_aclk to my_ip_drpclk (2)			
my_ip_glblclk to my_ip_drpclk (6)			
my_ip_axi_aclk to my_ip_glblclk (913)	~		
Report CDC - cdc_1 (928 violations) × Re	port	CDC - cdc	_2 (928 violations) ×

The detailed section for the $my_{ip_glblclk}$ to $my_{ip_axi_aclk}$ CDC shows that the Critical CDC-10 was replaced with an Info CDC-3.



7. Select the new CDC-3 row, and click the Schematic toolbar button ¹. Double-click the **Q** pin of the output register to expand the schematic to match what is shown in the following figure.

The CDC path includes a 5-level synchronizer on the output of the selected destination register. This is the reason the CDC-10 was replaced with CDC-3 for this topology, as shown in the following figure.





IMPORTANT! By default, Report CDC only reports a single violation per endpoint and per clock pair. When multiple violations apply to the same endpoint, only the violation with the highest precedence is reported. Because CDC-10 has a higher precedence than CDC-3, only CDC-10 is reported when both CDC-10 and CDC-3 apply to the same endpoint. For more information on CDC rules precedence, see this link in the Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906).



TIP: To report all of the CDC violations for each endpoint regardless of the precedence rules, use the command line option *-all_checks_per_endpoint*. However, unsafe rules are not reported on a register if at least one safe rule on the same register is detected.

Step 4: Generating a Report for Waived Violations

You can generate a report for the CDC, DRC, or methodology check violations that were waived. This step shows how to generate a report for waived CDC violations using the Tcl Console as well as the Vivado IDE menu commands.

Generating a Text Report for Waived Violations

1. In the Tcl Console, enter:

report_cdc -waived

 In the CDC report, verify that a single CDC-10 violation is listed, because only one waiver was created.



Generating a Vivado IDE CDC Report for Waived Violations

- 1. Select Reports \rightarrow Timing \rightarrow Report CDC.
- 2. In the Report CDC dialog box, enable *Report only waived paths*, and click OK.
- 3. In the CDC Report, check the Summary (by clock pair) and CDC Details to verify that a single CDC-10 violation is listed.



Note: The icon next to the violation shows that the violation was waived *8*.

Tcl Console Messages Timing ×													? _ 0 0
Q ¥ ≑ C	Q Summa	ry (by clock pai	ir)										•
General Information	Severity ^1	Source Clock	Destination Clock	CDC Type	Exceptions	Endpoint	s Safe	Unsafe	Unknown	No ASYN	C_REG		
Summary (by clock pair)	Critical	my_ip_glblclk	my_ip_axi_aclk	No Common Primary Clock	False Path		1 0		(0	0		
Summary (by type)													
Summary (by waived endpoints)													
CDC Details (1)													
my_ip_glblclk to my_ip_axi_aclk (1)													
Report CDC - cdc_1 (928 violations) × Repo	rt CDC - cdc_2 (92	8 violations)	× Report CDC - cdc_	_3 (1 waived) ×									
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing ×	rt CDC - cdc_2 (92	8 violations)	× Report CDC - cdc_	3 (1 waived) ×									? _ 🗆 🖾
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q X ♦ C	irt CDC - cdc_2 (92)	8 violations)	× Report CDC - cdc_	3 (1 waived) ×		⊘ () Crit	tical warnin	ıg (1) [🖉 🕛 Warnii	ng (0) 🕑) 🚯 Info (0)	Hide	? _ 🗆 🖄
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q X ♦ C General Information	rt CDC - cdc_2 (92)	8 violations)	Report CDC - cdc_ lclk to my_ip_axi_aclk escription	3 (1 waived) ×	Depth Exc	♥ 🕕 Crit	tical warnin ource (Fron	ıg (1) (🛛 🕛 Warnii	ng (0) 🕑 Destination) 🚯 Info (0) n (To)	Hide	? _ Category
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q × Q General Information Summary (by clock pair)	Critical	8 violations)	Report CDC - cdc_ lclk to my_ip_axi_aclk escription combinational logic dete	3 (1 waived) ×	Depth Exc 5 Fals	♥ ● Crit ption So e Path i_1	tical warnin ource (From my_ip_sup	ıg (1) (1) portsysr	Warning 9 - Warning 9 - C	ng (0) 🕑 Destination i_my_ip_su) 🚺 Info (0) n (To) upportes_ff	Hide /	? _ Category Unsafe
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q ₹ € C General Information Summary (by clock pair) Summary (by type)	Q 2 292	8 violations)	X Report CDC - cdc_	3 (1 waived) ×	Depth Exce 5 Fals	Path i_1	tical warnin burce (Fron my_ip_sup	ng (1) (1 n) portsysn	2 🕒 Warnin ef_r_reg/C	ng (0) Destination i_my_ip_st) 🚺 Info (0) n (To) upportes_ff	Hide /	? _ Category Unsafe
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q ₹ ♦ C General Information Summary (by kpc) Summary (by kpc) Summary (by valved endpoints) Summary (by valved endpoints)	Q 3 Severity 1 Scritical	8 violations)	Report CDC - cdc_ Iclk to my_ip_axi_aclk escription ombinational logic dete	3 (1 waived) ×	Depth Exc 5 Fals		tical warnin ource (Fron my_ip_sup	ıg (1) (1) port…sysri		ng (0) 🕑 Destination i_my_ip_st) 1 Info (0) n (To) upportes_ff	Hide /	? _ Category Unsafe
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q X ♦ C General Information Summary (by clock pair) Summary (by type) Summary (by valved endpoints) CDC Details (1)	Critical	8 violations)	Report CDC - cdc_	3 (1 waived) ×	Depth Exc 5 Fals	♥ ① Crit ption So e Path i_t	tical warnin ource (From my_ip_sup	ng (1) (n) portsysn	✓ ● Warnin af_r_reg/C	ng (0) 🕑 Destination i_my_ip_st) 1 Info (0) n (To) upportes_ff	Hide /	? _ Category Unsafe
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q X ♦ C General Information Summary (by topc) Summary (by type) Summary (by valved endpoints) × CDC Details (1) my, jp, giblick to my, jp, asi_acik (1) Timing asi_acik (1)	d C it CDC - cdc_2 (92) Q b it CDC - cdc_2 (8 violations)	Report CDC - cdc_	3 (1 waived) ×	Depth Exc 5 Fals	₽tion So e Path i_1	tical warnin nurce (Fron my_ip_sup	ng (1) (1 n) portsysn	O Warnin O Warnin O	ng (0) 🕑 Destination i_my_ip_st) () Info (0) n (To) upportes_ff	Hide /	? _ Category Unsafe
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q ₹ ♦ C General Information Summary (by clock pair) Summary (by valved endpoints) Summary (by walved endpoints) × CDC Details (1) my_ip_globick to my_ip_axi_acik (1) Messages Timing	rt CDC - cdc_2 (92) Q Severity ^1 ⊘ Critical	8 violations)	Keport CDC - cdc_	3 (1 waived) ×	Depth Exc 5 Fais	vertion So e Path i_t	tical warnin wurce (Fron my_ip_sup	ig (1) (1 1) portsysn	✓ ● Warnin af_r_reg/C	ng (0) Destination i_my_ip_st) 🗊 Info (0) n (To) upportes_ff	Hide /	? _ Category Unsafe
Report CDC - cdc_1 (928 violations) × Report Tcl Console Messages Timing × Q ₹ ♦ C General Information Summary (by clock pair) Summary (by pole) Summary (by valved endpoints) ∨ CDC Details (1) my_ip_glblckt to my_ip_asi_acik (1) my_ip_asi_acik (1)	rt CDC - cdc_2 (92) Q Severity ^1 ⊗ Critical	8 violations)	Report CDC - cdc_ Iclk to my_ip_axl_acik escription ombinational logic dete	3 (1 waived) ×	Depth Exci	✓ ● Criticity iption Sc Sc e Path i_1	tical warnin ource (Fron my_ip_sup	n) portsysr	Varnin	ng (0) 🕑 Destination i_my_ip_si) 🜒 Info (0) n (To) upportes_ff	Hide /	? – Category Unsafe

Step 5: Generating a Text Report with Details for Waived Violations

In this step, you generate text reports with additional details, including a list of all of the rules and all of the violations regardless of the waivers.

Generating a List of Rules with Waived Violations

1. In the Tcl Console, enter:

report_cdc -details -show_waiver

2. Verify that the my_ip_glblclk to my_ip_axi_aclk CDC-10 violation is waived and the two CDC-3 violations are not waived.

Note: In the text report, all of the rules are reported, whether they were waived or not. The Waived column indicates the status of the rule.

CDC Re	port										
ID	Severity	Count	Description				ς.				
CDC-1 CDC-3 CDC-4 CDC-9 CDC-10 CDC-11 CDC-13 CDC-14 CDC-15	Critical Info Critical Info Critical Critical Critical Critical Varning	536 10 4 5 186 2 170 5 10	I-bit winnow CDC circuitry I-bit winnow CDC circuitry Multi-bit winnow CDC circuitry Regurdrowaur seest winnorad with ROWC_REG pr Combinatorial logic distorted before a winnorad Bernour from Lanch Flop to destination ciock Bernour from Lanch Flop to destination ciock Multi-bit CDC path on a normFD primitive Clock enable controlled CDC structure detected	operty r							
ID CDC-10	Waived 1										
Source Destin CDC Ty	Clock: my_ ation Clock pe: No Comm	_ip_glb: <: my_ip non Prim	kclk ⊳_axi_aclk nary Clock								ļ
Row I	D Seve	erity l	lescription	Depth	Exception	Source (From)			Destination (To)	Waived	l
1 C 2 C 3 C	DC-3 Info DC-3 Info DC-10 Crit	b b tical (-bit synchronized with ASYNC_REG property -bit synchronized with ASYNC_REG property Combinatorial logic detected before a synchronizer	5 5 5	False Path False Path False Path	i_my_ip_support_b i_my_ip_support_ i_my_ip_support_b		s_32/got_sync_reg/C _32/got_sysref_r_reg/C s_32/got_sysref_r_reg/C	i_wy_ip_support_block/jesd204_i/inst/sync_tx_sync/syncstages_ff_reg[0]/D i_wy_ip_support_block/jesd204_i/inst/sync_tx_sysref_captured/syncstages_ff_reg[0]/D i_wy_ip_support_block/jesd204_i/inst/sync_tx_sysref_captured/syncstages_ff_reg[0]/D	N N Y	l



Generating a List of All Violations Regardless of the Waivers

1. In the Tcl Console, enter:

CDC Deserve

 \bigcirc

report_cdc -no_waiver

2. In the text report, verify that the table matches the original report from Report CDC before the CDC-10 waiver was created.

CDC Kepor	ι.								
Severity	Source Clock	Destination Clock	СДС Туре	Exceptions	Endpoints	Safe	Unsafe 	Unknown	No ASYNC_REG
Critical	my_ip_glblclk	my_ip_axi_aclk	No Common Primary Clock	False Path	2	1	1	0	0
Critical	my_ip_axi_aclk	my_ip_drpclk	No Common Primary Clock	False Path	2	0	2	0	0
Critical	my_ip_axi_aclk	my_ip_glblclk	No Common Primary Clock	False Path	942	12	351	579	185
Info	my_ip_drpclk	my_ip_axi_aclk	No Common Primary Clock	False Path	1	1	0	0	0
Info	input port clock	my_ip_drpclk	No Common Primary Clock	False Path	2	2	0	0	0
Info	my_ip_glblclk	my_ip_drpclk	No Common Primary Clock	False Path	6	6	0	0	0
Info	my_ip_drpclk	my_ip_glblclk	No Common Primary Clock	False Path	2	2	0	0	0
			•						

TIP: You can also generate a list of all violations regardless of the waivers from the Vivado IDE. Select **Reports** \rightarrow **Timing** \rightarrow **Report CDC**. In the Report CDC dialog box, enable **Ignore all waivers**, and click **OK**.

Step 6: Waiving Multiple CDC Violations

The my_ip_axi_aclk to my_ip_drpclk CDC includes two Critical CDC-11 violations. This step covers how to waive both CDC-11 violations simultaneously.

Tcl Console Messages Timing ×								? _ [0 6
Q <u>∓</u> ≑ C	Q H -	⊗ my_ip	_axi_aclk to my_ip_drpclk	xi_aclk to my_ip_drpclk					٥
General Information	Severity ^1	ID	Description	Depth	Exception	Source (From)	Destination (To)	Category	
Summary (by clock pair)	Oritical	CDC-11	Fan-out from launch flop to destination clock	5	False Path	i_my_ip_supporetch_reg[10]/C	i_my_ip_supportff_reg[0]/CLR	Unsafe	
Summary (by type)	Critical	CDC-11	Fan-out from launch flop to destination clock	5	False Path	i_my_ip_supporetch_reg[10]/C	i_my_ip_supportff_reg[0]/CLR	Unsafe	
Summary (by waived endpoints)									
V CDC Details (928)									
my_ip_drpclk to my_ip_axi_aclk (1)									
my_ip_glblclk to my_ip_axi_aclk (2)									
input port clock to my_ip_drpclk (2)									
my_ip_axi_aclk to my_ip_drpclk (2)									
	<u>.</u>								
Report CDC - cdc_1 (928 violations) × Report CD	C - cdc_2 (928 vi	plations)	×						

1. To waive the violations, select the **CDC-11** rows in the CDC Report, right-click, and select **Create Waiver**.



Tcl Console Messages Timing ×								? _	0 6
Q 素 ≑ C	Q 🔄 🔄 🗞 my_ip	_axi_aclk to my_ip_drpclk			🖌 🌗 Critical warning (2) 🛛 🖌	Warning (0)	🕑 🚯 Info (0) 🛛 Hi	de All	٥
General Information	Severity ^1 ID	Description	Depth	Exc	ception Source (From)	Destination	(To)	Category	
Summary (by clock pair)	Critical CDC-11	Fan-out from launch flop to destination clock	ş	Fo	los Dath i mu in aunnar atab raal10		nnortff_reg[0]/CLR	Unsafe	
Summary (by type)	Oritical CDC-11	Fan-out from launch flop to destination clock	5		Path Properties	Ctrl+E	ortff_reg[0]/CLR	Unsafe	
Summary (by waived endpoints)			·		Elide Setting	,	•		
V CDC Details (928)				٠.	Highlight	,			
my_ip_drpclk to my_ip_axi_aclk (1)					Linbiabliabt				
my_ip_glblclk to my_ip_axi_aclk (2)				~	onnightight				
input port clock to my_ip_drpclk (2)				\otimes	Mark	,			
my_ip_axi_aclk to my_ip_drpclk (2)					Unmark				
my_ip_glblclk to my_ip_drpclk (6)				Н	Schematic				
my_ip_axi_aclk to my_ip_glblclk (913)					View Path Report				
my_ip_drpclk to my_ip_glblclk (2)					Report Timing on Source to Destination				
					Pot Maximum Dalay				
					Set maximum Delay				
					Set Bus Skew	1			
				2)	Create Waiver				
				-	Export to Spreadsheet				
Report CDC - cdc_1 (928 violations) × Report CDC	C - cdc_2 (928 violations)	×							

2. In the Create Waiver dialog box, enter a description, and click **OK**.

🝌 Create Wa	aiver X
Create waivers	for 2 cdc paths
User:	Xilinx
Description:	Safe fanout. Circuitry has been reviewed
Tags:	
Tcl Command	1 Preview
Q	
create_waive create_waive	r -type CDC -id CDC-11 -from [get_pins {i_my_ip_support_block/jesd204_i/inst/i_my_ip_reset_block/stre r -type CDC -id CDC-11 -from [get_pins {i_my_ip_support_block/jesd204_i/inst/i_my_ip_reset_block/stre
<	>
?	OK Cancel

In the Timing Report, the two selected rows are disabled when the waivers are created.

Note: One waiver is created for each selected row. In this example, two waivers are created.

Severity \land 1	ID	Description	Depth	Exception	Source (From)	Destination (To)	Category
Critical	CDC-11	Fan-out from launch flop to destination clock	5	False Path	i_my_ip_suppotch_reg[10]/C	i_my_ip_supporff_reg[0]/CLR	Unsafe
Critical	CDC-11	Fan-out from launch flop to destination clock	5	False Path	i_my_ip_suppotch_reg[10]/C	i_my_ip_supporff_reg[0]/CLR	Unsafe

- 3. Select **Reports** → **Timing** → **Report CDC** to rerun Report CDC. In the Report CDC dialog box, make sure that *Report only waived paths* is unchecked, and click **OK**.
- 4. In the CDC Report, look at the my_ip_axi_aclk to my_ip_drpclk CDC.



The two Critical CDC-11 violations were replaced with two Info CDC-9 violations. Based on the CDC precedence rules, waiving CDC-11 unmasks CDC-9 for this circuit.

Tcl Console Messages Timing ×								? _ 🗆 🖸	
Q Imp_p_axi_acik to my_ip_drpclk Imp_p_axi_acik to my_ip_drpclk Imp_maxi_acik to my_ip_drpclk									
General Information	Severity ^ 1	ID	Description	Depth	Exception	Source (From)	Destination (To)	Category	
Summary (by clock pair)	Info	CDC-9	Asynchronous reset synchronized with ASYNC_REG property	5	False Path	i_my_ip_supporetch_reg[10]/C	i_my_ip_supportff_reg[0]/CLR	Safe	
Summary (by type)	Info	CDC-9	Asynchronous reset synchronized with ASYNC_REG property	5	False Path	i_my_ip_supporetch_reg[10]/C	i_my_ip_supportff_reg[0]/CLR	Safe	
Summary (by waived endpoints)									
V CDC Details (928)									
my_ip_drpclk to my_ip_axi_aclk (1)									
my_ip_glblclk to my_ip_axi_aclk (2)									
input port clock to my_ip_drpclk (2)									
my_ip_axi_aclk to my_ip_drpclk (2)									
my_ip_glblclk to my_ip_drpclk (6)									
my_ip_axi_aclk to my_ip_glblclk (913)									
my_ip_drpclk to my_ip_glblclk (2)									
Report CDC - cdc_1 (928 violations) × R	eport CDC - cdc	_2 (928 vic	olations) × Report CDC - cdc_3 (928 violations) ×						

- To view a schematic of the violation, select the CDC-9 row in the CDC Report, and click the Schematic toolbar button 3.
- 6. Verify that there is a 5-level synchronizer on the destination clock domain.



7. Compare the new Summary (by type) information with the information from the previous CDC Report.

In the updated CDC Report, the two CDC-11 violations are no longer listed. Instead, there are two new CDC-9 violations.

Tcl Console Messages Timing ×				
Q ¥ ≑ C	Q Summa	ry (by type)		
General Information	Severity ^1	ID	Count	Description
Summary (by clock pair)	Critical	CDC-1	536	1-bit unknown CDC circuitry
Summary (by type)	Critical	CDC-4	4	Multi-bit unknown CDC circuitry
Summary (by waived endpoints)	Critical	CDC-10	186	Combinational logic detected before a synchronizer
✓ CDC Details (928)	Critical	CDC-13	170	1-bit CDC path on a non-FD primitive
my_ip_drpclk to my_ip_axi_aclk (1)	Critical	CDC-14	5	Multi-bit CDC path on a non-FD primitive
my_ip_glblclk to my_ip_axi_aclk (2)	👴 Warning	CDC-15	10	Clock enable controlled CDC structure detected
input port clock to my_ip_drpclk (2)	1 Info	CDC-3	10	1-bit synchronized with ASYNC_REG property
my_ip_axi_aclk to my_ip_drpclk (2)	1nfo	CDC-9	7	Asynchronous reset synchronized with ASYNC_REG property
my_ip_glblclk to my_ip_drpclk (6)				
my_ip_axi_aclk to my_ip_glblclk (913)				
my_ip_drpclk to my_ip_glblclk (2)				
Report CDC - cdc_1 (928 violations) × R	eport CDC - cdc	_2 (928 viola	ations)	× Report CDC - cdc_3 (928 violations) ×

8. Look at the Summary (by waived endpoints) information.



In the updated CDC Report, there are three waived endpoints. This number is different from the number of waived violations (2), because CDC-11 is a multi-bit violation.



9. Generate different text reports and compare the results with previous reports.

For example, you can run the following Tcl commands:

report_cdc -details
report_cdc -details -waived
report_cdc -details -show_waiver
report_cdc -details -no_waiver

The following report was generated using the report_cdc -details -waived Tcl command and shows that three violations were waived.

CDC Report	
ID Severity Count Description	
CDC-10 Critical 1 Combinatorial logic detected before a synchronizer	
The life and	
10 0alveu	
CDC-11 2	
Source Clock; my_ip_glblclk	
CDC Type: No Connon Prinary Clock	
Row ID Severity Description Depth Exception Source (From)	Destination (To)
1 CDC-10 Critical Combinatorial logic detected before a synchronizer 5 False Path i_my_ip_support	/s_32/got_sysref_n_reg/C i_my_ip_support_block/jesd204_i/inst/sync_tx_sysref_captured/syncstages_ff_reg[0]/D
Source Clock: mg.jp.axi.aclk Bestination Clock: mg.jp.drpclk CDE Type: No Common Primary Clock	
Row ID Severity Description Depth Exception Source (From)	Destination (To)
1 CIC-11 Critical Fan-out from launch flop to destination clock 5 False Path i_my_ip_support_block 5 False Path i_my_ip_support_block	reg[10]/C i_ny_ip_support_block/i_jesd204_phy/inst/jesd204_phy_block_i/sync_rx_reset_data/xpm_cdc_async_rst_inst/arststages_ff_reg[0]/ClR xg[10]/C i_ny_ip_support_block/i_jesd204_phy/inst/jesd204_phy_block_i/sync_tx_reset_data/xpm_cdc_async_rst_inst/arststages_ff_reg[0]/CLR
I	

Step 7: Exporting Waivers

In this step, you export waivers with the write_waivers Tcl command.

Note: The XDC output file can be imported using the read_xdc or source Tcl commands.

1. To export the CDC waivers, enter: write_waivers -type cdc waivers.xdc.

TIP: Alternatively, because there are no DRC or methodology waivers, you can enter:

write_waivers waivers.xdc Of write_xdc -type waiver waivers.xdc.

2. Open the waivers.xdc file to view the three waivers.

 \bigcirc



Note: The following example is reformatted to better show the different command line options.

```
create_waiver -type CDC -id {CDC-10} -user "Xilinx" \
  -desc "This is a safe CDC per review with the team"
  -from [get_pins i_my_ip_support_block/jesd204_i/inst/i_my_ip/i_tx/
i_tx_counters_32/got_sysref_r_reg/C] \
  -to [get_pins {i_my_ip_support_block/jesd204_i/inst/
sync_tx_sysref_captured/syncstages_ff_reg[0]/D}] \
  -timestamp "<timestamp>" ;#1
create_waiver -type CDC -id {CDC-11} -user "Xilinx" \
  -desc "Safe fanout. Circuitry has been released"
  -from [get_pins {i_my_ip_support_block/jesd204_i/inst/
i_my_ip_reset_block/stretch_reg[10]/C}] \
  -to [get_pins {i_my_ip_support_block/i_jesd204_phy/inst/
jesd204_phy_block_i/sync_rx_reset_data/xpm_cdc_async_rst_inst/
arststages_ff_reg[0]/CLR}] \
  -timestamp "<timestamp>" ;#1
create_waiver -type CDC -id {CDC-11} -user "Xilinx" \
  -desc "Safe fanout. Circuitry has been released" \
  -from [get_pins {i_my_ip_support_block/jesd204_i/inst/
i_my_ip_reset_block/stretch_reg[10]/C}] \
  -to [get_pins {i_my_ip_support_block/i_jesd204_phy/inst/
jesd204_phy_block_i/sync_tx_reset_data/xpm_cdc_async_rst_inst/
arststages_ff_reg[0]/CLR}] \
  -timestamp "<timestamp>" ;#2
```

Step 8: Using the create_waiver Command

Waivers added from the Report CDC dialog box are created using the create_waiver command. You can view these commands as follows.

Note: You can use the create_waiver command line command for CDC, DRC, and methodology waivers. The options differ slightly depending on whether you are creating a CDC, DRC, or methodology waiver. For more information, including information on the different options, see the create_waiver command in the *Vivado Design Suite Tcl Command Reference Guide* (UG835).

- 1. Open the Vivado journal file (vivado.jou) to see the three distinct create_waiver commands issued by the Vivado IDE.
- 2. Scroll through the history of the Tcl Console to see the same three create_waiver commands.

TIP: The -from and -to options are used to specify the startpoints and endpoints. When a waiver is set from the Report CDC dialog box, both -from and -to are specified to match the exact violation. However, you can specify a CDC waiver using only the -from option or only the -to option, but more paths might be waived than expected.

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Step 9: Waiving Multiple CDC Violations

In this step, you waive multiple CDC violations simultaneously.

1. In the CDC Report, view the my_ip_axi_aclk to my_ip_glblclk CDC under CDC Details.

This crossing has five CDC-14 violations, which are multi-bit violations. The five CDC-14 violations all start from the same two register clock pins:

i_my_ip_support_block/jesd204_i/inst/tx_cfg_test_modes_reg[2:1]/C

TIP: You can sort the table by the column ID to more easily see the five CDC-14 violations.

cl Console Messages Timing x								? _ 🗆 🖸
Q ¥ ≑ C	• Q 片 *	my_ip_ax	ki_aclk to my_ip_glblclk		🕑 🕒 Critical	warning (901) 🛛 🚽 🕘 Warning (1	0) 🕑 🕄 Info (2) 🛛 Hide	All 🔅
General Information	∧ Severity	ID ^ 1	Description	Depth	Exception	Source (From)	Destination (To)	Category
Summary (by clock pair)	Warning	CDC-15	Clock enable controlled CDC structure detected	0	False Path	i_my_ip_supportmodes_reg[1]/C	i_my_ip_suppod_nls_r_reg/D	Safe
Summary (by type)	Oritical	CDC-14	Multi-bit CDC path on a non-FD primitive	0	False Path	i_my_ip_supportodes_reg[2:1]/C	i_my_ip_supp/TXDATA[2:1]	Unknown
Summary (by waived endpoints)	O Critical	CDC-14	Multi-bit CDC path on a non-FD primitive	0	False Path	i my ip supportodes reg[2:1]/C	i my ip supp/TXDATA[2:1]	Unknown
CDC Details (928)	O Critical	CDC-14	Multi-bit CDC path on a non-FD primitive	0	False Path	i my ip support odes reg[2:1]/C	i my ip supp/TXDATA[2:1]	Unknown
my_ip_drpclk to my_ip_axi_aclk (1)	O Critical	CDC-14	Multi-bit CDC path on a non-FD primitive	0	False Path	i my ip support odes reg[2:1]/C	i my ip supp/TXDATA[2:1]	Unknown
my_ip_glblclk to my_ip_axi_aclk (2)	O Critical	CDC-14	Multi-bit CDC path on a non-FD primitive	0	False Path	i my ip support odes reg[2:1]/C	i my ip supp/TXDATA[2:1]	Unknown
input port clock to my_ip_drpclk (2)	Oritical	CDC-13	1-bit CDC path on a non-FD primitive	0	False Path	i my ip supportmodes reg[2]/C	i my ip suppo T/TXCTRL2[0]	Unsafe
my_ip_axi_aclk to my_ip_drpclk (2)	O Critical	CDC-13	1-bit CDC path on a non-FD primitive	0	False Path	i my ip supportmodes reg[2]/C	i my ip suppoT/TXCTRL2[1]	Unsafe
my_ip_glbick to my_ip_drpck (6)	O Critical	CDC-13	1-bit CDC path on a non-FD primitive	0	False Path	i my ip supportmodes reg[2]/C	i my ip suppoT/TXCTRL2[3]	Unsafe
my_ip_axi_acik to my_ip_gloicik (913) my_ip_drocik to my_ip_gloicik (2)	9 Critical	CDC-13	1-bit CDC path on a non-FD primitive	0	False Path	i_my_ip_supportmodes_reg[1]/C	i_my_ip_suppST/TXDATA[0]	Unsafe

2. Because i_my_ip_support_block/jesd204_i/inst/ tx_cfg_test_modes_reg[*]/C matches five pins and you only need to target two of

those five pins, construct the list of startpoints as follows:

```
set startpoints [list \
   [get_pins i_my_ip_support_block/jesd204_i/inst/
tx_cfg_test_modes_reg[1]/C] \
   [get_pins i_my_ip_support_block/jesd204_i/inst/
tx_cfg_test_modes_reg[2]/C] \
   ]
```

3. To waive the five CDC-14 violations, use the create_waiver Tcl command with the -from option:

```
create_waiver -type {CDC} -id {CDC-14} -user {Xilinx} -desc {No more CDC
14!} -from $startpoints
```

- 4. From the Vivado IDE, select **Reports** \rightarrow **Timing** \rightarrow **Report CDC** to rerun Report CDC.
- 5. In the CDC Report, verify that the CDC-14 violations are no longer reported in the Summary section.



Tcl Console Messages Timing x					
Q 素 ⊜ C	Q Summa	ry (by type)			
General Information	Severity ^1	ID	Count	Description	
Summary (by clock pair)	Oritical	CDC-1	536	1-bit unknown CDC circuitry	
Summary (by type)	Oritical	CDC-4	4	Multi-bit unknown CDC circuitry	
Summary (by waived endpoints)	Oritical	CDC-10	186	Combinational logic detected before a synchronizer	
V CDC Details (923)	Oritical	CDC-13	170	1-bit CDC path on a non-FD primitive	
my_ip_drpclk to my_ip_axi_aclk (1)	Warning	CDC-15	10	Clock enable controlled CDC structure detected	
my_ip_glblclk to my_ip_axi_aclk (2)	Info	CDC-3	10	1-bit synchronized with ASYNC_REG property	
input port clock to my_ip_drpclk (2)	1 Info	CDC-9	7	Asynchronous reset synchronized with ASYNC_REG property	
my_ip_axi_aclk to my_ip_drpclk (2)	v				
Report CDC - cdc_1 (928 violations) × Re	port CDC - cdc_2	(928 violatio	ns) ×	Report CDC - cdc_3 (928 violations) × Report CDC - cdc_4 (923 violations)	×

6. To report only the waived violations, enter:

report_cdc -details -waived

The following figure shows the waived CDC violations in two different tables. The first table shows the 5 CDC-14 violations waived as multi-bit violations. The second table shows the 10 single-bit violations, calculated by multiplying the 5 multi-bit violations by 2 bits per multi-bit violation.

ID	Seve	rity Coun	t Description						
-000 -010 -010	10 Crit 11 Crit 14 Crit	ical ical ical	1 Combinatorial logic detected before a s 2 Fan-out from launch flop to destination 5 Multi-bit CDC path on a non-FD primitiv	ynchron _clock e	izer				
ID CDC- CDC- CDC- CDC- Sour Dest	Waiv 10 11 14 ce Clock ination	ed 1 2 10 : my_ip_gl Clock: my_ Common Pr	blclk ip_axi_aclk inaru_Clock						
Row	ID	Severity	Description		Dep	pth E	Exception	Source (From)	
1	CDC-10	Critical	Combinatorial logic detected before a syn	chroniz	 er	5 F	False Path	i_my_ip_support_block/jesd204_i/inst/i_my_ip/i_tx/i_tx_co	ounters_32/gol
Sour Dest CDC	ce Clock ination Type: No	: my_ip_ax Clock: my_ Common Pr	i_aclk ip_drpclk imary Clock						
Ro⊎	ID	Severity	Description	D	epth B	Except	tion Sour	ce (From)	
1 2	CDC-11 CDC-11	Critical Critical	Fan-out from launch flop to destination c Fan-out from launch flop to destination c	lock lock	5 F 5 F	False False	Path i_my Path i_my	_ip_support_block/jesd204_i/inst/i_my_ip_reset_block/stref _ip_support_block/jesd204_i/inst/i_my_ip_reset_block/stref	:ch_reg[10]/C :ch_reg[10]/L
Sour Dest CDC	ce Clock ination Type: No	: my_ip_ax Clock: my_ Common Pr	i_aclk ip_glblclk imary Clock						
Ro⊎	ID	Severity	Description	Depth	Except	tion	Source (F	rom)	Destination
1 2 3 4 5	CDC-14 CDC-14 CDC-14 CDC-14 CDC-14 CDC-14	Critical Critical Critical Critical Critical	Multi-bit CDC path on a non-FD primitive Multi-bit CDC path on a non-FD primitive	0 0 0 0 0	False False False False False	Path Path Path Path Path	i_my_ip_s i_my_ip_s i_my_ip_s i_my_ip_s i_my_ip_s	<pre>upport_block/jesd204_i/inst/tx_cfg_test_modes_reg[2:1]/C upport_block/jesd204_i/inst/tx_cfg_test_modes_reg[2:1]/C upport_block/jesd204_i/inst/tx_cfg_test_modes_reg[2:1]/C upport_block/jesd204_i/inst/tx_cfg_test_modes_reg[2:1]/C upport_block/jesd204_i/inst/tx_cfg_test_modes_reg[2:1]/C</pre>	<pre>i_my_ip_suppr i_my_ip_suppr i_my_ip_suppr i_my_ip_suppr i_my_ip_suppr i_my_ip_suppro,</pre>

7. To export all the waivers inside a script and verify that a total of four waivers were added, enter:

write_waivers -type cdc waivers.xdc -force

Note: Because the waivers.xdc file already exists, the -force option must be specified to override the file.



TIP: Alternatively, because there are no DRC or methodology waivers, you can enter:

```
write_waivers waivers.xdc -force
```

or

 \bigcirc

write_xdc -type waiver waivers.xdc -force

The list of waivers inside waivers.xdc appears as follows.

```
WRITE CDC Maivers

cnd; write_waivers = type cdc = file waivers,xdc = force

current_instance = quiet

create_waiver = type CDC = id (CDC-10) = user "Xilinx" = desc "This is a safe CDC per review with the team" = from [get_pins i_mg_ip_support_block/jesd204_i/inst/i_mg_ip_itx/i_tx_counters_32/got_

create_waiver = type CDC = id (CDC-11) = user "Xilinx" = desc "Safe fanout, Circuitry has been released" = from [get_pins i_mg_ip_support_block/jesd204_i/inst/i_mg_ip_reset_block/stretch_reg[10]/C

create_waiver = type CDC = id (CDC-14) = user "Xilinx" = desc "Safe fanout, Circuitry has been released" = from [get_pins (i_mg_ip_support_block/jesd204_i/inst/i_mg_ip_reset_block/stretch_reg[10]/C

create_waiver = type CDC = id (CDC-14) = user "Xilinx" = desc "No more CDC-14!" = from [list [get_pins {i_mg_ip_support_block/jesd204_i/inst/tx_cfg_test_modes_reg[1]/C}] [get_pins {i_mg_ip_support_l

current_instance = quiet
```

8. To import the waivers.xdc file, enter:

read_xdc waivers.xdc

The following warnings show that duplicate waivers were not added to the existing waivers. Only waivers that are exact duplicates of existing waivers are rejected.

```
WARNING: [Vivado_Tcl 4-935] Waiver ID 'CDC-10' is a duplicate and will
not be added again.
WARNING: [Vivado_Tcl 4-935] Waiver ID 'CDC-11' is a duplicate and will
not be added again.
WARNING: [Vivado_Tcl 4-935] Waiver ID 'CDC-11' is a duplicate and will
not be added again.
WARNING: [Vivado_Tcl 4-935] Waiver ID 'CDC-14' is a duplicate and will
not be added again.
```

Step 10: Waiving Multiple DRC Violations

In this step, you waive multiple DRC violations simultaneously.

- 1. Select **Reports** \rightarrow **Report DRC**.
- 2. In the Report DRC dialog box, leave all settings at their default, and click **OK**.



🍌 Report DRC			\times
Check design against sele	cted rule decks and/or individual desig	in rules.	4
<u>R</u> esults name: <u>Interactive report file:</u> <u>Export to file:</u>	drc_1		
Waivers Apply waivers Display only w Ignore all waivers Rule Decks Vivado Rule Deck default	raived violations s (7)	Rules (2119 of 2135) Q X 2119 of 2135) ✓ ■ All Rules (2135)	
opt_check opt_check	s ecks checks checks ss	 Netlist (737) Pin Planning (110) Clocking (4) Memory (148) Floorplan (10) Implementation (239) Physical Configuration (842) 	~
 ✓ Open in a new tab ? 		ОК	Cancel

3. In the DRC Report, right-click **UCIO#1**, and select **Create Waiver** to create a waiver for the UCIO-1 violations.

Note: The UCIO#1 violation combines 125 individual violations into a single violation. Similarly, the NSTD#1 violation covers 113 ports.



Tcl Console Messages DR	C × Timing							
Q ¥ ♦ ■ 8	🗸 🌖 3 Critical Warnings 🛛 🖌 1 Warning 🛛 Hide All							
Name	Details							
• (1) NSTD-1 (1)								
• NSTD #1	NSTD #1 113 out of 125 logical ports use I/O standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This may cause I/O contentic components to which it is connected. To correct this violation, specify all I/O standards. This design will fail to generate a bitstream unless all logical p command: set_property SEVERITY {Warning} [get_drc_checks NSTD-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl com s axi araddr[10], s axi araddr[9], s axi araddr[8], s axi araddr[7], s axi araddr[6], s axi araddr[6], s axi araddr[4], s axi araddr[7],							
UCIO-1 (1)								
UCIO #1	UCIO #1 125 out of 125 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incom correct this violation, specify all pin locations. This design will fail to generate a bitstream unless a [get_drc_checks UCIO-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs To							
 Implementation (1) 		,	Auto Soloct Objects					
✓ ➡ Routing (1)		ľ	Auto-Mark Objects					
Chip Level (1)								
• () RTSTAT-13 (1)		~	wrap Lines					
RTSTAT #1	A signficant portion of the design is not routed. Routed nets status (RTSTAT-*) DRC checks will no		Create waiver	ute_s				
drc_1 (4 violations)			Export to Spreadsheet					

4. In the Create Waiver dialog box, look at the output in Tcl Command Preview, and click OK.

🝌 Create Wa	aīver	\times
Create waiver f	or 1 violation	
User:	Xilinx	
Description:	Waive UCIO DRC violations	\otimes
Tags:		
Tcl Command	I Preview	
Q		
create_waive	r -of_objects [get_drc_violations -name drc_1 {UCIO-1#1}] -user Xilinx -description {Waive UCIO DRC v	viol
4		>
?	OK Cancel	•

5. To generate the drc_waivers.xdc file and verify that the waiver is waiving all 125 objects, enter:

write_waivers -type DRC drc_waivers.xdc

6. In the XDC file, look at the expanded port list, and notice that some of the strings from the violations message were converted to wildcards (*).



Strings are automatically converted to wildcards for UCIO-1, NSTD-1, TIMING-15, and TIMING-16 type violations. For UCIO-1, the numbers of objects in the violations are replaced with wildcards, because the numbers of elements are not meaningful.

T
* WRITE DRC WAIVERS
cwd; write_waivers -type DRC drc_waivers,xdc
current_instance -quiet
create_waiver -type DRC -id {UCIO-1} -user "Xilinx" -desc "Waive UCIO DRC violations" -objects [get_ports { refclk0p glblclkp refclk0n tx_start_of_frame[3] tx_start_of_multiframe[3] glblclkp
tx_reset drpclk tx_start_of_multiframe[2] txp[3] tx_start_of_multiframe[0] tx_start_of_frame[2] tx_start_of_frame[1] s_axi_rready tx_sync tx_sysref tx_aresetn s_axi_rdata[1] s_axi_rvalid
s_axi_rresp[0] s_axi_rresp[1] s_axi_rdata[0] s_axi_rdata[2] s_axi_rdata[3] s_axi_rdata[4] s_axi_rdata[9] s_axi_rdata[5] s_axi_rdata[10] s_axi_rdata[6] s_axi_rdata[7] s_axi_rdata[8]
s_axi_rdata[15] s_axi_rdata[11] s_axi_rdata[12] s_axi_rdata[13] s_axi_rdata[16] s_axi_rdata[17] s_axi_rdata[18] s_axi_rdata[14] s_axi_rdata[20] s_axi_rdata[21] s_axi_rdata[22] s_axi_rdata[22
s_axi_rdata[23] s_axi_rdata[19] s_axi_rdata[25] s_axi_rdata[26] s_axi_arready s_axi_rdata[28] s_axi_rdata[24] s_axi_rdata[30] s_axi_rdata[31] s_axi_araddr[2] s_axi_arvalid s_axi_rdata[29]
s_axi_araddr[7] s_axi_araddr[3] s_axi_araddr[4] s_axi_araddr[5] s_axi_araddr[6] s_axi_bvalid s_axi_araddr[9] s_axi_araddr[10] s_axi_bready s_axi_wstrb[0] s_axi_wstrb[1] s_axi_araddr[8]
s_axi_bresp[1] s_axi_wready s_axi_wvalid s_axi_wdata[0] s_axi_bresp[0] s_axi_wstrb[2] s_axi_araddr[11] s_axi_wdata[4] s_axi_wdata[1] s_axi_wstrb[3] s_axi_wdata[2] s_axi_wdata[3]
s_axi_wdata[9] s_axi_wdata[5] s_axi_wdata[6] s_axi_wdata[7] s_axi_wdata[8] s_axi_wdata[14] s_axi_wdata[10] s_axi_wdata[11] s_axi_wdata[12] s_axi_wdata[13] s_axi_wdata[19] s_axi_wdata[15]
s_axi_wdata[16] s_axi_wdata[17] s_axi_wdata[18] s_axi_wdata[24] s_axi_wdata[20] s_axi_wdata[28] s_axi_wdata[25] s_axi_wdata[26] s_axi_wdata[27] s_axi_awready s_axi_awvalid txp[4]
tx_start_of_multiframe[1] txp[1] tx_start_of_frame[0] txp[2] txn[1] txn[3] txn[2] s_axi_awaddr[11] txn[0] txn[0] txp[0] s_axi_awaddr_saxi_awaddr[7] s_axi_awaddr[7] s_axi_awaddr[8]
s_axi_awaddr[9] s_axi_awaddr[2] txn[4] s_axi_awaddr[5] s_axi_awaddr[6] s_axi_awaddr[3] s_axi_awaddr[4] }] -strings { "*" } -strings { "*" } -timestamp "Wed Mar 14 22;57:14 GMT 2018" ;#1

7. To delete the DRC waiver and rewrite the waiver using wildcards to target a subset of the ports objects, enter:

```
delete_waivers [get_waivers -type drc]
create_waiver -type DRC -id {UCIO-1} -user "Xilinx" -desc "Waive
selected UCIO violations" -objects [get_ports { s_axi_rdata[*]
s_axi_wdata[*] s_axi_araddr[*] } ] -strings { "*" } -strings { "*" }
```

Note: This command only covers a subset of the original 125 objects.

- 8. Select **Reports** \rightarrow **Report DRC** to rerun Report DRC.
- 9. In the Report DRC dialog box, select **Display only waived violations** to report only waived violations, and click **OK**.





À Report DRC			\times
Check design against sele	cted rule decks and/or individual des	ign rules.	4
<u>Results name:</u> Interactive report file: <u>Export to file:</u> <u>Waivers</u> Apply waivers	drc_2		
Display only w	vaived violations		
 Ignore all waivers Rule Decks ✓ ■ Vivado Rule Deck ✓ Ø default Ø opt_check Ø placer, ch 	s (7) S	Rules (2120 of 2136) Q X → Image: All Rules (2136) > Image: Netlist (737)	î
 □ pictor_chi □ ∅ router_chi □ ∅ bitstream_ □ ∅ incr_eco_u □ ∅ eco_check 	ecks _checks checks KS	 Pin Planning (110) Clocking (4) Memory (148) Floorplan (11) Implementation (239) Physical Configuration (842) 	~
 ✓ Open in a new tab ? 		ок	ancel

In the DRC Report, verify that only 68 violations are waived out of 125.



IMPORTANT! You cannot waive READONLY or NODISABLE violations. For example, if you enter:

create_waiver -type DRC -id RTSTAT-1 -description "Waive RTSTAT-1"



The Vivado tools issue the following error:

ERROR: [Vivado_Tcl 4-934] Waiver ID 'RTSTAT-1' is READONLY or NODISABLE and cannot be waived. These Factory designations specify that a check is required and may not be overridden by user action.

Step 11: Generating a Summary Report for Waived Violations

This step covers how to use the report_waivers Tcl command to generate a summary report for CDC, DRC, and methodology waivers.



IMPORTANT! Before running the *report_waivers* command, you must rerun Report CDC, Report DRC, or Report Methodology to ensure that added or removed waivers are included in the statistics reported by *report_waivers*.

1. To rerun Report CDC, enter:

report_cdc

2. To rerun Report DRC, enter:

report_drc

Note: You do not need to rerun Report Methodology, because no methodology waivers were set.

3. To create a summary report, enter:

report_waivers

By default, report_waivers reports only waived violations. The following figure shows the UCIO-1, CDC-10, CDC-11, and CDC-14 rules, which have defined waivers.



Table Of	f Conter	its								
1. REPOR 2. REPOR 3. REPOR 4. REPOR	rt summa Rt detai Rt detai Rt detai	IS (DRC) LS (DRC) LS (METHO LS (CDC)	DOLOGY: no waive	ers)						
1. REPOR	rt summa	IRY								
Waiver 1	Туре То	tal Vios	Remaining Vios	Waived Vios	Used Waivers	Set Waivers				
DRC METHODOL	23 LOGY 0	19	171 0	68 0	1 0	1 0				
Note: Ti	his repo	wrt is bas	ed on the most r	recent report_	drc/report_met	4 hodology/repor	t_cdc runs.			
	DT DETAI									
Rule	Severi	ty	Description		Total Vios	Remaining Vios	Waived Vios	Used Waivers	Set Waivers	
UCI0-1*	Critic	al Warnin	g Unconstrained	d Logical Port	125	57	68	1	1	
4. REPOR	RT DETAI	LS (CDC)								
Rule	Severit	y Descri	ption			Total Vios	Remaining Vios	Waived Vios	Used Waivers	Set Waivers
CDC-10 CDC-11 CDC-14	Critica Critica Critica	l Combin l Fan-ou l Multi-	ational logic de t from launch fl bit CDC path on	tected before lop to destina a non-FD prim	a synchronize tion clock itive	r 187 2 10	186 0 0	1 2 10	1 2 1	1 2 1
Note: Ar	ny 'Rule ather th	'which i an the nu	s flagged by ' * ' wber of messages	is an aggreg	ating message	and its counts	are based on t	he number of	objects represe	mted,

Note the number of waived objects and total violations:

- The aggregating DRCs are reported as 1 violation per object inside the violation. Because there are 113 objects in NSTD-1, 125 objects in UCIO-1 plus 1 in RTDAT-13, a total number of 239 DRC violations are reported in the Summary table.
- The Report Summary table reports all of the violations.
- The Report Details tables only report the check IDs that have one or more waivers.
- 4. To generate detailed tables with all of the rules, including rules with no waivers, enter:

report_waivers -show_msgs_with_no_waivers

The following figure shows the report with all DRC and CDC rules reported in the Report Details.



Table Of 1. REPORT 2. REPORT 3. REPORT 4. REPORT	SUMMARY DETAILS (DRI DETAILS (MET DETAILS (CDI) HODOLOGY: no waiv)	ers)										
1. REPORT	SUMMARY												
Waiver Ty	pe Total Vio	s Remaining Vios	Waived Vios	Use	d Waivers	Set Wa	ivers						
DRC METHODOLO CDC Note: Thi	239 GY 0 957 s report is b	171 0 944 ased on the most	68 0 13 recent report,	1 0 4 drc/	report_met/	1 0 4 hodolog	yy/report_c	dc runs.					
2. REPORT	DETAILS (DRO	:)											
Rule	Severity	Descriptio	n		Total Vios	Renai	ning Vios	Waived Vios	Used	d Waivers	Set	Waivers	
UCIO-1* NSTD-1* RTSTAT-13	Critical Wa Critical Wa Critical Wa	rning Unconstrai rning Unspecifie rning Insufficie	ned Logical Po d I/O Standard nt Routing	ort d	125 113 1	57 113 1		68 0 0	1 0 0		1 0 0		
4. REPORT	DETAILS (CD	.)											
Rule S	everity Desc	ription					Total Vio	s Remaining	Vios	Waived V	ios	Used Waivers	Set Waiver
CDC-10 C CDC-11 C CDC-14 C CDC-1 C CDC-3 L CDC-3 L CDC-4 C CDC-9 L CDC-13 C CDC-13 C CDC-15 W	ritical Coek ritical Fan- ritical Mult ritical 1-bi ritical Mult nfo 1-bi ritical Mult nfo Asyr ritical 1-bi arning Cloo	inational logic c out from launch f i-bit CDC path or t unknown CDC cir t synchronized wi i-bit unknown CDC chronous reset sy t CDC path on a r k enable controll	etected before lop to destina a non-FD prin cuitry th ASINC_REG p circuitry nchronized with on-FD primitiv ed CDC structs	e a s ation aitiv prope th AS ve ure d	synchronize n clock we arty SYNC_REG pro detected	operty	187 2 10 536 9 28 5 170 10	186 0 536 9 28 5 170 10		1 2 10 0 0 0 0 0 0 0		1 2 1 0 0 0 0 0 0 0 0	1 2 1 0 0 0 0 0 0 0 0
Note: Any rat	'Rule' which her than the	is flagged by ' number of message	'is an aggres s.	9atin	ng message	and its	counts ar	e based on th	e nu	wher of ob	ject	s represented,	

5. To run Report Methodology, enter:

report_methodology

6. To generate detailed tables with all of the rules, including rules with no waivers, enter:

report_waivers -show_msgs_with_no_waivers

The exact statistics are reported, as shown in the following figure.

Note: This figure does not include the Report Details (CDC) section.



1 REPORT 9	SUMMARY										
Waiver Type	e Total V	Vios F	emaining Vios	Waived Vios	Used Waiv	ers	Set Waivers				
DRC METHODOLOGY CDC Note: This	239 / 157 957 report is	s based	.71 57 144 1 on the most r	 68 0 13 ecent report_c	 0 4 Irc/report,	 _metł	 1 0 4 hodology/report_(cdc runs.			
2. REPORT I	DETAILS ()	DRC)									
Rule	Severity		Description		Total	Vios	Remaining Vios	Waived Vios	Used Waivers	Set Waivers	
UCIO-1* Critical Warning NSTD-1* Critical Warning RTSTAT-13 Critical Warning		ng Unconstrain ng Unspecified ng Insufficien	ed Logical Por I/O Standard t Routing	t 125 113 1		 57 113 1	68 0 0	1 0 0	1 0 0		
3. REPORT I)ETAILS (1	METHODO	LOGY)								
Rule	Severit	y Desc	ription		Total V	ios	Remaining Vios	Waived Vios	Used Waivers	Set Waivers	
LUTAR-1* TIMING-9 TIMING-10 TIMING-18*	Warning Warning Warning Warning	LUT Unkr Miss Miss	drives async r nown CDC Logic sing property o sing input or o	eset alert n synchronizer utput delay	40 1 1 115		40 1 1 115	0 0 0 0	0 0 0 0	0 0 0 0	

Step 12: Using Waiver Commands

In this step, you run additional commands related to the waivers.

1. To return a collection of CDC waiver objects, enter:

get_waivers -type cdc

The following CDC waivers are returned:

CDC-10#1 CDC-11#1 CDC-11#2 CDC-14#1

2. To filter the list of waivers to only return CDC-14 waivers, enter:

get_waivers -filter {ID == CDC-14}
CDC-14#1

3. To report all of the properties on a CDC waiver object, enter:

report_property [lindex [get_waivers -type cdc] end]

The following properties are returned:

Property	Type	Read-only	Value
CLASS	string	true	cdc_waiver
DESCRIPTION	string	false	No more CDC-14!
ID	string	true	CDC-14
INDEX	string	true	1
IS_SCOPED	bool	true	0
NAME	string	true	CDC-14#1
OBJECT_COUNTS	string	true	pins:2
SCOPE	string	true	



TAGS	string	false	
TIME	string	true	<timestamp></timestamp>
TYPE	string	true	CDC
USED_CNT	string	true	10
USER	string	true	Xilinx

Note: You cannot retrieve the design objects attached to a waiver object.

4. To delete all of the previously created CDC-14 waivers, enter:

```
delete_waivers [get_waivers -filter {ID == CDC-14}]
```

Note: After a waiver object is deleted, the waiver no longer applies and the violations that it waived are reported again.

5. To delete all of the remaining CDC waivers, enter:

```
delete_waivers [get_waivers -type cdc]
```

Summary

In this lab, you accomplished the following:

- Waived CDC and DRC violations
- Generated reports for waived violations
- Exported waivers
- Used waiver commands



Lab 2

Increasing Design Performance Using Report QoR Suggestions

Introduction

Note: This tutorial requires the installation of a patch. For more information, refer to Xilinx Answer Record 75374.

The report_qor_suggestions (RQS) command enables the Vivado® Design Suite tools to analyze a design and provide automated solutions for enhancing QoR. The command can be run on an open design after synthesis or after any stage in the implementation flow. RQS evaluates the design in five key areas and suggests fixes or improvements in these areas. The five areas are utilization, clocking, constraints, congestion, and timing. Recommendations from RQS can take the following forms:

- RQS objects. These can add:
 - Switches to a given command
 - Properties to a given design object
 - Implementation strategies customized for the design using machine learning algorithms
- Text recommendations that require intervention by the user.

This tutorial will cover how to:

- Analyze the QoR suggestion report
- Export suggestions to an RQS file
- Add an RQS file to synthesis and implementation runs
- Accumulate suggestions in an RQS file by generating suggestions at different implementation stages or on different runs



Step 1: Understanding the Design

This lab uses an architected design to demonstrate some of the features of RQS. Suggestions are triggered by the design of the RTL and the placement of blocks using floorplanning. The design contains the following modules:

• Clocking Module: The main clocking circuit for the design resides in clocking_module.vhd. For simplicity, RST is tied to GND. LOCKED is registered and tied to an output port. The structure of this block is shown in the following figure.



- **Reg CLKA to CLKB Module:** This module contains a synchronous CDC for a large bus. It registers input data using CLKA and then passes it to a register on the CLKB domain to be passed to the output. Registering large buses on different related clock domains can impact hold slack (WHS/THS) and setup slack (WNS/TNS).
- **Bit Expander and Bit Reducer Modules:** These modules enable the expansion and contraction of internal data widths so that the design does not run out of I/Os. The modules take an arbitrary data width and expand or contract it to or from a desired size. The contraction logic creates many logic levels.

The following steps cover opening the project and examining the placement of the floor-planned modules.

1. In the Vivado Design Suite, go to File → Project → Open and select the project located in <extract_Dir>/Lab2/project_2.



	<u>F</u> ile	Flow	Tools	<u>W</u> indo	w <u>H</u> elp	Q- Quick Access
		Project		•	<u>N</u> ew	
		<u>C</u> onstrai	nts		Open	. _N
		Simul <u>a</u> tio	on Waveforr	m →	Open [Recent ►
l		Chec <u>k</u> point			Opent	Ex <u>a</u> mple
		<u>I</u> P		•		
		I <u>m</u> port			art	
ļ		Exit				

- 2. In the Flow Navigator, click Run Synthesis and wait for synthesis to complete.
- 3. In the Flow Navigator, click **Open Synthesized Design**.
- 4. In the Netlist view, look at the hierarchy.





5. In Device view, look at the pblock. This has been added to control placement of the reg_clka_to_clkb modules and force a poor clock skew.



Step 2: Running Report QoR Suggestions

This step covers running the <code>report_qor_suggestions</code> command to generate a report. The command can be run on an open design at any stage of the implementation flow after synthesis. In project mode, this is typically after synthesis or implementation. In non-project mode, this can be after <code>synth_design,link_design,opt_design,place_design,phys_opt_design, or route_design.</code>

1. In the Vivado IDE, from the pull down menus, click **Reports** → **Report QoR Suggestions...** to bring up the dialog box shown in the following figure.

🝌 Report QoR Suggestions	×
Report design and tool option changes to improve the quality of results (QoR)	4
 ✓ Generate new suggestions Number of paths for suggestion analysis: ☐ View existing suggestions 	100 \$
ок	Cancel

The equivalent Tcl command is:

report_qor_suggestions -quiet -name qor_suggestions_1

The command will:

- Examine the design and generate new suggestions
- Generate a report on the suggestions

The report opens automatically in the integrated design environment (IDE). Due to the interactive nature of the report, only one instance of the report can be open at any time.

Note: By default, the RQS command reports on the 100 worst failing paths per clock group. You can change the number of paths that RQS uses for the analysis of timing-critical paths by modifying the -max_paths switch. Increasing this number generates more suggestions, but on paths that are reducing in criticality.

Step 3: Understanding the Report

This step explains the different sections of the generated QoR Suggestions report. On the left of the report window, you can navigate to the different sections of the report; on the right, more information is provided.



1. In the generated report, under RQS Summary, select **GENERATED**. This brings up the report section shown in the following figure.

QoR Suggestions							_ ם _×
Q 素 ≑ ← → *	Q, 🔮 🏮 GE	NERA	TED				
General	ID	☑	GENERATED_AT	APPLICABLE_FOR	AUTOMATIC	Incre	DESCRIPTION
~ RQS Summary	∼ 🗁 Timing	✓					
GENERATED	RQS_TIMING-33-1	\checkmark	synth_design	synth_design	Yes	No	Retiming registers in critical paths can improve timing.
✓ Timing	RQS_TIMING-44-1	\checkmark	synth_design	synth_design	Yes	No	Improve timing on critical path using RETIMING_BACKWARD property.
RQS_TIMING-33-1	✓ □ XDC	\checkmark					
RQS_TIMING-44-1	RQS_XDC-1-1	✓	synth_design	synth_design	No	No	Tight constraints for given paths. Review critical paths with difficult requirements and either re
~ XDC		\checkmark					
RQS_XDC-1-1	RQS_CLOCK-9-1	\checkmark	synth_design	place_design	Yes	Yes	Sub optimal Fvco on MMCM/PLL. Update MMCM/PLL settings to improve the jitter.
Clocking ROS CLOCK-9-1	ML Strategies are available of the strategies are available	nly in	default/explore at su	ccessfully routed desig	jn.		
			Reset De	efault Export Sug	gestions	Add Sugge	estions to Project

The GENERATED section provides a list of all the suggestions that have just been generated at this stage of the current run. Each suggestion has a description that details the reason for the suggestion. Additionally, for each suggestion the following information is provided.

Table 1: RQS Summary Column Description

Item	Description	Comment
GENERATED_AT	This shows what stage of the design the suggestion was generated at. Typical values place_design or route_design	As you progress through the design stages, the decisions that the tool makes are based on the information available at the time. Additionally, information accuracy increases after placement and again after routing.
APPLICABLE_FOR	This is the stage that must be rerun in order for the suggestion to take effect.	Most suggestions are executed at either <pre>synth_design</pre> or <pre>place_design</pre>
AUTOMATIC	Details whether the suggestion is executed automatically or the user must manually intervene	Automatic suggestions will either recommend a switch to the tool or a property to be added to a cell or net
INCREMENTAL FRIENDLY	Details if the suggestion is optimized for the incremental flow or not.	Non-incremental friendly suggestions must be already present in the reference checkpoint. If you want to add non incremental friendly suggestions, an updated reference checkpoint must be used.

Under the other sections of the report there are details about the individual suggestions that have been generated.

2. Click on the **RQS_XDC_1_1** hyperlink. This will take you to the details section for this suggestion.

QoR Suggestions													_ 🗆 🖓 🗙
Q ★ ♦ ♦ *	Q RQS_)	(DC-1-1											
General ^	No of Paths	Logic Levels	Routes	Slack	Req.	Skew	Datapath Delay	Cell%	Route%	Source Clock	Destination Clock	Startpoint	
~ RQS Summary	1	5	6	-0.396	1.667	-0.145	1.902	56.50	43.50	clk_600_clk_wiz_0	clk_600_clk_wiz_0	clk300_to_clk600_ffs	_i/expanded_sig3_rec
GENERATED													
✓ Timing													
RQS_TIMING-33-1													
RQS_TIMING-44-1													
~ XDC													
RQS_XDC-1-1													
Clocking													
RQS_CLOCK-9-1 🗸													
<>	<												>
				Res	et Defaul	Ex	port Suggestions	Add	Suggestion	is to Project			

The suggestion description says that the timing constraint is too tight for the given path(s).



The path has a large negative slack which would stand out in a timing report. Timing paths use net delays that are optimal, this gives the tools the correct order to place and route them. Close analysis shows this is a 600 MHz path with high logic levels. This is a path that will need to be fixed.

- 3. Click on the back arrow button * to go back to the GENERATED view.
- 4. In the GENERATED view, click on **RQS_TIMING-33_1** row. You can see this is an AUTOMATIC suggestions that is APPLICABLE_FOR synth_design. This tells us that you must rerun the synth_design command in order to make use of this suggestion.

QoR Suggestions							_ D J X
Q ¥ ≑ ← → *	Q 🛨 🌲 📵 Ge	NERA	TED				
General	ID		GENERATED_AT	APPLICABLE_FOR	AUTOMATIC	Incre	DESCRIPTION
~ RQS Summary	∼ 🚍 Timing	\checkmark					
GENERATED	RQS_TIMING-33-1		synth_design	synth_design	Yes	No	Retiming registers in critical paths can improve timing.
V Timing	RQS_TIMING-44-1	✓	synth_design	synth_design	Yes	No	Improve timing on critical path using RETIMING_BACKWARD property.
RQS_TIMING-33-1	✓	✓					
× YDC	RQS_XDC-1-1	✓	synth_design	synth_design	No	No	Tight constraints for given paths. Review critical paths with difficult requirements and either re
ROS XDC-1-1		✓					
Clocking	RQS_CLOCK-9-1	\checkmark	synth_design	place_design	Yes	Yes	Sub optimal Fvco on MMCM/PLL. Update MMCM/PLL settings to improve the jitter.
RQS_CLOCK-9-1	<						>
	ML Strategies are available of	only in	default/explore at suc	ccessfully routed desig	in.		
			Reset De	efault Export Sug	gestions	Add Sugge	estions to Project

When you select the row in the RQS Summary view, the suggestion object is selected and the properties can be seen in the QoR Suggestion Properties window. If you examine the command property, you can confirm that generates a retiming forward property for synth_design.



5. In the GENERATED view, click on **RQS_TIMING-33_1** ID to take you to the details table for that suggestion. Careful examination of the Endpoint column will confirm that this is the same path that was mentioned for RQS_XDC-1.

QoR Suggestions								_ D @ X
Q ¥ ≑ ≠ *	• Q	RQS_TIMING-33	1					
General	nout	Datapath Delay	Cell%	Route%	Source Clock	Destination Clock	Startpoint	Endpoint
V RQS Summary		1.902	56.50	43.50	clk_600_clk_wiz_0	clk_600_clk_wiz_0	clk300_to_clk600_ffs_i/expanded_sig3_reg[1932]/C	clk300_to_clk600_ffs_i/bit_reducer_i/tmp_r_reg/D
V Timing								
RQS_TIMING-33-1								
RQS_TIMING-44-1								
~ XDC								
RQS_XDC-1-1								
Clocking								
RQS_CLOCK-9-1 🗸								
<>	<							>
					Reset Default	Export Suggestions	Add Suggestions to Project	

 In the GENERATED view, you can see the remaining suggestions. Note that the RQS_CLOCK-9 suggestion is APPLICABLE_FOR = place_design. This is shown in the following figure:

QoR Suggestions							<i>P</i> ×
Q, ≍ ≑ ← ⇒ "	Q	NERA	TED				
General	ID		GENERATED_AT	APPLICABLE_FOR	AUTOMATIC	Incre	DESCRIPTION
V RQS Summary		1					
GENERATED	RQS_TIMING-33-1	\checkmark	synth_design	synth_design	Yes	No	Retiming registers in critical paths can improve timing.
✓ Timing	RQS_TIMING-44-1		synth_design	synth_design	Yes	No	Improve timing on critical path using RETIMING_BACKWARD property.
RQS_TIMING-33-1	✓ □ XDC	✓					
RUS_TIMING-44-1	RQS_XDC-1-1	✓	synth_design	synth_design	No	No	Tight constraints for given paths. Review critical paths with difficult requirements and either re
		✓					
V Clocking	RQS_CLOCK-9-1		synth_design	place_design	Yes	Yes	Sub optimal Fvco on MMCM/PLL. Update MMCM/PLL settings to improve the jitter.
RQS_CLOCK-9-1	<						>
<	ML Strategies are available of	only in	default/explore at su	ccessfully routed desig	ın.		
			Reset De	efault Export Sug	gestions	Add Sugge	estions to Project

7. With all the boxes checked, click **Add Suggestions to Project**. When the report suggestion dialogue box is open, change the filename to **rqs_report.rqs** and select **Copy sources to project** as shown in the following figure.

▲ Export Suggestion		×
Save selected suggestions to proje	t.	4
Save suggestions as:	rqs_report.rqs	⊗
		DK Cancel



8. Examine the Sources window. You will see that the RQS file has been added to the utils_1 fileset. This ensures that the file is captured using the get_files command, project archives and recognized in the next step when we add the file to a run.



Step 4: Run with Suggestions

You will now add a suggestion to a run and examine what happens when a suggestion is applied and how it is reported.

 In the Design Runs window, click the + icon and generate both a new Synthesis and Implementation run. Ensure both runs have the Default run strategy and in the final step, select **Do not launch now**.

À Create New Runs					×
Launch Options Configure hosts for la	aunching runs, and/or set advanced la	unch options			4
Launch <u>d</u> irectory: Options	Sectory Content of Con				~
 Launch rur Generate s Do not laur 	s on local host Number of jobs: 6 cripts only ich now	~			
?		< <u>B</u> ack	Next >	<u>F</u> inish	Cancel



2. In the Design Runs window, right-click on the new synth_2 run and select Set QoR Suggestions

	Synthesis Run Properties	Ctrl+E
×	Delete	Delete
	Make Active	
	Change Run Settings	
	Set Incremental Synthesis	
	Include Incremental Synthesis Information in DCP	
	Set QoR Suggestions	
	Save As Run Strategy	
	Save As Report Strategy	
	Display Messages	
	Copy Run	
+	Create Runs	
	Open Run Directory	
	Export to Spreadsheet	

3. Specify the suggestion file as the RQS file added to the project from the previous step and click **OK**.



- 4. Repeat steps 2 and 3 for the implementation run. Specify the same RQS file for each run.
- 5. In the Design Runs window, right-click on synth_2 and select Make Active.
- 6. In the Flow Navigator, click **Run Synthesis**.



7. As this design takes a long time to route, we will only run to place_design and analyze at this stage. When synthesis is complete, in the Design Runs window, right-click on the new implementation run and select Launch Step To → place_design.



8. When place_design is finished, first go and examine the very top of the implementation log file for the new implementation run. You can see a table summary of the suggestions that have been read in. This summary helps confirm that what is read in is what you expect.



1. Read QOR Suggestions Summary		
Read QOR Suggestions Summary	+	+ +
Suggestion Summary	Incr Friendly	Total
+	+	+ +
Total Number of Suggestions	1	4
Automatic	1 1	3
Manual	0	1
APPLICABLE_AT		I I
synth_design	0	3
opt_design	0	
That overlap with synthesis suggestions	0	0
place_design	1	1
postplace_phys_opt_design	0	
route_design	0	
postroute_phys_opt_design	I 0	
+		+ +

- 9. Right-click on the implementation run and select **Open Run Directory**. Next open the checkpoint file by double-clicking on **top_placed.dcp**. This step is necessary as we are examining an intermediate run step in the interests of saving time.
- 10. In the new instance of Vivado tools, select **Reports** \rightarrow **Report QoR Suggestions**
- 11. In the Report QoR Suggestions dialog box, ensure that **View Existing Suggestions** is selected, and click **OK**.

Report design and tool option changes to improve the c QoR)	uality of results
✓ Generate new suggestions	
Number of paths for suggestion analysis:	100 🌲
✓ <u>V</u> iew existing suggestions	

In the new report, you will notice that there are more sections under RQS Summary.

QoR Suggestions						_ □ ㅋ×
Q, ¥ ♦ ← →	Q 🔮 🌲 Appli	ED				
General	ID 🗹	GENERATED_AT	APPLICABLE_FOR	AUTOMATIC	Incremental Friendly	DESCRIPTION
✓ RQS Summary	∼ 🖹 Timing 🖉)				
GENERATED	🔒 RQS_TIMING-33-1 🕑	synth_design	synth_design	Yes	No	Retiming registers in critical paths can improve timing.
EXISTING	RQS_TIMING-44-1	synth_design	synth_design	Yes	No	Improve timing on critical path using RETIMING_BACKWARD property.
APPLIED)				
Timing	RQS_CLOCK-9-1	synth_design	place_design	Yes	Yes	Sub optimal Fvco on MMCM/PLL. Update MMCM/PLL settings to improve the jitter.
RQS_TIMING-33-1						
RQS_TIMING-44-1						
Clocking						
RQS_CLOCK-9-1						
RQS_CLOCK-15-1						
RQS_CLOCK-1-1						
~ XDC	1					
RQS_XDC-1-1	ML Strategies are available only	in default/explore at su	ccessfully routed desig	an.		/
			Reset Default	Export Sugge	stions	

- GENERATED This is where new suggestions are listed
- EXISTING These are suggestions that existed previously but are not applied



• APPLIED - These are where suggestions that have been applied are listed

There is also another category possible called FAILED_TO_APPLY which is not listed here. This can be shown when design changes cause the suggestion to fail.

Also note that the option to add to the project is not available when a checkpoint is opened. You can still export a file but it is not added to a project.

12. Click **APPLIED** and select the details table for one of the items. For APPLIED suggestions, the timing path summary is still available but it is not possible to cross probe to other views in Vivado as some items may have changed.

Step 5: Accumulating Suggestions

You can now review the newly generated suggestions and add them to the RQS file.

- 1. Click on **GENERATED**. RQS_CLOCK-15 is a message that reports the high THS paths but does not provide an automatic suggestion. Therefore, we will focus on RQS_CLOCK-1-1. This suggestion applies CLOCK_DELAY_GROUP to related clocks.
- 2. Click on **RQS_CLOCK-1-1** to view the detailed report. In this report, you can see that there is a high clock skew.

QoR Suggestions 💷 🖬 🛪												
Q 素 ♠ ♠ [∞] (Q R0s_CLOCK-1.1												
Clocking	^	Path Type	Skew	Slack	Req.	Datapath Delay	Cell%	Route%	Source Clock	Destination Clock	Source Clock Topology	Destination Clock T
RQS_CLOCK-9-1		HOLD	0.924	-1.017	0.000	0.182	61.50	38.50	clk_600_clk_wiz_0	clk_300_clk_wiz_0	INBUF IBUFCTRL MMCME4_ADV BUFGCE FDRE	INBUF IBUFCTRL M
RQS_CLOCK-15-1												
RQS_CLOCK-1-1												
~ XDC												
RQS_XDC-1-1 V <										>		
	Reset Default Export Suggestions											

Clock skew is difficult to identify before place_design as the skew estimate depends heavily on placement. As a consequence, RQS does not offer this suggestion unless a design is placed. Whenever there is a change in information level, it can be worth running report_qor_suggestions. The following summarizes the changes as you progress through the tool flow:

- Clocking estimates are accurate after place_design
- Congestion is available after placement and improves further after routing
- Timing estimates improve throughout the flow and are impacted by the number of paths analyzed
- 3. Click **Export Suggestions**. When suggestions are exported, the APPLIED status is reset. All the previous suggestions and the new RQS_CLOCK-1-1 are combined into one file. You can overwrite the previous file and reuse the runs, or create a new file and runs.



4. Select the file location to overwrite the existing file. You can find out the location of this by selecting it in the sources window. Alternatively, it should be at the following location if you have followed the steps carefully <extract_dir>/Lab2/project_2/project_2.srcs/utils_1/imports/project_2.

You are now at the point where you know the fundamentals in handling RQS files and accumulating suggestions. If you have time, rerun implementation through to route_design and examine the impact of the latest suggestion. Alternatively generate alternative suggestions by running report_qor_suggestions on your own design.

Summary

In this lab, you used RQS to conduct a complex analysis of a demonstration design. You firstly examined the reports that showed RQS provided recommendations to solve implementation problems, then generated an RQS file and added it to a project implementation run. The Vivado implementation tools executed these suggestions automatically for you. You subsequently performed further analysis and generated further suggestions, accumulating them in the RQS file.



Lab 3

Running ML Strategies

Introduction

The report_qor_suggestions command can generate an implementation design strategy that is predicted to be optimal for the design using machine learning algorithms. In this tutorial, you will look at:

- How to generate ML Strategy suggestions
- How to setup the implementation run to use ML Strategy suggestions
- Reporting specifics related to ML Strategies

Step1: Generating an ML Strategy RQS File

This step shows the process of opening a routed design with QoR Suggestions and generating a new RQS file with strategies. For details on the design refer to Step 1: Understanding the Design.

1. In the Vivado Design Suite, go to File → Project → Open and select the project located in <extract_Dir>/Lab3/project_2.



- 2. In the Flow Navigator, click Open Implemented Design.
- 3. At the Tcl console, type report_qor_assessment at the Tcl console.



4. In the following Overall Assessment Summary table, you will see that this design is ML compatible. This table identifies good candidate designs to use ML Strategy suggestions.

QoR Assessment Score	2 - Implementation may complete. Timing will not meet.
Report Methodology Severity	Methodology not run.
ML Strategy Compatible	Yes
Incremental Compatible	No
Next Recommended Flow Stage	Run report_qor_suggestions and run recommended ML strategies.

If a design is not ML Compatible, it does not prevent the tools generating strategies but it does indicate whether you are likely to benefit from them. Designs that are a long way from meeting timing are excluded from being compatible as they have issues that should be resolved before increasing effort levels in the tool flow.

- 5. In the Design Runs window, confirm the strategy is Vivado Implementation Defaults. ML Strategies can only be generated when a design has been run with either the Vivado Implementation Default or Performance_Explore strategy. In non-project mode, the equivalent commands are when all commands have directive set to all Default or all Explore. A mix of Default and Explore is not allowed.
- 6. From the pull-down menus, select **Reports** → **Report QoR Suggestions**
- 7. In the Report QoR Suggestions dialog box, ensure that **View Existing Suggestions** is selected, and click **OK**.

 ✓ Generate new suggestions Number of paths for suggestion analysis: 100 ♀ ✓ View existing suggestions 	Report design and tool option changes to improve the QoR)	quality of results
Number of paths for suggestion analysis: 100 🗘	✓ Generate new suggestions	
✓ View existing suggestions		100 *
	Number of paths for suggestion analysis:	100 -
Export to file:	Number of paths for suggestion analysis: <u>V</u> iew existing suggestions	100 +

8. In the QoR suggestion report, select **GENERATED**. Here you will see 3 new strategies generated but they are not selectable. Strategy generation is currently only available using Tcl and for this reason they are not selectable.

QoR Suggestions	QoR Suggestions									
Q ≚ ≑ ← →	~	Q 🔮 🖨 GENERA	TED							
General	^	ID		GENERATED_AT	APPLICABLE_FOR	AUTOMATIC	Incremental Friendly	DESCRIPTION		
~ RQS Summary			✓							
GENERATED		RQS_CLOCK-1-1	✓	route_design	place_design	Yes	No	Critical paths with high clock skew due to sub-optimal clock r		
EXISTING		✓								
APPLIED		RQS_STRAT-35-1		route_design	none	No	No	ML Strategy suggestion to improve timing		
✓ Timing		RQS_STRAT-17-1		route_design	none	No	No	ML Strategy suggestion to improve timing		
RQS_TIMING-33-1		RQS_STRAT-12-1		route_design	none	No	No	ML Strategy suggestion to improve timing		
RQS_TIMING-44-1										
Clocking										
RQS_CLOCK-9-1										
RQS_CLOCK-1-1	~	<	_					>		
				Reset Default	Export Suggestions	Add Sugge	stions to Project			



9. Select RQS_STRAT-35-1. Here you can see the details of the strategy being recommended. It is possible to see the details of the strategy suggested. It would be possible manually set these up as shown but in order to automate the process more easily, the recommended flow is to read an RQS file containing strategies, and set the directive to RQS on the implementation commands.

QoR Suggestions					$-\Box \supseteq \times$					
Q ≚ ≑ ← →	$Q \equiv \varphi \Rightarrow \varphi$ $Q = Q_s STRAT-35-1$									
	^	Command	Options							
RQS_CLOCK-9-1		opt_design	-directive ExploreWithRemap							
V XDC		place_design	-directive AltSpreadLogic_low							
		phys_opt_design	-directive AggressiveExplore							
<pre>Strategy</pre>		route_design	-directive NoTimingRelaxation							
RQS_STRAT-35-1	~									
	F	Reset Default Expo	ort Suggestions Add Sugges	stions to Project						

10. At the Tcl console, ensure you are in a suitable writable directory. This can be at the same level as the project. Also, issue the write_qor_suggestions command to write out the suggestions as shown in the following example.

```
file mkdir <extract_Dir>/Lab3/project_2/ML_STRAT
cd <extract_Dir>/Lab3/project_2/ML_STRAT
write_qor_suggestions -strategy_dir ./
```

This writes one RQS file per strategy. Each RQS file also contains all of the other suggestions that are not strategy suggestions. This ensures you can use all the other QoR suggestions and the tools do not get confused which strategy suggestion they should select.

Step 2: Creating ML Strategy Runs

In this step we will use the files generated to create ML Strategy project based runs.

1. Examine the contents of the ML_STRAT directory

Name	Date modified	Туре	Size
impl_2Project_MLStrategyCreateRun1.tcl	25/08/2020 16:49	TCL File	2 KB
impl_2Project_MLStrategyCreateRun2.tcl	25/08/2020 16:49	TCL File	2 KB
impl_2Project_MLStrategyCreateRun3.tcl	25/08/2020 16:49	TCL File	2 KB
impl_2SuggestionFile1.rqs	25/08/2020 16:49	RQS File	6 KB
impl_2SuggestionFile2.rqs	25/08/2020 16:49	RQS File	6 KB
impl_2SuggestionFile3.rqs	25/08/2020 16:49	RQS File	6 KB
NonProject_MLStrategyCreateRun1.tcl	25/08/2020 16:49	TCL File	1 KB
NonProject_MLStrategyCreateRun2.tcl	25/08/2020 16:49	TCL File	1 KB
NonProject_MLStrategyCreateRun3.tcl	25/08/2020 16:49	TCL File	1 KB

You can see the following contents:

- a. 3 x RQS files
- b. 3 x Project based Tcl scripts
- c. 3 x Non project based Tcl scripts



The RQS files are common for both project and non project flows. The non project scripts are examples of how to use the RQS file. The project based scripts can be sourced. Each of the 3 scripts references one of the RQS files. All three should be sourced.

2. Source each of the project based Tcl files. Each will create a run in the Design Runs window, setup the RQS file and set the directives to RQS. The run options will be copied from the reference run.

```
source ./impl_2Project_MLStrategyCreateRun1.tcl
source ./impl_2Project_MLStrategyCreateRun2.tcl
source ./impl_2Project_MLStrategyCreateRun3.tcl
```

3. In the Design Runs window, select **impl_2_ML_Strategy_1**.

Design Runs								? _ 🗆 🔊	×
Q 素 ♦ I4 ≪ I	> + %								
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	F
✓ ✓ synth_2	OriginalConstraints	synth_design Complete!							
✓ impl_2 (active)	OriginalConstraints	route_design Complete, Failed Timing!	-1.268	-1527.661	0.000	0.000	0.000	0.980	
impl_2_ML_Strategy_1	OriginalConstraints	Not started							
impl_2_ML_Strategy_2	OriginalConstraints	Not started							
impl_2_ML_Strategy_3	OriginalConstraints	Not started							
<									>

- 4. In the Implementation Run Properties window, select the **Properties** tab and confirm that RQS_FILES is set.
- 5. In the Implementation Run Properties window, select the **Options** and confirm the directive is set to RQS for each for the commands.



Implementation Run Properties				? _ □	ых
impl_1_ML_Strategy_1			+	→ 6	\$
Incremental Implementation:	Not	set			··· î
<u>S</u> trategy:	1 0	Vivado In	nplementati	on 👻	-
Description:	Defa	ault settir	ngs for Imple	ementation.	
✓Design Initialization (init_des	sign)				
tcl.pre					•••
tcl.post					•••
✓Opt Design (opt_design)					
is_enabled			\checkmark		
tcl.pre					•••
tcl.post					•••
-verbose			\Box		_
-directive*		RQS			~
More Options					-
YPower Opt Design (power_o	pt_de	esign)			~
General Properties Optic	ons	Log	Reports	Messages	3

You are now setup to run with ML Strategies. Once you have an ML Strategy file, you cannot generate new strategies after design changes but you can add other suggestions.

6. You are now ready to launch the runs. Select all the ML Strategy runs, right-click, and select **Launch Runs...**. The runs will now complete like a standard run.

Summary

In this lab, you used <code>report_qor_suggestions</code> to generate ML Strategies. Then created the RQS and Tcl files using <code>write_qor_suggestions</code>. Finally you sourced the Tcl to setup the ML Strategy runs and confirmed the key aspects of how to setup an ML Strategy run.





Appendix A

Additional Resources and Legal Notices

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