# **Vivado Design Suite Tutorial**

## **Using Constraints**

UG945 (v2019.2) December 6, 2019

This tutorial was validated with 2019.1. Minor procedural differences might be required when using later releases.



II☐ See all versions of this document



### **Revision History**

12/06/2019: Released with Vivado® Design Suite 2019.2 without changes from 2019.1.

Section	Revision Summary
06/24/2019	Version 2019.1
<ul> <li>Figure 2: Create an Example Project Page of the Open Example Project Wizard</li> <li>Figure 3: Select Example Project Page of the Open Example Project Wizard</li> <li>Figure 4: Project Name Page of the Open Example Project Wizard</li> <li>Figure 5: Default Part Page of the Open Example Project Wizard</li> <li>Figure 6: New Project Summary Page of the Open Example Project Wizard</li> <li>Figure 7: Project Default View</li> <li>Figure 8: Create Constraint Set Drop-Down Menu</li> <li>Figure 10: Sources WindowFigure 10: Sources Window</li> <li>Figure 11: Clock Sources with Missing Clock Definitions</li> <li>Figure 12: Completed Primary Clocks Page of the Timing Constraints Wizard</li> <li>Figure 13: Input Delay Page of Timing Constraints Wizard</li> <li>Figure 14: Completed Inputs Page of the Timing Constraints Wizard</li> <li>Figure 15: Timing Constraints Wizard</li> <li>Figure 16: Timing Constraints Window</li> <li>Figure 18: Choose Start Points Window for set_false_path Dialog Box</li> <li>Figure 19: Completed set_false_path Constraint Window</li> </ul>	2019.1 release figure updates.





Figure 21: Set Multicycle Path – Options Tab
Figure 23: timing.xdc Tab





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### Using Constraints Tutorial

**IMPORTANT:** This tutorial requires the use of the Kintex®-7 family of devices. You will need to update your Vivado® tools installation if you do not have this device family installed. Refer to the Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973) for more information on Adding Design Tools or Devices.

### **Overview**

This tutorial is comprised of two labs that demonstrate aspects of constraining a design in the Vivado Design Suite. The constraints format supported by the Vivado Design Suite is called Xilinx® Design Constraints (XDC), which is a combination of the industry standard Synopsys® Design Constraints and proprietary Xilinx constraints. For more information on Timing Closure, see the *UltraFast Design Methodology Timing Closure Quick Reference Guide* (UG1292).

**VIDEO:** You can also learn more about defining constraints in the Vivado Design Suite by viewing the quick take video at <u>Vivado Design Constraints Overview</u>

**TRAINING:** Xilinx provides training courses that can help you learn more about the concepts presented in this document. Use these links to explore related courses:

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Essentials of FPGA Design

<u>Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints</u>

XDCs are not just simple strings; they are Tcl commands that the Vivado Tcl interpreter sequentially reads and parses. You can enter design constraints in several ways at different points in the design flow. You can store XDCs in one or more files that can be added to a constraint set in Vivado Project Mode, or read the same files directly into memory using the read\_xdc command in Non-Project mode. For more information on Project and Non-Project modes, refer to the *Vivado Design Suite User Guide: Design Flows Overview* (UG892). With a design open in Vivado tools, you can also type constraints as commands directly in the Tcl console when working in the Vivado IDE or at the Tcl command prompt when working outside of the IDE. This is particularly powerful for defining, validating, and debugging new constraints interactively in the design.

The Vivado Design Suite synthesis and implementation tools are timing driven. Having accurate and correct timing constraints is vital for meeting design goals and ensuring correct operation. Because the Vivado tools are timing driven, it is important to fully constrain a design, but not over-constrain, or under-constrain it. Over-constraining a design can lead to long run-times and sub-optimal results because the tool can struggle with unrealistic design objectives. Under-constraining a design can cause





the Vivado tools to perform unnecessary optimizations, such as examining paths with multicycle delays or false paths, and prevent focus on the real critical paths.

This tutorial discusses different methods for defining and applying design constraints.

### **Tutorial Design Description**

The sample design used throughout this tutorial consists of a small design called project\_cpu\_netlist. There is a top-level EDIF netlist source file, as well as an XDC constraints file.

The design targets an XC7K70T device. A small design is used to allow the tutorial to be run with minimal hardware requirements and to enable timely completion of the tutorial, as well as to minimize the data size.

### Hardware and Software Requirements

This tutorial requires that the 2016.3 Vivado Design Suite software release or later is installed.

See the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973) for a complete list and description of the system and software requirements.

### **Preparing the Tutorial Design Files**

You can find a ZIP file containing the files for this tutorial in the examples directory of the Vivado Design Suite software installation, at the following location:

<Vivado\_install\_area>/Vivado/<version>/examples/Vivado\_Tutorial.zip

Extract the ZIP file contents from the software installation into any write-accessible location.

The location of the extracted Vivado\_Tutorial directory is referred to as the <*Extract\_Dir*> in this Tutorial.

You can also extract the provided ZIP file at any time to restore the files to their starting condition.

**Note:** You will modify the tutorial design data while working through this tutorial. Use a new copy of the original Vivado\_Tutorial directory each time you start this tutorial.





### Lab 1: Defining Timing Constraints and Exceptions

### Introduction

In this lab, you will learn two methods of creating constraints for a design. You will use the Kintex®-7 CPU Netlist example design that is included in the Vivado<sup>®</sup> IDE.

### **Step 1: Opening the Example Project**

Open Vivado IDE:

#### On Linux:

- Change to the directory where the lab materials are stored: cd <Extract Dir>/Vivado Tutorial
- 2. Launch the Vivado IDE: vivado

#### **On Windows:**

1. Launch the Vivado Design Suite IDE:

#### Start > All Programs > Xilinx Design Tools > Vivado 2019.x > Vivado 2019.x

**Note:** Your Vivado Design Suite installation might be called something other than Xilinx Design Tools on the Start menu.

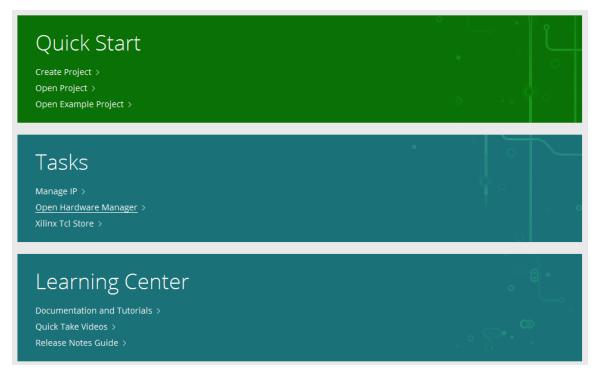
Note: As an alternative, click the Vivado 2019.x Desktop icon to start the Vivado IDE.

The Vivado IDE Getting Started page contains links to open or create projects and to view documentation.

2. From the Getting Started page, click **Open Example Project**, as shown in the following figure.







#### Figure 1: Open Example Project

The Open Example Project wizard opens to the Open Example Project page, as shown in the following figure.

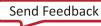




🝌 Open Example Proje	ect	$\times$
HLX Editions	Create an Example Project This wizard will guide you through the creation of a new Vivado project from a predefined template. To create a Vivado project you will specify the type of template project you would like to create. Next, you will need to provide a name and a location for your project files and choos a default board.	;e
E XILINX.		
(?)	< <u>B</u> ack <u>N</u> ext > <u>F</u> inish Cance	I

Figure 2: Create an Example Project Page of the Open Example Project Wizard

- 3. Click Next.
- 4. In the Select Example Project page, select **CPU (Synthesized)**, as shown in the following figure.





🍌 Open Example Project				$\times$
Select Project Template Select one of the below predefined templates on which	to base your new project			4
Templates	Description			
Base Zynq UltraScale+ MPSoC Base MicroBlaze Base Zynq BFT Configurable MicroBlaze Design	CPU (Synthesized) Large synthesized netlist GT IOs	t project Wishbo	one	
Select Project Template Select one of the below predefined templates on which Templates Base Zynq UltraScale+ MPSoC Base MicroBlaze Base Zynq BFT	Open RIS			
	FFT Engine	BFT	USB 1	>
(?)	< <u>B</u> ack	<u>N</u> ext >	Einish	Cancel

Figure 3: Select Example Project Page of the Open Example Project Wizard

5. Click Next.





6. In the Project Name page, specify the project name and location, as shown in the following figure.

🝌 Open Examp	le Project			$\times$
Project Name				
Enter a name for yo	our project and specify a directory where the project d	ata files will be stored		
<u>P</u> roject name:	project_cpu_netlst			
Project location:	C://ivado_Tutorial			⊗ …
🕑 Create projec	t subdirectory			
Project will be cr	eated at: C:/Vivado_Tutorial/project_cpu_netIst			
?	<	<u>B</u> ack <u>N</u> ext >	Einish	Cancel

#### Figure 4: Project Name Page of the Open Example Project Wizard

- 7. Specify the following:
  - Project name: project\_cpu\_netlist
  - Project location: <Extract\_Dir>
- 8. Click Next.





9. In the Default Part page, select the default part as shown in the following figure.

A	Open Example F	Project							$\times$
	efault Part 100se a default Xilinx	: part for your proj	iect.						A
	Search: Q+			<b>~</b>					
	Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb 1
	xc7k70tfbg676-2	676	300	41000	82000	135	0	240	8
	<								>
(	?			< <u>B</u> ac	k 📃	<u>N</u> ext >	<u>F</u> inish	Ca	ancel

Figure 5: Default Part Page of the Open Example Project Wizard





A New Project Summary appears, as shown in the following figure.

🙏 Open Example Proj	ect	$\times$
HLx Editions	<ul> <li>New Project Summary</li> <li>A new project named 'project_cpu_netlst' will be created from the 'CPU (Synthesized)' template.</li> <li>The default part and product family for the new project: Default Part: xc7k70tfbg676-2 Product: Kintex-7 Family: Kintex-7 Package: fbg676 Speed Grade: -2</li> </ul>	
E XILINX.	To create the project, click Finish	
?	< <u>B</u> ack <u>N</u> ext > <u>Einish</u> Cance	I

Figure 6: New Project Summary Page of the Open Example Project Wizard

10. Click **Finish** to finish creating the project.





The Vivado IDE displays the default view of the opened project, as shown in the following figure.

🝌 project_cpu_netlst - [C:/Vivado_T	utorial/project_	cpu_netlst/pr	oject_cpu_net	lst.xpr]	- Viva	do 201	9.1					_		×
<u>File Edit Flow Tools Reports</u>	<u>W</u> indow La	vout <u>V</u> iew	Help Q- Q	uick Acc	ess									Ready
	ι: Ο	<u>11.</u>	×									Defa	ult Layout	~
Flow Navigator 😤 🚔 ? 🔔	PROJECT MANAG	ER - project_cp	u_netist											? ×
✓ PROJECT MANAGER	Sources			2	00	~	Draiaa	t Summa	-				0	o c x
🍄 Settings		+ 2+		£ _		ò			-				f	
Add Sources						*	Overv	niew ∣ Da	ashboard					\$
Language Templates	> Design So						Setti	ngs Ed	it					ï
<ul> <li>SIMULATION</li> <li>Run Simulation</li> </ul>	> 🗁 Simulation > 🗁 Utility Sour	-Only Sources (	1)				Proje	ect name: ect location	n: C:/	ject_cpu_netIst /ivado_Tutorial/pr tov 7	oject_cp	pu_net	tist	
✓ NETLIST ANALYSIS		mpile Order					Proje Top	uct family: ect part: module na	xc7 ame: top					
> Open Synthesized Design	Properties			? _		×		et langua; Jator lang						
✓ IMPLEMENTATION				+	⇒	•	-			-				
Run Implementation							Imple	ementatio	n					
> Open Implemented Design		Select an objec	t to see propertie	es			Statu	IS:		Not started	warning	10		~
Y PROGRAM AND DEBUG							<							>
👫 Generate Bitstream	Tcl Console	Nessages L	og Reports	Desigr	n Runs	×							?	_ 🗆 🖾
> Open Hardware Manager	Q		▶   ≫   <b>+</b>	%										
	Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM I
	▷ impl_1	constrs_2	Not started											
	<					,								>

**Figure 7: Project Default View** 







### **Step 2: Defining Constraint Sets and Files**

Start by creating a new constraint set and adding an empty XDC constraints file to it. The example design already contains two constraint sets, but you do not use them for this lab.

- 1. From the Flow Navigator, click Add Sources in the Project Manager section.
- 2. From the Add Sources dialog box, select Add or create constraints.
- 3. Click Next.
- 4. From the Add or Create Constraints dialog box, use the Specify Constraint Set drop-down menu to select **Create Constraint Set** as shown in the following figure.



Figure 8: Create Constraint Set Drop-Down Menu

- 5. In the Create Constraint Set dialog box, specify the constraint set name as **lab1** and click **OK**.
- 6. Enable the **Make active** check box.
- 7. Click the **Add** button <sup>+</sup> and select **Create File** to add a new XDC file to the project.
- 8. The Create Constraints File dialog box appears.

🝌 Create Co	nstraints File	×
Create a new co	onstraints file and add it to your project	4
<u>F</u> ile type:	T XDC	~
F <u>i</u> le name:		
Fil <u>e</u> location:	<local project="" to=""></local>	~
?	OK	el

Figure 9: Create Constraints File Dialog Box





- 9. Type timing as the file name, and leave the file location set to <Local to Project>.
- 10. Click **OK**.

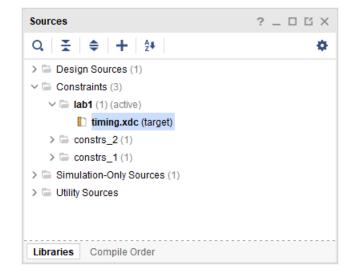
The timing.xdc file is added to the lab1 constraint set.

11. Click Finish to complete the creation of the new constraint set and XDC file.

You should see the new constraint set and XDC file in the Sources window, as shown in the following figure. The constraint set is made active, as you directed when you created it.

12. In the Sources window (shown in the following figure), right-click timing.xdc and select **Set as** Target Constraint File.

This sets the timing.xdc file as the target XDC file. All constraints added to the design are saved in the target XDC file.



#### Figure 10: Sources Window

### **Step 3: Creating Timing Constraints**

In this step, you will open the synthesized design and use the Vivado® Timing Constraints wizard. The Timing Constraints wizard analyzes the gate level netlist and finds missing constraints. Use the Timing Constraints wizard to generate constraints for this design.

- 1. From the Flow Navigator, click Open Synthesized Design.
- 2. When the synthesized design opens, click **Constraints Wizard** under the Synthesized Design section.

The introduction page of the Timing Constraints wizard appears. This page describes the types of constraints that the wizard creates: Clocks, Input and Output Ports, and Clock Domain Crossings.

3. After reading the page, click **Next** to continue.





The Primary Clocks page of the Timing Constraints wizard displays all the clock sources with a missing clock definition. For this design, the wizard detected five missing clock constraints that are needed to time logical paths, and four missing clock constraints that are only needed to verify pulse width and minimum or maximum period requirements.

Recon	nmended Constrai	ints					
Q,	13 🖉 🛄						
	Object	Name	Frequency (MHz)	Period (ns)	Rise At (ns)	Fall At (ns)	Jitter (ns)
	M TXOUTCLK	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROC	undefined	undefined			
	M TXOUTCLK	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROC	undefined	undefined			
	TXOUTCLK	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROC	undefined	undefined			
	M TXOUTCLK	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROC	undefined	undefined			
	III sysClk	sysClk	undefined	undefined			

Constraints for Pulse Width Check Only	Constraints	for Pulse	Width	Check Only
--	-------------	-----------	-------	------------

Q,	🕸 🖉 📅						
	Object	Name	Frequency (MHz)	Period (ns)	Rise At (ns)	Fall At (ns)	Jitter (ns)
	I TILE0_REFCLK_PAD_P_IN	TILE0_REFCLK_PAD_P_IN	undefined	undefined			
	I TILE1_REFCLK_PAD_P_IN	TILE1_REFCLK_PAD_P_IN	undefined	undefined			
	I TILE2_REFCLK_PAD_P_IN	TILE2_REFCLK_PAD_P_IN	undefined	undefined			
	I TILE3_REFCLK_PAD_P_IN	TILE3_REFCLK_PAD_P_IN	undefined	undefined			

Figure 11: Clock Sources with Missing Clock Definitions

You will fill in the periods for the five missing primary clocks in the design. The second category of clocks, shown in the Constraints for Pulse Width Check Only table, is optional. For this example, do not add these last constraints.

4. In the Recommended Constraints table, each row of the wizard is a missing constraint. To specify a constraint in the table, click the cell in the period column for the clock and type the value from Table 1 to fill in the periods of the five missing primary clocks in the design. When you set the period for a clock, the frequency is automatically populated.





#### Table 1: Values to Use on the Primary Clock Page of the Wizard

Primary Clock	Period (ns)
mgtEngine/ROCKETIO_WRAPPER_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT	12.8
mgtEngine/ROCKETIO_WRAPPER_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT	12.8
mgtEngine/ROCKETIO_WRAPPER_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT	12.8
mgtEngine/ROCKETIO_WRAPPER_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT	12.8
sysClk	10.0

If you do not want to enter a constraint for a specific clock, uncheck the box next to the clock.

For more information about how the wizard finds these missing constraints, click the Quick Help button ("?") in the lower left-hand corner of the wizard. The quick help pages are context specific and contain more information about the topologies the wizard is looking for and an explanation as to why the constraint is being suggested.

The completed page looks like the following figure.





 $\times$ 

1

🝌 Timing Constraints Wizard

#### **Primary Clocks**

Primary clocks usually enter the design though input ports. Specify the period and optionally a name and waveform (rising and falling edge times) to describe the duty cycle if not 50%. More info

<	Object	Name		Frequency (	MHz)	Period (ns)	Rise At (r	ns) Fall A	t (ns)	Jitter (ns)
	M TXOUTCLK	mgtEngine/RO	CKETIO_WRAPPER_TILE_i/gt0		3.125	12.800	0.0	000	6.400	
<	M TXOUTCLK	mgtEngine/R0	CKETIO_WRAPPER_TILE_i/gt2	_ROC 7	3.125	12.800	0.0	000	6.400	
✓	TXOUTCLK	mgtEngine/RO	CKETIO_WRAPPER_TILE_i/gt4	_ROC 7	3.125	12.800	0.0	000	6.400	
	M TXOUTCLK	mgtEngine/RO	CKETIO_WRAPPER_TILE_i/gt6	_ROC 7	3.125	12.800	0.0	000	6.400	
	I sysClk	sysClk		10	0.000	10.000	0.0	000	5.000	
<b>Q</b>	tte ⊘ ⊥⊥ Object		Name	Frequency (MHz)			e At (ns)	Fall At (ns)	Jitter (	ns)
	Object		Name	Frequency (MHz)	Perio	d (ns) Rise	e At (ns)	Fall At (ns)	Jitter (	ns)
		_REFCLK_PAD_P_IN TILE0_REFCLK_PAD_P_IN		undefined		defined				
	M TILE1_REFCL		TILE1_REFCLK_PAD_P_IN	undefined		efined				
			TILE2_REFCLK_PAD_P_IN	undefined		efined				
	IUL HLE3_REFUL	K_PAD_P_IN	TILE3_REFCLK_PAD_P_IN	undefined	und	efined				
	command Preview (	5) Evicting	Create Clock Constraints (0)							
	ommanu Preview (	5) Existing (								
Q,										
		-	ngine/ROCKETIO_WRAPPER_T ngine/ROCKETIO WRAPPER T		_	_		_		-
		-	ngine/ROCKETIO_WRAPPER_T		_	_		_		
		_	ngine/ROCKETIO_WRAPPER_T		IO_WR	APPER_TILE	_i/GT6_TX	DUTCLK_O	UT -wav	eform {0.000
reate	e_clock -period 10.0	00 -name sysC	lk -waveform {0.000 5.000} [get_]	ports {sysClk}]						
										>

Figure 12: Completed Primary Clocks Page of the Timing Constraints Wizard

5. Click **Next** to continue.

The primary clock constraints have been added to the design. Next, the wizard looks for unconstrained generated clocks. Generated clocks are derived from primary clocks in the FPGA fabric. A good example would be a binary counter used to create a divided clock.

In this design, the wizard determined that there are no unconstrained generated clocks.

6. Click **Next** to continue.





Next, the wizard looks for forwarded clocks. A forwarded clock is a generated clock on a primary output port of the FPGA. These are commonly used for source synchronous buses when the capture clock travels with the data.

The wizard has determined that there are no unconstrained forwarded clocks in the design.

7. Click **Next** to continue.

Next, the wizard looks for external feedback delays. MMCM or PLL feedback delay outside the FPGA is used to compute the clock delay compensation in the timing reports.

The wizard did not find any unconstrained MMCM external feedback delays in the design.

8. Click **Next** to continue.

Next, the wizard looks at the input delays. The following figure shows the Input Delay page of the Timing Constraints wizard. There are three sections to the page.





ion	nmended Constraints								1	Delay Parameters		
)	Interface	Clock	Synchronous	^1	Alignment	^ 2	Data Rate and Edge	^3		Clock period:	10	ns
)	DataIn_pad_0_i[*]	I sysClk	System	~	Edge	× .	Single Rise	~	^	· ·		
9	DataIn_pad_1_i[*]	SysClk	System	~	Edge	~	Single Rise	$\sim$	Ш	tco_min:	undefined	ns
)	LineState_pad_0_i[*]	M sysClk	System	~	Edge	~	Single Rise	~		tco_max:	undefined	ns
)	LineState_pad_1_i[*]	III sysClk	System	~	Edge	~	Single Rise	~		trce_dly_min:	undefined	ns
)	VStatus_pad_0_i[*]	SysClk	System	~	Edge	~	Single Rise	$\sim$	Ш	tree dly max:	undefined	
)	VStatus_pad_1_i[*]	SysClk	System	~	Edge	~	Single Rise	~	Ш	trce_dly_max:	undelined	ns
)	GTPRESET_IN	👖 mgtEngi	System	~	Edge	~	Single Rise	$\sim$	Ш		D	
)	GTPRESET_IN	👖 mgtEngi	System	~	Edge 🖊 🔪	~	Single Rise	~			D	
)	GTPRESET_IN	👖 mgtEngi	System	~	Edge	~	Single Rise	~				
)	GTPRESET_IN	👖 mgtEngi	System	~	Edge	~	Single Rise	~		Rise Max = tco_m	ax + trce_dly_max	
)	? RxActive_pad_0_i	SysClk	System	~	Edge	~	Single Rise	~		Rise Min = tco_mi	in + trce_dly_min	
9	? RxActive_pad_1_i	SysClk	System	~	Edge	~	Single Rise	~				
)	? RxError_pad_0_i	SysClk	System	~	Edge	~	Single Rise	~		[		
9	? RxError_pad_1_i	M sysClk	System	~	Edge	~	Single Rise	~	~		Apply	
	input clock data	Existing Set Inp	uut Delay Constrai	XXX	min + trce_dly_	<b>C</b>	data					_

Figure 13: Input Delay Page of Timing Constraints Wizard Showing the Major Sections

In section A, you can see all the input ports that are missing input delay constraints in the design. In this table, you select the timing template you would like to use to constrain the input.

In section B, you provide the delay values for the template. This section will change depending on the template chosen in section A.

In section C, there are three tabs:

- **Tcl Command Preview** previews the Tcl commands that will be used to constrain the design.
- Existing Set Input Delay Constraints shows input delay constraints that exist in the design.
- **Waveform** displays the waveform associated with the template.





Next, you will fill out the form based on Table 2.

- 1. Click the **Clock** column header to sort the table alphabetically by clock name.
- 2. Select the template in section A, enter the values in section B, and observe the Tcl commands, existing input delays, and the template specific waveform in section C.

Skip entering the first four constraints shown in Table 2 by unchecking the box to the left of the constraint. In this particular case, you false path these paths from the GTPRESET\_IN port later, as it is an asynchronous reset signal synchronized inside the design.

The blocks of colored rows in Table 2 can all be entered at the same time in the Input Delays page of the Timing Constraints wizard, shown in Figure 14, page 23, by selecting multiple rows in the wizard (use the **Shift** or **Ctrl** buttons and click to select multiple rows) and then entering the values once. Some inputs are constrained relative to virtual clocks, since they are captured by an internal generated clock with a waveform different than the board clock. In this case, the wizard creates a virtual clock with the same frequency and waveform as the internal clock, and recommends a constraint relative to the virtual clock.

Table 2 is shaded to indicate which groups of signals can be entered in this manner.

Interface	Clock	Synchronous	Alignment	Data Rate and Edge	tco_min (ns)	tco_max (ns)	trce_dly_min (ns)	trce_dly_max (ns)
GTPRESET_IN	mgtEngine/	System	Edge	Single Rise	ι	Jncheck cons	traint – will false pa	th later
GTPRESET_IN	mgtEngine/	System	Edge	Single Rise	ι	Jncheck cons	traint – will false pa	th later
GTPRESET_IN	mgtEngine/	System	Edge	Single Rise	ι	Jncheck cons	traint – will false pa	th later
GTPRESET_IN	mgtEngine/	System	Edge	Single Rise	ι	Jncheck cons	traint – will false pa	th later
DataIn_pad_0_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
DataIn_pad_1_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
LineState_pad_0_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
LineState_pad_1_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
VStatus_pad_0_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
VStatus_pad_1_i[*]	sysClk	System	Edge	Single Rise	1	2	1	1
RxActive_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
RxActive_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
Rx_Error_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
Rx_Error_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
Rx_Valid_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
Rx_Valid_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
TxReady_pad_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
TxReady_pad_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
usb_vbus_paf_0_i	sysClk	System	Edge	Single Rise	1	2	1	1
usb_vbus_paf_1_i	sysClk	System	Edge	Single Rise	1	2	1	1
or1200_clmode	VIRTUAL_cpuClk_5	System	Edge	Single Rise	0.1	2.5	0.1	0.2
or1200_pic_ints	VIRTUAL_cpuClk_5	System	Edge	Single Rise	0.1	2.5	0.1	0.2
reset	VIRTUAL_cpuCLK_5	System	Edge	Single Rise	0.1	2.5	0.1	0.2

#### **Table 2: Input Constraint Values**

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3. The following figure shows the completed input delay page. Note the four constraints being skipped.

Image: Section of the section of th	Image: Contract of the contract	Imported       Option	Inductor       Openance       Openance <td< th=""><th>Image: Section of the section of th</th><th>Immedia       One of the model       Angentiant       One of the reset of the</th><th>Image: Sector of the sector</th><th></th><th>🕸 🖪 🖬 🗸</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>Delay Parameter</th><th></th><th></th></td<>	Image: Section of the section of th	Immedia       One of the model       Angentiant       One of the reset of the	Image: Sector of the sector		🕸 🖪 🖬 🗸								Delay Parameter		
Do Grif REEET_IN       Iul migeingi System       Edge       Single Rise         Do GTPRESET_IN       Iul migeingi System       Edge       Single Rise         Do Datain_pad_0_it*       Iul sysCik       System       Edge       Single Rise         Do Datain_pad_0_it*       Iul sysCik       System       Edge       Single Rise         Do Datain_pad_0_it*       Iul sysCik       System       Edge       Single Rise         Do LineState_pad_0_it*       Iul sysCik       System       Edge       Single Rise         Do LineState_pad_0_it*       Iul sysCik       System       Edge       Single Rise         Do Xstatus_pad_0_it*       Iul sysCik       System       Edge       Single Rise         Do RxActive_pad_0_i       Iul sysCik       System       Edge       Single Rise         Do RxError_pad_0_i       Iul sysCik       System       Edge       Single Rise       Image: Single Rise         Do RxError_pad_1_i       Iul sysCik       System       Edge       Single Rise       <	Do Grif RESET_IN       ILI mgLengi Gystem       Edge       Single Rise         D G GTPRESET_IN       ILI mgLengi System       Edge       Single Rise         D G GTPRESET_IN       ILI mgLengi System       Edge       Single Rise         D G GTPRESET_IN       ILI mgLengi System       Edge       Single Rise         D G GTPRESET_IN       ILI mgLengi System       Edge       Single Rise         D DataIn_pad_0_it*       ILI mgLengi System       Edge       Single Rise         D DataIn_pad_1_it*       ILI mgLengi System       Edge       Single Rise         D DataIn_pad_0_it*       ILI mgLengi System       Edge       Single Rise         D DataIn_pad_1_it*       ILI sysCik System       Edge       Single Rise         D LineState_pad_0_it*       ILI sysCik System       Edge       Single Rise         D V Status_pad_0_i*       ILI sysCik System       Edge       Single Rise         D RxActive_pad_0_i       ILI sysCik System       Edge       Single Rise         D RxActive_pad_0_i       ILI sysCik System       Edge       Single Rise         D RxActive_pad_0_i       ILI sysCik System       Edge       Single Rise         D RxActive_pad_1_i       ILI sysCik System       Edge       Single Rise         D RxError_pad_0_i	Image Ryse       Edge       Single Rise         Image Ryse       Edge       Single Rise         Image Ryse       System       Edge       Single Rise       Image Ryse         Image Ryse       System       Edge       Single Rise       Image Ryse         Image Ryse       System       Edge       Single Rise       Image Ryse         Image Ryse       System       Edge       Single Rise       Image Ryse       Image Ryse         Image Ryse       System       Edge       Single Rise       Image Ryse       Image Ryse       Image Ryse       Image Ryse         Image Ryse       System       Edge       Single Rise       Image Ryse	Image: Type Contracted in Migling Oystem       Edge       Single Rise         Image: Type Set Type Set Type Set Type System       Edge       Single Rise         Image: Type Set Type Set Type Set Type Set Type System       Edge       Single Rise         Image: Type Set Type Set Type Set Type System       Edge       Single Rise         Image: Type Set Type Set Type Set Type System       Edge       Single Rise         Image: Type Set Type Set Type Set Type System       Edge       Single Rise         Image: Type Set	Image: high reset       Edge       Single Rise         Image: high reset       Image: high reset       Single Rise         Image: high reset       Image: high reset       Single Rise         Image: high reset       Image: high reset       Single Rise         Image: high reset       Single Rise       Single Rise         Image: high reset       Image: high reset       Single Rise         Image: high reset       Image: high reset       Single Rise         Image: high reset       Single Rise       Single Rise       Single Rise         Image: high reset       Single Rise       Single Rise       Single Rise       Single Rise         Ima	D       OF OFFRESET_IN       III mgEngi       System       Edge       Single Rise         D       OF GTPRESET_IN       III mgEngi       System       Edge       Single Rise         D       OF GTPRESET_IN       III mgEngi       System       Edge       Single Rise         D       OF GTPRESET_IN       III mgEngi       System       Edge       Single Rise         D       D Dataln_pad_0_1[*]       III sysClk       System       Edge       Single Rise         D       D Dataln_pad_1_1[*]       III sysClk       System       Edge       Single Rise         D       D Dataln_pad_0_1[*]       III sysClk       System       Edge       Single Rise         D       D Dataln_pad_1_1[*]       III sysClk       System       Edge       Single Rise         D       LineState_pad_0_1[*]       III sysClk       System       Edge       Single Rise         D       LineState_pad_0_1[*]       III sysClk       System       Edge       Single Rise         D       VStatus_pad_0_1[*]       III sysClk       System       Edge       Single Rise         D       RxActive_pad_0_1       III sysClk       System       Edge       Single Rise         D       RxActive_pad_0_1	D       Origin Reserve       Edge       Single Rise         D       Origin Reserve       Single Rise       Single Rise         D       D Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         D       D Dataln_pad_1_i(*)       III sysClk       System       Edge       Single Rise         D       D Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         D       D Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         D       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise         D       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise         D       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise         D       N VStatus_pad_0_i       III sysClk       System       Edge       Single Rise         D       RxActive_pad_0_i       III sysClk       System <t< th=""><th></th><th>Interface</th><th>Clock ^1</th><th>Synchronous</th><th></th><th>Alignment</th><th></th><th>Data Rate and Edge</th><th></th><th>Clock period:</th><th>10</th><th>ns</th></t<>		Interface	Clock ^1	Synchronous		Alignment		Data Rate and Edge		Clock period:	10	ns
Image: Contract of the series of the seri	Image: Preser in v       Introduction System       Edge       Single Rise         Image: Preser in v       Image: Preser in v       Image: Preser in v       Image: Preser in v       Edge       Single Rise         Image: Preser in v       Image: Preser in v       Image: Preser in v       Image: Preser in v       Edge       Single Rise         Image: Preser in v       Image: Preser in v       Image: Preser in v       Edge       Single Rise       V         Image: Preser in v       Image: Preser in v       Edge       Single Rise       V       Tree_dly_min:       1@ ns         Image: Preser in v       Image: Preser in v       Edge       Single Rise       V       Tree_dly_min:       1@ ns         Image: Preser in v       Image: Preser in v       Edge       Single Rise       V       Tree_dly_max       1@ ns         Image: Preser in v       Image: Preser in v       Edge       Single Rise       V       Tree_dly_max       1@ ns         Image: Preser in v       VStatus_pad_0_i(")       Image: Preser in v       Edge       Single Rise       V       Rise Max = tco_max + tree_dly_max         Image: Preser in v       VStatus_pad_0_i       Image: Preser in v       Edge       Single Rise       V         Image: Preser in v       Image: Preser in v       Image	Image: Presser JN       Im	Image: Comparison of the comparison of thequation of the comparison of the comparison of the comparison of	Image: Signation of the section of the system       Edge       Single Rise         Image: Signation of the system       Edge       Single Rise	Image: Presser in the inglering system       Edge       Single Rise         Image: Presser in the inglering system       Edge       Single Rise         Image: Presser in the inglering system       Edge       Single Rise         Image: Presser in the inglering system       Edge       Single Rise         Image: Presser in the inglering system       Edge       Single Rise         Image: Presser in the inglering system       Edge       Single Rise         Image: Presser in the inglering system       Edge       Single Rise         Image: Presser in the inglering system       Edge       Single Rise         Image: Presser ingleringlering system<	Image: System       Edge       Single Rise         Image: System	_	? GTPRESET_IN				Edge		Single Rise				
Image: Second System       Edge       Single Rise         Image: System	Image: Second System       Edge       Single Rise         Image: System	Image: Section of the system       Edge       Single Rise         Image: Rise Rise       Single Rise       Single Rise	Image: Second System       Edge       Single Rise         Image: Rise </td <td>Image: Second Second</td> <td>Image: Second System       Edge       Single Rise         Image: System</td> <td>?       GTPRESET_IN       III mgtEngi       System       Edge       Single Rise         ?       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         ?       Dataln_pad_1_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_min:       1@ ns         ?       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_max       1@ ns         ?       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_max       1@ ns         ?       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       *         ?       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       *         ?       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       *         ?       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise       *         ?       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       *         ?       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       <t< td=""><td>_</td><td></td><td></td><td></td><td></td><td>Edge</td><td></td><td>Single Rise</td><td></td><td>ico_min.</td><td></td><td></td></t<></td>	Image: Second	Image: Second System       Edge       Single Rise         Image: System	?       GTPRESET_IN       III mgtEngi       System       Edge       Single Rise         ?       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         ?       Dataln_pad_1_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_min:       1@ ns         ?       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_max       1@ ns         ?       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_max       1@ ns         ?       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       *         ?       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       *         ?       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       *         ?       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise       *         ?       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       *         ?       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise <t< td=""><td>_</td><td></td><td></td><td></td><td></td><td>Edge</td><td></td><td>Single Rise</td><td></td><td>ico_min.</td><td></td><td></td></t<>	_					Edge		Single Rise		ico_min.		
Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_0_i       Image: System       Edge       Single Rise         Image	Image: Dataln_pad_0_i[*]       Image: System       Edge       Single Rise         Image: Dataln_pad_1_i[*]       Image: System       Edge       Single Rise         Image: Dataln_pad_1_i[*]       Image: System       Edge       Single Rise       Image: System         Image: Dataln_pad_1_i[*]       Image: System       Edge       Single Rise       Image: System       Image: System </td <td>Image: Classing of the system       Image: Classing of the system       Edge       Single Rise         Image: Classing of the system       Edge       Single Rise       Image: Classing of the system       Image: Class</td> <td>Image: Clic System       Edge       Single Rise         Image: Clic Sys</td> <td>Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise       Image: Comparison of the comparison</td> <td>2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_max:       10 ns         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise          2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise          2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise          2       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise          2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise          2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise          2       RxActive_pad_0_i       III sysClk       System       Edge       Single R</td> <td>2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       Itce_diy_min:       Itce_diy_min:</td> <td>_</td> <td></td> <td></td> <td>-</td> <td></td> <td>-</td> <td></td> <td>Single Rise</td> <td></td> <td>tco_max:</td> <td>2 🛞</td> <td>ns</td>	Image: Classing of the system       Image: Classing of the system       Edge       Single Rise         Image: Classing of the system       Edge       Single Rise       Image: Classing of the system       Image: Class	Image: Clic System       Edge       Single Rise         Image: Clic Sys	Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise       Image: Comparison of the comparison	2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_max:       10 ns         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise          2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise          2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise          2       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise          2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise          2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise          2       RxActive_pad_0_i       III sysClk       System       Edge       Single R	2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       Itce_diy_min:	_			-		-		Single Rise		tco_max:	2 🛞	ns
Image: Single Rise of the system of the s	Image: Constraints (Image: Constrai	Image: Second	Image: Second	Image: Second state st	Image: Construction of the system of the	Image: Construction of the system of the								-		trce_dly_min:	1 🛛	ns
Image: System of the system	Image: System of the system	Image: System of the system	Image: System of the system	✓       Datain_pad_1[1]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       LineState_pad_0_[1]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       LineState_pad_0_[1]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       LineState_pad_0_[1]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       V Status_pad_0_[1]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       V Status_pad_0_1[1]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       N Xstatus_pad_0_1       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       RxActive_pad_1_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       RxError_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       RxError_pad_1_i       III sysClk       S	Image: DataIn_pad_1_i(*)       Image: System       Edge       Single Rise       Single Rise         Image: DataIn_pad_1_i(*)       Image: System       Edge       Single Rise       Single Rise       Single Rise         Image: DataIn_pad_1_i(*)       Image: System       Edge       Single Rise       Single Ri	Image: Datain_pad_1_(!)       Image: System       Edge       Single Rise       Single Rise         Image: Datain_pad_1_(!)       Image: System       Edge       Single Rise       Single Rise       Single Rise         Image: Datain_pad_1_(!)       Image: System       Edge       Single Rise       Single Rise<	_					-		-		trce dly max	1 🕅	ns
ImeState_pad_1_i(*)       Imagesting       System       Edge       Single Rise       Imagesting       Imagesting <td>ImeState_pad_1_i(*)       Imagesting       System       Edge       Single Rise       Imagesting       Imagesting<td>Image: State_pad_1_i(*)       Image: System       Edge       Single Rise       Image: Single Rise</td><td>Image: Second system       Edge       Single Rise         Image: Second system       Edge       Single Rise</td><td>✓       LineState_pad_1_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       VStatus_pad_0_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       VStatus_pad_0_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       NxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxError_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxError_pad_1_i       III sysClk       System       ✓       Edge       ✓       Single Ri</td><td>Image: Single Rise pad_1_i(*)       Image: System with the system withten with the system withe system withe system with the system with the system wi</td><td>Image: Single Rise pad_1_i(*)       Image: System view       Edge view       Single Rise view         Image: System view       Edge view       Single Rise view</td><td>_</td><td></td><td></td><td>-</td><td></td><td>-</td><td></td><td>_</td><td></td><td>acc_ay_max.</td><td>10</td><td></td></td>	ImeState_pad_1_i(*)       Imagesting       System       Edge       Single Rise       Imagesting       Imagesting <td>Image: State_pad_1_i(*)       Image: System       Edge       Single Rise       Image: Single Rise</td> <td>Image: Second system       Edge       Single Rise         Image: Second system       Edge       Single Rise</td> <td>✓       LineState_pad_1_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       VStatus_pad_0_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       VStatus_pad_0_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       NxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxError_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxError_pad_1_i       III sysClk       System       ✓       Edge       ✓       Single Ri</td> <td>Image: Single Rise pad_1_i(*)       Image: System with the system withten with the system withe system withe system with the system with the system wi</td> <td>Image: Single Rise pad_1_i(*)       Image: System view       Edge view       Single Rise view         Image: System view       Edge view       Single Rise view</td> <td>_</td> <td></td> <td></td> <td>-</td> <td></td> <td>-</td> <td></td> <td>_</td> <td></td> <td>acc_ay_max.</td> <td>10</td> <td></td>	Image: State_pad_1_i(*)       Image: System       Edge       Single Rise       Image: Single Rise	Image: Second system       Edge       Single Rise	✓       LineState_pad_1_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       VStatus_pad_0_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       VStatus_pad_0_i[*]       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ✓       NxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxActive_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxError_pad_0_i       III sysClk       System       ✓       Edge       ✓       Single Rise       ✓         ✓       ○       RxError_pad_1_i       III sysClk       System       ✓       Edge       ✓       Single Ri	Image: Single Rise pad_1_i(*)       Image: System with the system withten with the system withe system withe system with the system with the system wi	Image: Single Rise pad_1_i(*)       Image: System view       Edge view       Single Rise view	_			-		-		_		acc_ay_max.	10	
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      &gt; VStatus_pad_0_i[*]       III sysClk       System       &gt; Edge       &gt; Single Rise       &gt;         ?       &gt; VStatus_pad_1_i[*]       III sysClk       System       &gt; Edge       &gt; Single Rise       &gt;         ?       &gt; RxActive_pad_0_i       III sysClk       System       &gt; Edge       &gt; Single Rise       &gt;         ?       &gt; RxActive_pad_0_i       III sysClk       System       &gt; Edge       &gt; Single Rise       &gt;         ?       &gt; RxActive_pad_0_i       III sysClk       System       &gt; Edge       &gt; Single Rise       &gt;         ?       &gt; RxActive_pad_0_i       III sysClk       System       &gt; Edge       &gt; Single Rise       &gt;         ?       &gt; RxError_pad_0_i       III sysClk       System       &gt; Edge       &gt; Single Rise       &gt;</td> <td>_</td> <td>_</td> <td></td> <td>-</td> <td></td> <td>-</td> <td></td> <td>_</td> <td></td> <td></td> <td></td> <td></td>	2       > VStatus_pad_0_i[*]       III sysClk       System       > Edge       > Single Rise       >         2       > VStatus_pad_1_i[*]       III sysClk       System       > Edge       > Single Rise       >         2       > RXActive_pad_0_i       III sysClk       System       > Edge       > Single Rise       >         2       > RxActive_pad_0_i       III sysClk       System       > Edge       > Single Rise       >         2       > RxActive_pad_0_i       III sysClk       System       > Edge       > Single Rise       >         2       > RxActive_pad_0_i       III sysClk       System       > Edge       > Single Rise       >         3       > RxActive_pad_0_i       III sysClk       System       > Edge       > Single Rise       >         4       > RxError_pad_0_i       III sysClk       System       > Edge       > Single Rise       >	? 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RxActive_pad_1_i                III sysClk             System               Edge               Single Rise                  RxError_pad_0_i               III sysClk             System               Edge               Single Rise                   RxError_pad_0_i               III sysClk             System               Edge               Single Rise               Apply                   RxError_pad_1_i               III sysClk             System               Edge               Single Rise               Appply                 clommand Preview (41)               Existing Set Input Delay Constraints (0)               Waveform - System   Edge   Single Rise	RxActive_pad_1_i                III sysClk             System               Edge               Single Rise                  RxError_pad_0_i               III sysClk             System               Edge               Single Rise                   RxError_pad_0_i               III sysClk             System               Edge               Single Rise               Apply                   RxError_pad_1_i               III sysClk             System               Edge               Single Rise               Appply                 clommand Preview (41)               Existing Set Input Delay Constraints (0)               Waveform - System   Edge   Single Rise	RxActive_pad_1_i                III sysClk             System               Edge               Single Rise                  RxError_pad_0_i               III sysClk             System               Edge               Single Rise               Apply                 RxError_pad_1_i               III sysClk             System               Edge               Single Rise               Apply                 RxError_pad_1_i               III sysClk             System               Edge               Single Rise               Apply                 Clommand Preview (41)             Existing Set Input Delay Constraints (0)             Waveform - System   Edge   Single Rise               Image: Single Rise	Image: RxActive_pad_1_i       Image: RxActive_pad_1_i <td>RxActive_pad_1_i                  RxActive_pad_1_i                                     ■ RxError_pad_0_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                                     ■ RxError_pad_1_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                         ■ RxError_pad_1_i                ■ RxError_pad_1_i                    ■ RxError_pad_1_i</td> <td>P RxActive_pad_1_i       M sysClk       System       Edge       Single Rise          P RxError_pad_0_i       M sysClk       System       Edge       Single Rise</td> <td>P RxActive_pad_1_i       M sysClk       System       V       Edge       V       Single Rise       V         P RxError_pad_0_i       M sysClk       System       V       Edge       V       Single Rise       V</td> <td>_</td> <td></td> <td></td> <td>-</td> <td></td> <td>-</td> <td></td> <td>_</td> <td></td> <td></td> <td></td> <td></td>	RxActive_pad_1_i                  RxActive_pad_1_i                                     ■ RxError_pad_0_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                                     ■ RxError_pad_1_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                ■ RxError_pad_1_i                         ■ RxError_pad_1_i                ■ RxError_pad_1_i                    ■ RxError_pad_1_i	P RxActive_pad_1_i       M sysClk       System       Edge       Single Rise          P RxError_pad_0_i       M sysClk       System       Edge       Single Rise	P RxActive_pad_1_i       M sysClk       System       V       Edge       V       Single Rise       V         P RxError_pad_0_i       M sysClk       System       V       Edge       V       Single Rise       V	_			-		-		_				
		RxError_pad_0_i                M sysClk             System               Edge               Single Rise               Lage               Lage               Lage               Single Rise               Lage	Image: Second system       Image: System       Edge       Single Rise       Image: System       Single Rise       Image: System	RxError_pad_0_i       M sysClk       System       Edge       Single Rise       Apply         RxError_pad_1_i       M sysClk       System       Edge       Single Rise       Apply	RxError_pad_0_i     M sysClk     System     V     Edge     V     Single Rise	D RxError_pad_0_i     M sysClk     System     V     Edge     V     Single Rise	_	_		-		-		_		Rise Min = tco_n	nin + trce_dly_min	
			✓       ▶ RxError_pad_1_i       Ⅲ sysClk       System       ✓       Edge       ✓       Single Rise       ✓       ▲pply         Cl Command Preview (41)       Existing Set Input Delay Constraints (0)       Waveform - System   Edge   Single Rise       ✓       ▲pply	RxError_pad_1_i M sysClk System V Edge V Single Rise V						-		-		_				
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RxActive_pad_1_i                MI sysClk             System               Edge               Single Rise               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Bage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Waveform - System   Edge   Single Rise               Lage               Apply	RxActive_pad_1_i                MI sysClk             System               Edge               Single Rise               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Bage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Waveform - System   Edge   Single Rise               Lage               Apply	RxActive_pad_1_i                MI sysClk             System               Edge               Single Rise               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Bage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Waveform - System   Edge   Single Rise               Lage               Apply	RxActive_pad_1_i                MI sysClk             System               Edge               Single Rise               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Lage               Lage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Bage               Single Rise               Apply                 RxError_pad_1i               MI sysClk             System               Waveform - System   Edge   Single Rise               Lage               Apply	Image: RxActive_pad_1_i       Image: Rxscrvc_pad_0_i       Image: Rxscrvc_pad_0_i       Image: Rxscrvc_pad_0_i       Image: Rxscrvc_pad_1_i	RxActive_pad_1_i                M sysClk             System               Edge               Single Rise               //                 RxActive_pad_0_i               M sysClk             System               Edge               Single Rise	D RxActive_pad_1_i       M sysClk       System       V       Edge       V       Single Rise       V         D RxError_pad_0_i       M sysClk       System       V       Edge       V       Single Rise       V	_			-	~	-	~	_	~			
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   //               //               //               //               //                 //</td><td>P RxActive_pad_1_i       M sysClk       System       V       Edge       V       Single Rise       V         P RxError_pad_0_i       M sysClk       System       V       Edge       V       Single Rise       V</td><td>_</td><td></td><td></td><td>-</td><td></td><td>-</td><td></td><td>_</td><td></td><td></td><td></td><td></td></td<></td></td<></td></td<></td></td<>	Image: Right Section Constraints       Image: Right Section Constraints <td< td=""><td>Image: Right Section Constraints       Image: Right Section Constraints       <td< td=""><td>Image: Right Section Constraints       Image: Right Section Constraints       <td< td=""><td>RxActive_pad_1_i       III sysClk       System       Edge       Single Rise       *         RxError_pad_0_i       III sysClk       System       Edge       Single Rise       *         RxError_pad_1_i       III sysClk       System       Edge       Single Rise       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Image: Datain_pad_0_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_it*i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: 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    It on ns         7       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns         8       Rxterror_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns</td><td></td><td>? GTPRESET_IN</td><td>🕅 mgtEngi</td><td>System</td><td></td><td>Edge</td><td></td><td>Single Rise</td><td></td><td>tco_max:</td><td>2 🛞</td><td>ns</td></t<></td></t<></td></t<>	Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise       Image: Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise       Image: Single Rise       Image: Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise       Image: Single Rise <t< td=""><td>Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System 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Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v</td><td>Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise       Image: System         Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise       Image: System       Image: System</td><td>2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_max:       10 ns         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise       10         2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       10         2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       10         2       RxActive_pad_0_i       III sysClk       System       <t< td=""><td>2       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         2       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         3       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         4       LineState_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_max:       It on ns         3       LineState_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_max:       It on ns         4       VStatus_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It on ns         5       VStatus_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It on ns         6       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns         7       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns         8       Rxterror_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns</td><td></td><td>? GTPRESET_IN</td><td>🕅 mgtEngi</td><td>System</td><td></td><td>Edge</td><td></td><td>Single Rise</td><td></td><td>tco_max:</td><td>2 🛞</td><td>ns</td></t<></td></t<>	Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v	Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_1_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_if*       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v       Edge v       Single Rise v         Image: Datain_pad_0_i       Image: System v	Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_1_i(*)       Image: System       Edge       Single Rise         Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise       Image: System         Image: Datain_pad_0_i(*)       Image: System       Edge       Single Rise       Image: System	2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_min:       10 ns         2       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_diy_max:       10 ns         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise       10         2       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise       10         2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       10         2       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       10         2       RxActive_pad_0_i       III sysClk       System <t< td=""><td>2       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         2       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         3       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         4       LineState_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_max:       It on ns         3       LineState_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_max:       It on ns         4       VStatus_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It on ns         5       VStatus_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It on ns         6       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns         7       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns         8       Rxterror_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns</td><td></td><td>? GTPRESET_IN</td><td>🕅 mgtEngi</td><td>System</td><td></td><td>Edge</td><td></td><td>Single Rise</td><td></td><td>tco_max:</td><td>2 🛞</td><td>ns</td></t<>	2       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         2       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         3       Dataln_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_min:       It on ns         4       LineState_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_max:       It on ns         3       LineState_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It ce_diy_max:       It on ns         4       VStatus_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It on ns         5       VStatus_pad_0_(I^*)       III sysClk       System       Edge       Single Rise       It on ns         6       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns         7       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns         8       Rxterror_pad_0_i       III sysClk       System       Edge       Single Rise       It on ns		? GTPRESET_IN	🕅 mgtEngi	System		Edge		Single Rise		tco_max:	2 🛞	ns
Image: Second System       Edge       Single Rise         Image: System	Image: Second System       Edge       Single Rise         Image: System	Image: Section of the system       Edge       Single Rise         Image: Rise Rise       Single Rise       Single Rise         Image: Rise Rise System       Edge       Single Rise         Image: Rise Rise System       Edge       Single Rise	Image: Section of the system       Edge       Single Rise         Image: Rise Rise       Single Rise       Single Rise         Image: Rise Rise System       Edge       Single Rise         Image: Rise Rise System       Edge       Single Rise	Image: Second System       Edge       Single Rise         Image: System	Image: Second System       Edge       Single Rise         Image: System	?       GTPRESET_IN       III mgtEngi       System       Edge       Single Rise         ?       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise         ?       Dataln_pad_1_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_min:       1@ ns         ?       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_max:       1@ ns         ?       Dataln_pad_0_i(*)       III sysClk       System       Edge       Single Rise       trce_dly_max:       1@ ns         ?       LineState_pad_0_i(*)       III sysClk       System       Edge       Single Rise          ?       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise          ?       VStatus_pad_0_i(*)       III sysClk       System       Edge       Single Rise          ?       VStatus_pad_0_i       III sysClk       System       Edge       Single Rise          ?       Nx4ctive_pad_0_i       III sysClk       System       Edge       Single Rise          ?       Rx4ctive_pad_0_i       III sysClk       System       Edge       Single Rise <td></td> <td>? GTPRESET_IN</td> <td>🕅 mgtEngi</td> <td>System</td> <td></td> <td>Edge</td> <td></td> <td>Single Rise</td> <td></td> <td>tco_min:</td> <td>18</td> <td>ns</td>		? GTPRESET_IN	🕅 mgtEngi	System		Edge		Single Rise		tco_min:	18	ns
Image: Contract of the series of the seri	Image: Contract of the series of the seri	Image: Contract of the series of the seri	Image: Contract of the series of the seri	Image: System       Edge       Single Rise         Image: System	Image: Presser_IN       Indingends       System       Edge       Single Rise         Image: Presser_IN       III mgEngi       System       Edge       Single Rise       Iterc_dly_min:       Iterc_dly_max         Image: Presser_IN       III sysClk       System       Edge       Single Rise       Iterc_dly_max       Iterc_dly_max         Image: Presser_In       Image: Presser_In       Image: Presser_In       Iterc_dly_max       Iterc_dly_max       Iterc_dly_max         Image: Presser_In       Image: Presser_In       Image: Presser_In       Iterc_dly_max       Iterc_dly_max         Image: Presser_In       Image: Presser_In       Image: Presser_In       Iterc_dly_max       Iterc_dly_max         Image: Presser_In<	Image: Presser_IN       Indingengi System       Edge       Single Rise         Image: Presser_IN       Image: Presser_IN       Image: Presser_IN       Image: Presser_IN         Image: Presser_IN       Image: Presser_IN       Image: Presser_IN       Image: Presser_IN         Image: Presser_IN       Image: Presser_IN       Image: Presser_IN       Image: Presser_IN       Image: Presser_IN         Image: Presser_IN       Image: Presser_IN       Image: Presser_IN       Image: Presser_IN       Image: Presser_IN       Image: Presser_IN         Image: Presser_IN		? GTPRESET_IN	🕅 mgtEngi	System		Edge		Single Rise	-			
P       GTPRESET_IN       III mgtEngi System       Edge       Single Rise         P       Dataln_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       Dataln_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       LineState_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       LineState_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       VStatus_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise         P	P       GTPRESET_IN       III mgtEngi System       Edge       Single Rise         P       Dataln_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       Dataln_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       LineState_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       LineState_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       VStatus_pad_0_i[*]       III sysClk       System       Edge       Single Rise         P       RxActive_pad_0_i       III sysClk       System       Edge       Single Rise         P	P       GTPRESET_IN       III mgtEngi System       Edge       Single Rise         P       Dataln_pad_0_if*       III sysCik       System       Edge       Single Rise         P       LineState_pad_0_if*       III sysCik       System       Edge       Single Rise         P       V Status_pad_0_i       III sysCik       System       Edge       Single Rise          P       RxActive_pad_0_i       III sysCik       System       Edge       Single Rise          P       RxActive_pad_0_i       III sysCik       System       Edge       Si	P       GTPRESET_IN       III mgtEngi System       Edge       Single Rise         P       Dataln_pad_0_it*       III sysCik       System       Edge       Single Rise         P       LineState_pad_0_it*       III sysCik       System       Edge       Single Rise         P       LineState_pad_0_i*       III sysCik       System       Edge       Single Rise          P       NxActive_pad_0_i       III sysCik       System       Edge       Single Rise          P       RxActive_pad_1_i       III sysCik       System       Edge	Image: System       Edge       Single Rise         Image: System	P       GTPRESET_IN       III mgtEngi System       Edge       Single Rise         P       Dataln_pad_0_if*I       III sysClk System       Edge       Single Rise       trce_dly_min:       1@ ns         III estate_pad_0_if*I       III sysClk System       Edge       Single Rise       trce_dly_max       1@ ns         III estate_pad_0_if*I       III sysClk System       Edge       Single Rise       trce_dly_max       1@ ns         III estate_pad_0_i       III sysClk System       Edge       Single Rise       trce_dly_max       Rise Max = tco_max + trce_dly_max         III sysClk System       Edge       Single Rise       tisi	P GTPRESET_IN       III mgEngi System       Edge       Single Rise         P DataIn_pad_0_i(*)       III sysClk System       Edge       Single Rise         P LineState_pad_0_i(*)       III sysClk System       Edge       Single Rise         P V Status_pad_0_i(*)       III sysClk System       Edge       Single Rise         P RxActive_pad_0_i       III sysClk System       Edge       Single Rise         P RxActive_pad_0_i       III sysClk System       Edge       Single Rise         P RxActive_pad_0_i       III sysClk System		Interface	Clock ^1	Synchronous		Alignment		Data Rate and Edge		Clock period:	10	ne

Figure 14: Completed Inputs Page of the Timing Constraints Wizard

4. When you have successfully entered all the input constraint values, click Next.

The Output Delays page of the wizard displays all the outputs that are unconstrained in the design. The page layout is very similar to the inputs page.

- 5. In the Output Delays page, click the **Clock** header to sort the table alphabetically by clock name.
- 6. Use Table 3 below to constrain all the outputs as you did for the input constraint values. You can select multiple lines in the wizard at once and edit several entries at the same time.





Interface	Clock	Synchronous	Alignment	Data Rate and Edge	tsu (ns)	thd (ns)	trce_dly_max (ns)	trce_dly_min (ns)
OpMode_pad_0_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
OpMode_pad_1_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_pad_0_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_pad_0_o[*]	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
SuspendM_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
SuspendM_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TermSel_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TermSel_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TxValid_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
TxValid_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_Load_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
VControl_Load_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
XcvSelect_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
XcvSelect_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
phy_rst_pad_0_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
phy_rst_pad_1_o	sysClk	System	Setup/Hold	Single Rise	1.0	0.1	0.1	0.1
DataOut_pad_0_o[*]	VIRTUAL_wbClk_4	System	Setup/Hold	Single Rise	2.1	0.6	0.1	0.0
DataOut_pad_1_o[*]	VIRTUAL_wbClk_4	System	Setup/Hold	Single Rise	2.1	0.6	0.1	0.0
Or1200_pm_out[*]	VIRTUAL_wbClk_4	System	Setup/Hold	Single Rise	2.1	0.6	0.1	0.0

#### **Table 3: Output Constraint Values**

#### 7. Click **Next** to continue.

The wizard looks for any unconstrained combinational paths through the design. A combinational path is a path that traverses the FPGA without being captured by any sequential elements. This design does not contain any combinational paths.

8. Click **Next** to continue.

Physically exclusive clock groups are clocks that do not exist in the design at the same time. There are no unconstrained physically exclusive clock groups in this design.

9. Click **Next** to continue.

Logically exclusive clocks with no interaction are clocks that are active at the same time except on shared clock tree sections. Then these clocks do not have logical paths between each other and outside the shared sections, they are logically exclusive. There are no unconstrained logically exclusive clock groups with no interaction in the design.

#### 10. Click Next to continue.

Logically exclusive clocks with interaction are clocks that are active at the same time except on shared clock tree sections. When these clocks have logical paths between each other, only the clocks limited to the shared clock tree sections are logically exclusive and are therefore constrained differently than the logically exclusive clock with no interaction. There are no unconstrained logically exclusive clock groups with interaction in the design.

11. Click **Next** to continue.







The Asynchronous Clock Domain Crossings page recommends constraints for safe clock domain crossings. This design does not contain any unconstrained clock domain crossings.

12. Click **Next** to continue.

The following figure shows the final page of the Timing Constraints wizard. All the constraints that were generated by the wizard can be viewed by clicking the links. If you would like to run any reports once the wizard is finished, you can select them using the check boxes in the wizard.

À Timing Constraints	Nizard X
HLX Editions	Ocnstraints Summary         Image: The Timing Constraints Wizard created 83 new timing constraints:         Create Clock (7)         Set Input Delay (38)         Set Output Delay (38)
<b>E</b> XILINX.	<ul> <li>View Timing Constraints</li> <li>Create Timing Summary report</li> <li>Create Check Timing report</li> <li>Create Methodology report</li> </ul> To keep the new constraints and perform the selected actions, click Finish. The new constraints will automatically be saved to your target XDC file. To discard the constraints, click Cancel.
•	< <u>B</u> ack <u>N</u> ext > <u>Finish</u> Cancel

Figure 15: Timing Constraints Wizard Summary Page

13. Click **Finish** to complete the Timing Constraints wizard.





### **Step 4: Using the Constraints Editor**

1. Click **Edit Timing Constraints** from the Flow Navigator under the Synthesized Design section. The Vivado IDE displays the Timing Constraints window.

Project Summary	y x Device x Timing Constraints	×	1	203
<b>王   ≑   ≯</b>	+	🔸 🕂 📄 🖉 Create Clock		
V Clocks (7)	1	Clock Name	Period (ns)	Rise At (
Create Clo	ock (7)	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT	12.800	0.
Create Ge	nerated Clock (0)	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT	12.800	0.
Rename A	uto-Derived Clock (0)	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT	12.800	0.
Set Clock I	Latency (0)	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT	12.800	0.
Set Clock	Uncertainty (0)	sysClk	10.000	0.
Set Clock	Groups (0)	VIRTUAL_cpuClk_5	20.000	0.
Set Clock	Sense (0)	VIRTUAL_wbClk_4	20.000	0.
Set Input J		ick to create a Create Clock constraint		
Set Systen				
	al Delay (0)			
V Inputs (38)	A	I K		
Set Input D V Outputs (38)	Jelay (38)			
	Delay (38)			
<ul> <li>Assertions (0)</li> </ul>	Delay (30)			>
All Constraints				
		$\sim$		
Q.   ¥.   ♦			,	
Position	Command			
✓ Constraints				^
V ID timing.x	dc (C://ivado_Tutorial/project_cpu_netIst/proje	ct_cpu_netlst.srcs/lab1/new/timing.xdc)		
1	create_clock -period 12.800 -name mgtEngin	e/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT -waveform {0.0	00 6.400} [get_	_pins m
2	create_clock -period 12.800 -name mgtEngin	e/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT -waveform {0.0	00 6.400} [get_	_pins m
3	create_clock -period 12.800 -name mgtEngin	e/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT -waveform {0.0	00 6.400} [get_	_pins m
4	create_clock -period 12.800 -name mgtEngin	e/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT -waveform {0.0	00 6.400} [get_	pins m
5	create_clock -period 10.000 -name sysClk -w	aveform {0.000 5.000} [get_ports sysClk]		
6	create_clock -period 20.000 -name VIRTUAL_	_cpuClk_5 -waveform {0.000 10.000}		
7	set_input_delay -clock [get_clocks sysClk] -m	in -add_delay 2.0 [get_ports {DataIn_pad_0_i[*]}]		~
<		Apply Cancel		>

Figure 16: Timing Constraints Window

There are three sections to the Timing Constraints window, as shown in the following figure:

- Constraints tree view is labeled as section "A." This section displays standard timing constraints, grouped by category. Double-clicking a constraint in this section opens a form to help you define the selected constraint.
- Constraints Spreadsheet is labeled as section "B." This section displays timing constraints of the type currently selected in the Constraints tree view. If you prefer, you can use this to directly define or edit constraints instead of using the Constraints wizard.
- **All Constraints** is labeled as section "C." This section displays all the timing constraints that currently exist in the design.





The Timing Constraints wizard identifies missing clocks, I/O delays, and clock domain crossings exceptions, but it does not handle general timing exceptions. You are going to use the timing constraints editor to create the exceptions that exist in this design.

First, you are going to set a false path on the GTPRESET\_IN input. This is the input constraint that you skipped by unchecking it on the input delay page of the Timing Constraints wizard. The GTPRESET\_IN signal is an asynchronous reset that is properly synchronized inside the design. For more information about false paths, see <u>this link</u> in the *Vivado Design Suite User Guide: Using Constraints* (UG903).

- 2. In the Constraints tree view, scroll down to the Exceptions category, shown in the following figure.
- 3. Double-click Set False Path.

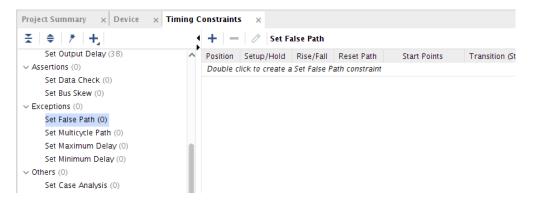


Figure 17: Set False Path Section in the Constraints Editor

4. To the right of the **From** text box, click the **Choose Start Points** button.

The Specify Start Points dialog box appears.

- 5. From the Find names of type drop-down list, select I/O Ports as shown in Figure 18, page 28.
- 6. Under Options, select "Name," "contains," and in the search pattern text box, enter GTPRESET\_IN.
- 7. Click the **Find** button.





8. Select **GTPRESET\_IN** in the found results text box and press the right arrow to move it to the selected names text box.



**TIP:** You can also double-click GTPRESET\_IN to move it from the **Find results** list to the **Selected names** list.

Notice that the Command field displayed at the bottom of the dialog box changes as you perform these different actions. The get\_ports command changes to:

get ports	"*GTPRESET_	IN*"

À Specify Start Points		×
Specify a list of path endpoints or clocks.		4
Fin <u>d</u> names of type: I/O Port 🗸 🗸		
Options		
NAME ~ contains	✓ GTPRESET_IN	⊗ +
Regular expression         Ignore case		
Of Objects:		
<u> </u>	<u>F</u> ind	
	Tura	
Results		
Found: 0	Selected: 1	₽₽
		Ť
Use the buttons on the right to move items to this list.	<b>*</b>	+
	<b>⇒</b>	<b>↓</b> ★
Command: get_ports "*GTPRESET_IN*"	-	⊗ □ Enumer <u>a</u> te
(?)		
	Set Apper	nd Cancel

Figure 18: Choose Start Points Window for set\_false\_path Dialog Box

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9. Click Set in the Specify Start Points dialog box.

The completed Set False Path dialog box is shown in the following figure. Notice the following command text in the **Command** field at the bottom of the dialog box:

set\_false\_path -from [get\_ports "\*GTPRESET\_IN\*"]

The Vivado IDE displays the Tcl command form of all constraints created via the dialogs for your review. This is useful for learning the Tcl command syntax, and for verifying the final constraint before adding it.

argets	Options					
tart Poin	s					
<u>F</u> rom:	[get_ports "*G	TPRESET_IN*"]	8	··· Transi	ition ris	e/fall 🗸 🗸
hrough P	oints					
Throu	gh:		••••	Transition	rise/fall	~ +
	1					
nd Points						

Figure 19: Completed set\_false\_path Constraint Window

10. Click **OK** to close the Timing Constraint Editor.

Vivado creates the false path exception.





### Add a MultiCycle Path

Next, you will add a multicycle path using the constraints editor.

- 1. Double-click on Set Multicycle Path under the Exceptions category of the tree.
- 2. In the Set Multicycle Path dialog box, set the path multiplier to **2**.
- 3. In the **Through** entry box, type the following string (alternately, you can copy and paste it from here):

```
[get_pins cpuEngine/or1200_cpu/or1200_alu/*]
```

Notice that the Tcl command displays in the **Command** field.

4. Click OK.

A new multicycle path is added to the constraints editor in the **<unsaved\_constraints>** section, as shown in the following figure.

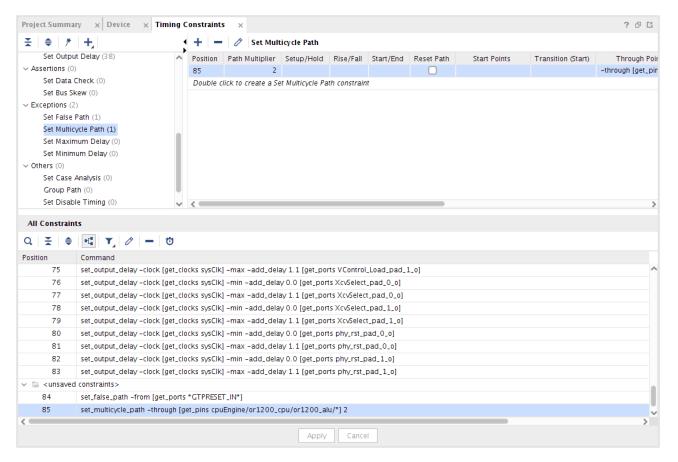


Figure 20: New Multicycle Path Added to the Constraints Editor

Adding a multicycle path by default pushes the setup timing to the specified number of cycles (N), *but it also pushes the hold timing to* N - 1 *cycles*. This is usually not what is intended and could cause Vivado tools to spend a lot of time fixing large hold violations. In this case we want the setup path





to be timed to two cycles of the clock, but we want the hold path to be timed to zero cycles of the clock. To achieve this, we need to define another multicycle path on the hold edge to 1, such that N - 1 is zero. For more information about this situation, see <u>this link</u> in the *Vivado Design Suite User Guide: Using Constraints* (<u>UG903</u>).

5. Double-click **Set Multicycle Path** under the Exceptions category of the tree for a second time.

Note that all the fields you entered previously are still filled in.

- 6. In the Set Multicycle Path dialog box, change the **Path Multiplier** to **1**.
- 7. Select the **Options** tab.
- 8. Under Setup/Hold, select the check box that says Use path multiplier.
- 9. Use the pull-down to select hold (minimum delay).

Specily pai	th <u>m</u> ultiplier:	1 🗘	
T <u>a</u> rgets	Options		
Setup/Hole	d		
✓ <u>U</u> se	e path multip	lier for hold (minimum delay) 🗸 calculation	
Rise/Fall			
U <u>s</u> e	e path multip	lier for endpoint rising 🗸 delays	
Start/End			
	ticycle inform	nation is relative to the startpoint 🗸 clock	
		atthe exceptions before setting multicycle path	
	e existing pa	an exceptions before setting multicycle path	

Figure 21: Set Multicycle Path – Options Tab

#### 10. Click **OK**.

We now have a fully constrained design in memory. To save the constraints to disk, proceed to Step 5: Saving Constraints.







### **Step 5: Saving Constraints**

Constraint management is an important step of the design flow, and the Vivado Design Suite provides you the flexibility of adding new constraints into an existing constraint file, overwriting existing constraints, or creating a new constraints file to track design changes or complete missing constraints.

You have created a few timing exceptions for the design, but the exceptions exist only in memory and not on disk yet. You need to save the exceptions to the timing.xdc file.

- 1. From the Sources window in Vivado, double-click timing.xdc under **Constraints > lab1**.
- Scroll to the bottom of the file and notice that the set\_false\_path and set\_multicycle\_path constraints do not exist in the file. This is also reflected in the Timing Constraints Editor as <unsaved\_constraints>, as shown in the following figure.

All Constrain	ls	
Q 🛛 🛣 🔤	► III × / //   -	
Position	Command	Scoped Cell
79	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports XcvSelect_pad_1_o]	
80	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.0 [get_ports phy_rst_pad_0_o]	
81	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports phy_rst_pad_0_o]	
82	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.0 [get_ports phy_rst_pad_1_o]	
83	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.1 [get_ports phy_rst_pad_1_o]	
∼ 📄 <unsave< td=""><td>d constraints&gt;</td><td></td></unsave<>	d constraints>	
84	set_false_path -from [get_ports *GTPRESET_IN*]	
85	set_multicycle_path -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 2	
86	set_multicycle_path -hold -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 1	
	Apply Cancel	

#### Figure 22: Unsaved Constraints Displayed in the Constraints Editor.

3. Click the **Save Constraints** button or use the **File > Constraints > Save As** command from the main menu.





4. Click the **Reload** link in the banner of the **timing.xdc** tab to reload the constraints file from disk. Notice that the false path and multi-cycle paths are now visible in the timing.xdc text file, as shown in the following figure.

Proje	ect Summary × Device × timing.xdc ×	? 🗆 🖸
C://i	ivado_Tutorial/project_cpu_netlst/project_cpu_netlst.srcs/lab1/new/timing.xdc	×
Q,		٥
54	<pre>set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports {VControl_pad_0_o[*]}]</pre>	-
55 ;	<pre>set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports {VControl_pad_0_o[*]}]</pre>	
56	<pre>set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports {VControl_pad_1_o[*]}]</pre>	
57	<pre>set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports {VControl_pad_1_o[*]}]</pre>	
58	set_output_delay -clock [get_clocks VIRTUAL_wbClk_4] -min -add_delay -0.600 [get_ports {or1200_pm_out[*]	}1
59	set_output_delay -clock [get_clocks VIRTUAL_wbClk_4] -max -add_delay 2.200 [get_ports {orl200_pm_out[*]}	1
60 ¦	set_output_delay_clock [get_clocks_sysClk] -min_add_delay_0.000 [get_ports_SuspendM_pad_0_o]	
61	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports SuspendM_pad_0_o]	
62 ¦	<pre>set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports SuspendM_pad_1_0]</pre>	
63	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports SuspendM_pad_1_0]	
64	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports TermSel_pad_0_0]	
6 <b>5</b>	<pre>set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports TermSel_pad_0_0]</pre>	
66	<pre>set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports TermSel_pad_1_0]</pre>	
57	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports TermSel_pad_1_0]	
58	set_output_delayclock [get_clocks_sysClk] -minadd_delay_0.000 [get_ports_TxValid_pad_0_o]	
69 ¦	set_output_delay -clock [get_clocks_sysClk] -max -add_delay 1.100 [get_ports_TxValid_pad_0_o]	
70 }	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports TxValid_pad_1_0]	
71	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports TxValid_pad_1_o]	
72	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports VControl_Load_pad_0_o]	
13	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports VControl_Load_pad_0_o]	
74 ¦	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports VControl_Load_pad_1_0]	
75	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports VControl_Load_pad_1_0]	- 1
76 ¦	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports XcvSelect_pad_0_0]	
77	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports XcvSelect_pad_0_0]	
78 ;	set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports XcvSelect_pad_1_0]	
79	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports XcvSelect_pad_1_0]	
80	<pre>set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports phy_rst_pad_0_0]</pre>	
81	<pre>set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports phy_rst_pad_0_0]</pre>	
82	<pre>set_output_delay -clock [get_clocks sysClk] -min -add_delay 0.000 [get_ports phy_rst_pad_1_0]</pre>	
83	set_output_delay -clock [get_clocks sysClk] -max -add_delay 1.100 [get_ports phy_rst_pad_1_0]	
84	<pre>set_false_path -from [get_ports *GTPRESET_IN*]</pre>	
85 ;	<pre>set_multicycle_path -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 2</pre>	
86	<pre>set_multicycle_path -hold -through [get_pins cpuEngine/or1200_cpu/or1200_alu/*] 1</pre>	
87		
1		1

Figure 23: timing.xdc Tab

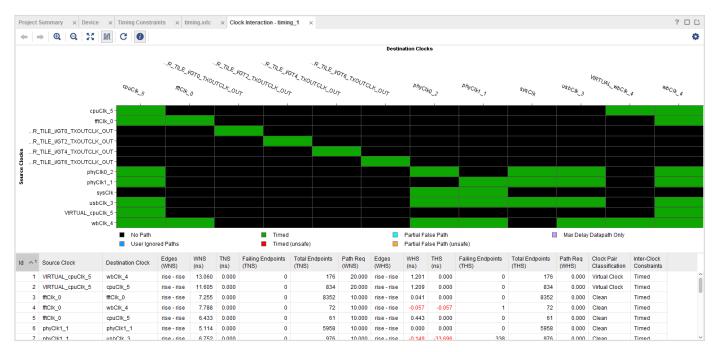




### **Step 6: Clock Interaction Report**

After or during constraints creation, you must verify that the constraints are complete and safe. Vivado Design Suite times all clocks together by default unless you specify otherwise by defining clock groups or other timing exceptions. The set\_clock\_groups command specifies asynchronous or exclusive clock domains and disables timing analysis between them. You can also use the set\_false\_path exception between two clocks to disable timing on all paths between them, or use it on specific netlist objects to only disable some paths. The set\_multicycle\_path exception modifies the clock edges used during timing analysis instead of the default single cycle assumption. For more information on using these constraints, see the *Vivado Design Suite User Guide: Using Constraints* (UG903).

Vivado automatically infers timing path requirements for paths that cross between two different clock domains, called inter-clock paths, making assumptions regarding phase and offset. The Report Clock Interaction command reports inter-clock paths, to help identify potential problems such as unrealistic setup or hold requirements between two clocks, or unsafe timing between asynchronous clocks (no known phase relationship) which can lead to unstable hardware behavior. For more information on the Clock Interaction Report, see the *Details of the Clock Interaction Report* (UG906).



 From the Flow Navigator, select Synthesized Design > Report Clock Interaction and click OK in the Report Clock Interaction dialog box to accept the default settings.

Figure 24: Clock Interaction Report

The Vivado IDE generates a graphical matrix illustrating the relationship of the various clocks in the design, as shown in the previous figure. For this design, the primary clock (sysClk) connects to an MMCM, which generates six additional clocks. The clock interactions shown are between these





generated clocks. In addition, the Timing Constraints wizard created additional generated clocks and virtual clocks to fully constrain the design.

In general, the Clock Interaction report shows clock pairs with no path between them (black), with paths safely timed (green and light blue), with paths not safely timed (red and orange) and with paths covered by Max Delay Datapath Only constraints. In this design, only black cells and green cells are displayed in the matrix.

$\wedge$
$\langle \rangle$

*Important!* Green in the matrix does not mean that timing is met, it simply means that the timing constraints and the clock tree topologies allows safe timing analysis and accurate slack computation.

In the Clock Interaction report, unsafe means there is no common primary clock (no known phase relationship), or no common node (uncommon scenario that results in unknown phase relationship), or no common clock period within the first 1000 clock cycles of the source and destination clocks. The Vivado timing engine selects edges on the launch and capture clocks based on the first 1000 cycles, but these edges might not reflect the most pessimistic analysis between the clocks.



**TIP:** The colors described here are the default colors. Your colors might be configured differently from those shown in Figure 24.

2. Close the Clock Interaction window by clicking the **Close** button  $\times$  in the window tab.

### **Step 7: Timing Summary Report**

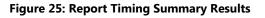
Timing paths start and end at clocked elements. Input and Output ports are not sequential elements, and by default Vivado timing analysis does not time paths to or from I/O ports in the design, unless input/output delay constraints are specified.

In this step you will generate and interpret timing reports in Vivado.

- 1. Select **Reports > Timing > Report Timing Summary**.
- 2. Click **OK** to generate the report, using the default options.

The timing summary tab opens, as shown in the following figure.

Tcl Console Messages Log	Reports	Design Runs Timing ×						? _ 🗆 🖸
Q   X   ≑   C   🕍   🥹	1	Design Timing Summary						
General Information Timer Settings	î	Setup		Hold		Pulse Width		
\rm Design Timing Summary		Worst Negative Slack (WNS):	2.250 ns	Worst Hold Slack (WHS):	-0.274 ns	Worst Pulse Width Slack (WPWS):	3.000 ns	
Clock Summary (14)		Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	-372.506 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns	
> 🚡 Check Timing (9)		Number of Failing Endpoints:	D	Number of Failing Endpoints:	6476	Number of Failing Endpoints:	0	
> 🕞 Intra-Clock Paths		Total Number of Endpoints:	46377	Total Number of Endpoints:	46377	Total Number of Endpoints:	16037	
> 🚡 Inter-Clock Paths > 🚍 Other Path Groups > 🚍 User Ignored Paths		Timing constraints are not met.						
Timing Summary - timing_1								



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This design passes setup timing but fails hold analysis. Before implementing the design, timing analysis uses estimated net delays that represent ideal placement. Small hold violations are common at this point of the flow and will be fixed during the routing step. For now, review the content of the report.

3. Click on the **Worst Negative Slack** link in the design timing summary section to see the worst timing path in the design, as shown in the following figure.

Q 😤 🚖 C 🔛 0												
> = phyClk0_2 to wbClk_4	^	Name	Slack ^1	Levels	Routes	High Fanout	From	То	Total Delay	Logic Delay	Net Delay	Requirement
> 🗁 phyClk1_1 to cpuClk_5		👍 Path 473	2.250	17	18	165	usbEngine1/u4/inta_reg/C	cpuEngine/or1u_err_o_reg/D	7.406	1.583	5.823	10.0
> 🚍 phyClk1_1 to sysClk		👍 Path 474	2.250	17	18	165	usbEngine1/u4/inta_reg/C	cpuEngine/or1g_o_reg[0]/D	7.406	1.583	5.823	10.0
> 📬 phyClk1_1 to usbClk_3	-	🔥 Path 475	2.250	17	18	165	usbEngine1/u4/inta_reg/C	cpuEngine/or1g_o_reg[1]/D	7.406	1.583	5.823	10.0
> 🗁 phyClk1_1 to wbClk_4	- 1	👍 Path 476	2.250	17	18	165	usbEngine1/u4/inta_reg/C	cpuEngine/or1g_o_reg[3]/D	7.406	1.583	5.823	10.0
> 🗁 sysClk to phyClk0_2		🔥 Path 477	2.257	17	18	165	usbEngine1/u4/inta_reg/C	cpuEngine/or1g_o_reg[2]/D	7.399	1.583	5.816	10.0
> 🗁 sysClk to phyClk1_1		👍 Path 478	2.257	17	18	165	usbEngine1/u4/inta_reg/C	cpuEngine/or1cstb_o_reg/D	7.399	1.583	5.816	10.0
∨ asbClk_3 to cpuClk_5		👍 Path 479	2.581	16	17	165	usbEngine1/u4/inta_reg/C	cpuEngine/or1r_o_reg[13]/D	7.075	1.540	5.535	10.0
Setup 2.250 ns (10)	~	<						1	-			>

Figure 26: Worst Timing Path in the Design

4. When the worst path is selected, press the **F4** key to bring up its schematic. The following figure shows the worst setup path in the design.

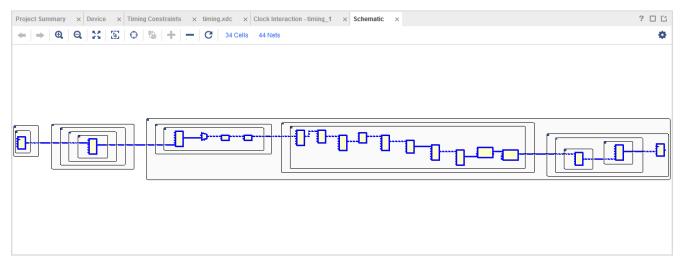


Figure 27: Schematic of Worst Setup Path in the Design





- 5. In the timing summary tree, select **Check Timing**.
  - There are nine issues flagged by Check Timing shown in the following figure.
  - Eight of these are pulse\_width\_clock checks, which were also flagged by the Timing Constraints wizard, but were not constrained. These violations have low severity because the corresponding missing clocks are not needed for timing logic paths.
  - The remaining issue flagged by Check Timing is a no\_input\_delay check, which is due to a missing input constraint on the reset signal that was set to false\_path. This can also be ignored in this example.

Q ≭ ♦ C ₩ 0	Q Check Timing		
🗠 🕞 Check Timing (9)	Timing Check	Count v1	Worst Severity
no_clock (0)	pulse_width_clock	8	Low
constant_clock (0)	no_input_delay	1	🕛 Medium
pulse_width_clock (8)	no_clock	0	
unconstrained_internal_endpoints (0)	constant_clock	0	
• no_input_delay (1) no_output_delay (0)	unconstrained_internal_endpoints	0	
	no_output_delay	0	
multiple_clock (0)	multiple_clock	0	
generated_clocks (0) loops (0) partial_input_delay (0) partial_output_delay (0)	generated_clocks	0	
	loops	0	
	partial_input_delay	0	
	partial_output_delay	0	
latch_loops (0)	latch loops	0	
🕞 📷 Intra-Clock Paths		Ű	
Inter-Clock Paths			

Figure 28: Check Timing Results in the Timing Summary Window





6. In the timing summary tree, select the **Clock Summary**, as shown in the following figure. The clock summary section of the timing summary report lists all the clocks in the design and shows the resulting frequencies and waveforms of each clock. The hierarchy shows the relationship between the generated clocks and the primary clock (for example, cpuClk\_5 vs. sysClk). For example, it shows that cpuClk\_5 is generated from primary clock SysClk, and its period is twice that of sysClk.

Q 🕺 🌩 🕑 💾 🕛	Q ₹ ♦ Clock Summary				
General Information	Name	Waveform	Period (ns)	Frequency (MHz)	
Timer Settings	VIRTUAL_cpuClk_5	{0.000 10.000}	20.000	50.000	
Design Timing Summary	VIRTUAL_wbClk_4	{0.000 10.000}	20.000	50.000	
Clock Summary (14)	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt0_ROCKETIO_WRAPPER_TILE_i/GT0_TXOUTCLK_OUT	{0.000 6.400}	12.800	78.125	
Check Timing (9)	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt2_ROCKETIO_WRAPPER_TILE_i/GT2_TXOUTCLK_OUT	{0.000 6.400}	12.800	78.125	
Intra-Clock Paths	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt4_ROCKETIO_WRAPPER_TILE_i/GT4_TXOUTCLK_OUT	{0.000 6.400}	12.800	78.125	
Inter-Clock Paths	mgtEngine/ROCKETIO_WRAPPER_TILE_i/gt6_ROCKETIO_WRAPPER_TILE_i/GT6_TXOUTCLK_OUT	{0.000 6.400}	12.800	78.125	
cpuClk_5 to VIRTUAL_wbClk_4	✓ sysClk	{0.000 5.000}	10.000	100.000	
wbClk_4 to VIRTUAL_wbClk_4	clkfbout	{0.000 5.000}	10.000	100.000	
phyClk0_2 to sysClk	cpuClk_5	{0.000 10.000}	20.000	50.000	
phyClk1_1 to sysClk	fftClk_0	{0.000 5.000}	10.000	100.000	
s usbClk_3 to sysClk	phyClk0_2	{0.000 5.000}	10.000	100.000	
VIRTUAL_cpuClk_5 to cpuClk_5	phyClk1_1	{0.000 5.000}	10.000	100.000	
fftClk_0 to cpuClk_5  phyClk0_2 to cpuClk_5	usbClk_3	{0.000 5.000}	10.000	100.000	



The remaining sections of the timing summary report group paths by their type. Each section lists the top ten paths (specified when the report was generated) in that group. These include inter-clock paths, intra-clock paths, other path groups, user ignored paths, and unconstrained paths. Clicking the roots will show a summary of the paths beneath. Expanding the tree further will ultimately display the top timing paths for each group.

### Conclusion

At this point you can either continue to **Lab #2**: Setting Physical Constraints, or exit the Vivado Design Suite and continue later. Lab #2 uses the project created during this lab, so be sure not to delete your work.

In this lab, you learned:

- How to Create a constraint set and set a target constraint file
- How to add timing constraints to a design using the Timing Constraints Wizard
- How to add timing exceptions using the Timing Constraints Editor
- The importance of saving constraints to disk versus in-memory constraints
- How to generate the clock interaction report and properly interpret the resulting matrix
- How to generate the timing summary report and properly interpret the results





# Lab 2: Setting Physical Constraints

### Introduction

In this lab, you will create physical constraints for the CPU Netlist design, observing how actions in the GUI translate into Tcl commands. Using Tcl commands, complex operations are easily scripted for repeated use, at various stages of the flow.

**Note:** If you are continuing from Lab1, and your design is open, skip ahead to <u>Step 2: Adding Placement</u> <u>Constraints</u>.

### **Step 1: Opening the Project**

This lab continues from the end of Lab #1 in this tutorial. You must complete Lab #1 prior to beginning Lab #2. If you closed the tool, or closed the tutorial project at the end of Lab #1, you will need to open them again.

- 1. Start by loading the Vivado<sup>®</sup> Integrated Design Environment (IDE) by doing one of the following.
  - o Launch Vivado IDE from the icon on the Windows desktop.
  - Select Windows > Programs > Xilinx Design Tools > Vivado 2019.x > Vivado 2019.x.
  - Type **vivado** from a command terminal.

From the Getting Started screen you can open recent projects.

2. Under Recent Projects, click project\_cpu\_netlist as shown in the following figure.









# **Step 2: Adding Placement Constraints**

Explore some of the design hierarchy, and begin placing logic elements to create physical constraints.

1. From the Flow Navigator, select **Open Synthesized Design**. The synthesized design might already be open if you came directly to this step.

The synthesized netlist opens with the Device window displayed.

- 2. Select the **Netlist** window and expand the **clkgen** hierarchy.
- 3. Expand the Leaf Cells folder and select the instance mmcm\_adv\_inst (MMCME2\_ADV).

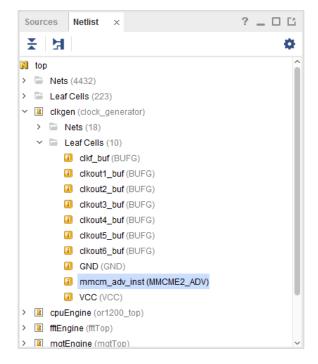


Figure 31: Netlist Window

4. Look in the Cell Properties view, under the Properties tab, and notice that the STATUS is UNPLACED, and there are no IS\_LOC\_FIXED or IS\_BEL\_FIXED properties shown.

5. Check this in the Tcl Console by typing: get\_property IS\_LOC\_FIXED [get\_cells clkgen/mmcm\_adv\_inst] This returns a zero, indicating the object is not fixed to a location.





6. Zoom into the bottom right of the Device view, to display the lower half of **Clock Region X1Y0**, to prepare for placing the selected object. See the following figure.

*Tip:* It is easier to place logic in the Device window if Routing Resources are not displayed. If they are displayed, select the **Routing Resources** toolbar button *to disable*.

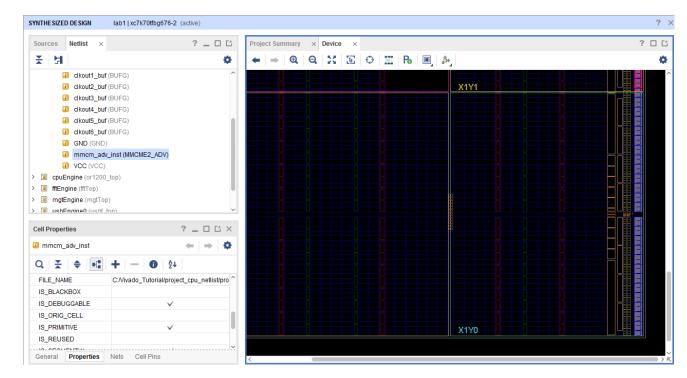


Figure 32: Placing the MMCM

- 7. In the Netlist window, click on the **mmcm\_adv\_inst** and drag it into the Device window to place it into the bottom right MMCME2\_ADV.
- 8. Look in the Tcl Console. You should see something like these three commands:

```
startgroup
place_cell clkgen/mmcm_adv_inst MMCME2_ADV_X1Y0/MMCME2_ADV
endgroup
```

The startgroup and endgroup Tcl commands bracket sequences of commands to support the undo function in the Vivado tools. If you make a mistake, you can use the undo command in the Tcl Console, or the **Edit > Undo** command. This will undo the placement and allow you to redo it. For more information on startgroup, endgroup, and undo, refer to the *Vivado Design Suite Tcl Command Reference Guide* (UG835).





9. Look at the Properties tab of the Cell Properties window for the MMCM cell you placed.

Notice that the IS\_BEL\_FIXED and IS\_LOC\_FIXED properties are now checked, reflecting that the object has been placed, as shown in the following figure. The STATUS property is set to FIXED as well.



**Tip:** The Cell Drag and Drop mode in the Device window determines whether only IS\_LOC\_FIXED is set, or IS\_BEL\_FIXED is also set, when placing objects. Refer to this <u>link</u> in the Vivado Design Suite User Guide: Using the Integrated Design Environment (UG893) for more information on using the Device window.

Cell Properties	? _ D 🗄 ×
mmcm_adv_inst	$\leftarrow   \Rightarrow   \diamondsuit$
Q   X   ♦   ■   +	— 0 \$t
DIVCLK_DIVIDE	1 🖉 ^
FILE_NAME	C:/Vivado_Tutorial/project_cpu_net
IS_BEL_FIXED	$\checkmark$
IS_BLACKBOX	
IS_DEBUGGABLE	$\checkmark$
IS_LOC_FIXED	
IS_ORIG_CELL	
General <b>Properties</b> Nets	Cell Pins

Figure 33: BEL and LOC Placement Constraints

The IS\_BEL\_FIXED and IS\_LOC\_FIXED properties on the object are physical constraints reflecting the placement of the object. These constraint are used by Vivado implementation, and will not be changed by the tool. However, if the properties are invalid, they will cause errors downstream in the design flow.

Notice that when you place mmcm\_adv\_inst in the Device window, the **Save Constraints** button is enabled. The physical constraints are added to the Vivado tool in-memory design, but are not yet saved to the target constraint file.





# **Step 3: Defining Additional Physical Constraints**

In this step you will define additional physical constraints to the design, such as the PACKAGE\_PIN, and PROHIBIT constraints.

1. Select **Layout** > **I/O Planning** to open the I/O Planning view layout from the Layout Selector in the tool bar menu.

The I/O Planning view layout displays the Package window, as well as the I/O Ports and Package Pins windows, to facilitate planning the I/O port assignment for the design.

For the purposes of this tutorial, assume the PCB layout has been completed, and therefore certain pins are not accessible on the FPGA package. You can prohibit the Vivado tool from using these pins during placement and routing (assuming you have not already specified all of your I/O assignments).

2. Select the **AA8** pin in the Package window.



**Tip:** Use the X and Y-axis values on the edge of the Package window to help you locate this pin on the package.

3. With the pin selected, right-click and select Set Prohibit.

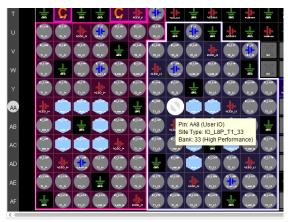


Figure 34: Package Pin A8

When you unselect the pin, you will notice the site now has a red circle with a diagonal line through it, indicating that it is unusable.

4. Look in the Tcl Console and review the TCL command produced by the Vivado IDE:

```
startgroup
set_property prohibit 1 [get_bels IOB_X1Y34/PAD]
set_property prohibit 1 [get_sites AA8]
endgroup
```





# **Step 4: Defining Constraints with Object Properties**

You can create timing and placement constraints as you have seen in this tutorial. You can also change the properties of cells to control how they are handled by Vivado implementation. Many physical constraints are defined as properties on a cell object.

For example, if you discover a timing issue with a RAM in the design, to avoid resynthesis, you can change a property of the RAM cell to add in pipeline registers. After confirming with the designer and validation teams that this is an acceptable approach, you can change the design.

### Setting Cell Properties

Because it can be too time consuming and costly to go back to the RTL after synthesis, you can make changes in the netlist as follows.

- 1. Select Edit > Find to open the Find dialog box, seen in the following figure.
  - a. Specify Find Cells.
  - b. Under Properties, set **PRIMITIVE\_TYPE** to **BMEM.BRAM**.
  - c. Make sure that Search Hierarchically is selected, as shown in the following figure.
  - d. Click OK.

Find		×
Find objects ir	the current design or device by filtering Tcl properties and objects.	4
R <u>e</u> sult nam <u>F</u> ind: Properties PRIMITI	e: find_1 Cells v /E_TYPE v is v BMEM.BRAM v +	
	expression Ignore case 🗹 Search hierarchically	
Of o <u>bj</u> ects:	show_objects -name find_1 [get_cells -hierarchical -filter { PRIMITIVE_TYPE =~ BMEM.bram.* } ]	
✓ <u>Open in</u>		
?		ancel

Figure 35: Find Dialog Box

The Find Results window opens.





- 2. Select the **Show Search** button  $\bigcirc$  on the toolbar menu of the Find Results window.
- 3. Search for **ingressLoop**, and select the following cell:

fftEngine/fftInst/ingressLoop[7].ingressFifo/

In the Properties tab of the Cell Properties window, you can see the DOA\_REG and DOB\_REG are set to zero, indicating that the output registers are disabled.

4. Generate a custom timing report from this cell directly from the Tcl Console. The Tcl command to enter is:

```
report_timing -from [get_cells fftEngine/fftInst/ingressLoop[7].ingressFifo/
buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg]
```

*Tip:* You can copy and paste the cell name from the General tab of the Cell Properties window into the Tcl console.

- 5. In the upper-right corner of the **Tcl console**, click the **Maximize** button  $\blacksquare$  to maximize the window and better view the timing report.
- 6. In the data path section of the report, 1.800ns is added by this RAMB.

RAMB36E1 (Prop_ramb36e1_CLk	BWRCLK DO	 BD0[16])	
ICAMDDOLT (ITOP_TambDOLT_CEN	_		An Franker (An Trank (Second and 177) is an an Fide (builden dide (inder dide black and an de bourse
	1.800	-0.526 r	fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/infer_fifo.block_ram_performance.
net (fo=2, unplaced)	0.466	-0.061	fftInst/toBft[15]_55[0]
DSP48E1		r	transformLoop[7].ct/xOutReg_reg/A[0]

- 7. Restore the Tcl Console to its normal size.
- 8. In the **Properties** tab of the Cell Properties window, select the **DOA\_REG** and **DOB\_REG** properties for this cell, and change their values from "0" to "1".

You can see the two set\_property commands run in the Tcl Console.

```
set_property DOA_REG {1} [get_cells {fftEngine/fftInst/ingressLoop[7].ingressFifo/
buffer_fifo/infer_fifo.block_ram_performance.fifo_ram_reg}]
```

set\_property DOB\_REG {1} [get\_cells {fftEngine/fftInst/ingressLoop[7].ingressFifo
/buffer\_fifo/infer\_fifo.block\_ram\_performance.fifo\_ram\_reg}]

9. Rerun the timing report from the selected cell. The Tcl command to enter is:

report\_timing -from [get\_cells fftEngine/fftInst/ingressLoop[7].ingressFifo
/buffer\_fifo/infer\_fifo.block\_ram\_performance.fifo\_ram\_reg]

10. Notice that the **data path delay** for the RAM is now 0.622 ns.

#### Setting Design Properties

Next, set the configuration mode on the design. This is another property that results in a physical constraint, in this case a property of the design rather than of a cell. To begin, list all of the properties of the current design.





1. List the properties of the design in the Tcl Console:

list\_property [current\_design]

This command returns the list of all defined properties on the current design. To make the list more readable, you can use the standard Tcl join command to combine the properties output with "\n" newline character, resulting in each property displaying on a separate line.

join [list\_property [current\_design]] \n

2. The specific property of interest is CONFIG\_MODE. To see what values this particular property can accept, use the list\_property\_value Tcl command:

join [list\_property\_value CONFIG\_MODE [current\_design]] \n

3. Use the **Tools > Edit Device Properties** command to set the CONFIG\_MODE property for the current design.

The Edit Device Properties dialog box opens.

- 4. Click **Configuration Modes** to open the Configuration Modes panel.
- 5. Scroll down on the page to find the **Master Serial** configuration mode option, as shown in the following figure.

dit Device Properties se this dialog to edit the pro	gramming and configuration properties for your current design; default values are set automatically.	×
Q <sub>*</sub>	Configuration Modes	
General Configuration Configuration Modes Startup Encryption Readback	Select up to two device configuration modes. JTAG is always selected. Selecting a check box assigns a mode and clicking an image displays details.  Prohibit usage of the configuration pins as user I/O and persist after configuration C  Reset configuration mode C  M[2:0]  M[2:0]  M[2:0]  DOUT  M[2:0]  DOUT  DIN  INIT_B  PUDC_B  PROGRAM_B  DONE  CCLK	Ŷ
	Master Serial	
Help		Cancel

Figure 36: Edit Device Properties – CONFIG\_MODE





6. Select the Master Serial configuration mode as shown, and click **OK** to close the dialog box.

The Tcl console shows the set\_property command that sets the CONFIG\_MODE:

set\_property CONFIG\_MODE M\_SERIAL [current\_design]

The configuration mode has now been set.

7. Use the get\_property command to confirm that the CONFIG\_MODE property was correctly set: get\_property CONFIG\_MODE [current\_design]

The property value M\_SERIAL is returned by the Vivado tool.

# **Step 5: Saving Constraints**

Notice that the Save Constraints icon is enabled because there are new design constraints. The cell and design properties you modified in Lab #2 have been added to the Vivado tool in-memory design, but are not yet saved to the target constraint file.

1. Click the Save Constraints button

The physical constraints you defined in Lab #2 are saved to the target constraint file.

2. Select the **target XDC** (in this case, timing.xdc) from the active constraint set in the Sources window to open the file in the Vivado IDE text editor.

*Note*: You might need to click on the *Reload* link to update the file if it is already opened in the *GUI*.

Notice that the seven set\_property commands you used in Lab #2 are saved to the constraint file. Only design constraints are written to the XDC file, not the object queries or reporting commands that you also used in this lab.

3. Look for the following constraints in the open constraint file:

```
set_property BEL MMCME2_ADV [get_cells clkgen/mmcm_adv_inst]
set_property LOC MMCME2_ADV_X1Y0 [get_cells clkgen/mmcm_adv_inst]
set_property PROHIBIT true [get_bels IOB_X1Y34/PAD]
set_property PROHIBIT true [get_sites AA8]
set_property DOA_REG 1 [get_cells \
{fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/infer_fifo.block_ram_\
performance.fifo_ram_reg}]
set_property DOB_REG 1 [get_cells \
{fftEngine/fftInst/ingressLoop[7].ingressFifo/buffer_fifo/infer_fifo.block_ram_\
performance.fifo_ram_reg}]
set_property CONFIG_MODE M_SERIAL [current_design]
```

4. Exit the Vivado IDE.





# Conclusion

In this lab, you learned how to use both the Vivado IDE and the Tcl Console to create and verify physical constraints. Most actions performed in the IDE result in Tcl commands being run in the Tcl Console. The Vivado IDE provides powerful interactive capabilities for developing physical and timing constraints, which can then be saved to constraint files and reused as needed.





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