Vivado Design Suite User Guide

Release Notes, Installation, and Licensing

UG973 (v2014.4) November 19, 2014

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/19/2014	2014.4	Featuring new Release Notes 2014.4 content and updated the Architecture Support and Requirements chapter to reflect the latest requirements.
10/20/2014	2014.3	Terminology updates in the Release Notes 2014.4 chapter.
10/01/2014	2014.3	Featuring new Release Notes 2014.4 content and updated the Architecture Support and Requirements chapter to reflect the latest requirements.
06/18/2014	2014.2	Updated Answer Record link.
06/04/2014	2014.2	Featuring new Download and Installation and Obtaining and Managing a License content.
05/06/2014	2014.1	Initial Xilinx release. Featuring new Download and Installation and Obtaining and Managing a License content.

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Appendix A: Additional Resources and Legal Notices

Release Notes 2014.4

What's New

Vivado® Design Suite 2014.4 adds device support for many of the 28nm and UltraScale™ devices. The Vivado® Design Suite 2014.4 supports new Artix®-7 and Zynq®-7000 devices as well as new low power Artix®-7, Kintex®-7, and Zynq®-7000 devices. Bitstream generation for additional UltraScale devices is also now enabled.

Device Support

The following new devices are enabled for this release.

Table 1-1: **Vivado 2014.4 Device Support**

Production Level	Vivado 2014.4 Device Support
General Access	• Zynq-7000, Artix-7, and Artix-7 Automotive: ◦ XC7Z035, XC7A15T, and XA7A15T • Support for -2LI and -1LI speed grades enabled for select 7 series and Zynq-7000 devices.
Early Access	• Virtex UltraScale devices: ◦ XCVU065, XCVU125, XCVU160, XCVU190 and XCVU440 • Contact Xilinx Field Application Engineer for access to these devices.

Bitstream Generation	• Bitstream generation for UltraScale devices are limited to:
	• Virtex UltraScale:
	  ◦ XCVU095 ES1
	• Kintex UltraScale:
	  ◦ XCKU040, XCKU060 ES2, XCKU115 ES2

Note: Part names aligned to silicon availability: XCKU040 ES1 is no longer supported and Multiple ES1 parts changed to ES2. Use the XCKU040 ES1 part along with 2014.2.

Licensing

• Virtual Machine support for Activation-based licenses

○ Virtual Machines are now supported for both client and server activation licenses. If you are using a VM machine, ensure that you are using Vivado 2014.4 or later utilities to initiate license generation.

• Introducing One-Step activation licensing

○ If using **Vivado License Manager**, for client (node-locked) licenses, and connected to the internet, Vivado License Manager downloads and install activation licenses automatically.

Vivado Design Edition Tools

Partial Reconfiguration

• The KU060 has been added to the supported list of UltraScale devices for place and route, joining the KU040 and VU095 devices.

○ Bitstream generation is disabled until ES2 silicon (Virtex UltraScale) or production silicon (Kintex UltraScale) is available.

• Partial bitstreams can be delivered over a PCIe® link by utilizing the dedicated MCAP connection. Enable the **PR over PCIe** Advanced option when customizing the PCIe IP for UltraScale devices only.

• For more information, see the *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909) [Ref 3].

Tandem Configuration

• Tandem PROM and Tandem PCIe is available as beta for the same UltraScale devices as supported for Partial Reconfiguration: KU040, KU060, and VU095.

○ Just as for Partial Reconfiguration, bitstream generation disabled until ES2 silicon (Virtex UltraScale) or production silicon (Kintex UltraScale) is available.

• For more information, see the *UltraScale Architecture Gen3 Integrated Block for PCI Express Product Guide* (PG156) v3.1.

Vivado Physical Implementation Tools

Clock Floorplanning Constraints:

• Clock Utilization Report (output of `report_clock_utilization`) includes clock floorplanning constraints at the end of the report.

• Provided as a convenience to lock down placement of global clock buffers and to floorplan the loads of the clocks to particular clock regions. While this is a useful feature for 7-Series to aid design closure involving complex clocking, it is not suitable for UltraScale designs.

- Fixing the LOC properties of `BUFGCE` global clock buffers to lock their placement can result in clock track contention and clock placement failures in UltraScale devices. Instead the `BUFGCE` should be assigned to a Pblock that covers the clock region containing its current location. In a future release, the clock floorplanning constraints will be updated for UltraScale to include this soft placement constraint for `BUFGCE`.

Power Analysis

Report Power in the IDE and `report_power` (Tcl) now support all UltraScale devices including UltraScale SSI devices.

Important Information

Updates to Existing IP

The following table lists current updates to existing IP for the 2014.4 release.

Table 1-2: **Existing IP Updates**

Existing IP	Existing IP Updates
10G Ethernet MAC	• New optional 32-bit low latency and size reduced IP • Added Zynq®-7000 AP Soc and 7 series defense grade devices
AXI 10G Ethernet MAC	• 10G Ethernet MAC and 10GBASE-KR or 10GBASE-R • Available in IP Integrator and IP Catalog • Added UltraScale Kintex® device support • Added Zynq-7000 AP Soc and 7 series defense grade devices
10GBASE-R	• New optional 32-bit low latency and size reduced IP • Added Zynq-7000 AP Soc and 7 series defense grade devices
AXI Ethernet Subsystem	• Added optional non processor mode (No AXI Buffer) • Available in IP Integrator and IP Catalog • TEMAC + 1000BASE-X with optional hardware timestamping for UltraScale Kintex® and 7 series
PCI Express®	• AXI-MM support for Gen3 PCI Express hard block (Virtex7 XT/HT). • Package Migration section in User Guide for UltraScale FPGA devices. • Tandem PCIe/PROM support (Beta) for UltraScale FPGA devices.
Aurora	• Additional UltraScale FPGA device support. • Simulation support with Labtools enabled. • AXI4-Lite to DRP interface compliance (Aurora 64B/66B).

Note: Part names aligned to silicon availability: XCKU040 ES1 is no longer supported and Multiple ES1 parts changed to ES2.

Documentation Navigator

- New integrated **Web Search Results** tab that searches for documents on Xilinx Support.

- Support for Design Hubs in the main Catalog View.

  ◦ Guided learning curve with recommended key concepts and FAQs.

- New **Send Feedback** link added to each Design Hub.

Vivado Design Suite Documentation Update

In the 2014.4 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2014.4 documentation suite.

Licensing

Activation licensing is not supported for USB dongles, on floating servers running SOLARIS OS, or on triple-redundant server configurations.

IP Known Issues and Change List

For Xilinx IP known issues, see the *IP Release Notes Guide* (XTP025) [Ref 7].

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 59464

Send Feedback

Architecture Support and Requirements

Operating Systems

Xilinx only supports the following operating systems on x86 and x86-64 processor architectures.

Microsoft Windows Support

- Windows 7 and 7 SP1 Professional (32-bit and 64-bit), English/Japanese
- Windows 8.1 Professional (64-bit), English/Japanese

Windows XP Support

For the Vivado 2014.4 release, Windows XP will no longer be supported. This is due, in large part, to Microsoft's termination of Windows XP support.

Linux Support

- Red Hat Enterprise Workstation 5.8 - 5.10 (32-bit and 64-bit)
- Red Hat Enterprise Workstation 6.4 - 6.5 (32-bit and 64-bit)
- SUSE Linux Enterprise 11.1 - 11.2 (32-bit and 64-bit)
- Cent OS 6.4 and 6.5 (64-bit)
- Ubuntu Linux 14.04 LTS (64-bit)

Architectures

The following table lists architecture support for commercial products in the Vivado®
Design Suite WebPACK™ tool versus all other Vivado Design Suite editions. For
non-commercial support:

- All Xilinx® Automotive devices are supported in the Vivado Design Suite WebPACK
tool.

- Xilinx Defense-Grade FPGA devices are supported where their equivalent commercial
part sizes are supported.

Table 2-1: **Architecture Support**

		Vivado WebPACK Tool	**Vivado Design Suite (All Other Editions)**
Zynq® Device		Zynq-7000 AP SoC Device • XC7Z010, XC7Z015, XC7Z020, XC7Z030	Zynq-7000 AP Soc Device • All
Virtex® FPGA		Virtex-7 FPGA • None Virtex UltraScale FPGA • None	Virtex-7 FPGA • All Virtex UltraScale FPGA • All
Kintex® FPGA		Kintex-7 FPGA • XC7K70T, XC7K160T Kintex UltraScale FPGA • None	Kintex-7 FPGA • All Kintex UltraScale FPGA • All
Artix® FPGA		Artix-7 FPGA • XC7A35T, XC7A50T, XC7A75T, XC7A100T, XC7A200T	Artix-7 FPGA • All

Compatible Third-Party Tools

Table 2-2: **Compatible Third-Party Tools**

Third-Party Tool	**Red Hat Linux**	**Red Hat Linux-64**	**SUSE Linux**	**Windows-7 32-bit**	**Windows-7 64-bit**	**Ubuntu**
Simulation						
Mentor Graphics Questa SIM SE/DE (10.3b)	Yes	Yes	Yes	Yes	Yes	N/A
Mentor Graphics Questa SIM PE (10.3b)	N/A	N/A	N/A	Yes	Yes	N/A
Mentor Graphics Questa Advanced Simulator(10.3b)	Yes	Yes	Yes	Yes	Yes	N/A

Table 2-2: **Compatible Third-Party Tools**

Third-Party Tool	Red Hat Linux	Red Hat Linux-64	SUSE Linux	Windows-7 32-bit	Windows-7 64-bit	Ubuntu
Cadence Incisive Enterprise Simulator (IES) (13.20.005)	Yes	Yes	Yes	N/A	N/A	N/A
Synopsys VCS and VCS MX (I2014.03)	Yes	Yes	Yes	N/A	N/A	N/A
The MathWorks MATLAB® and Simulink® with Fixed-Point Toolbox (2013a, 2013b, and 2014a)	Yes	Yes	Yes	Yes	Yes	N/A
Aldec Active-HDL (9.3sp1)[a]	N/A	N/A	N/A	Yes	Yes	N/A
Aldec Riviera-PRO (2014.02)	Yes	Yes	Yes	Yes	Yes	N/A
Synthesis[b]						
Synopsys Synplify/Synplify Pro (J-2014.09-SP1)[c]	Yes	Yes	Yes	Yes	Yes	N/A
Mentor Graphics Precision RTL/Plus (2012c)	Yes	Yes	Yes	Yes	Yes	N/A
Equivalence Checking						
Cadence Encounter Conformal (9.1)[d]	Yes	Yes	Yes	N/A	N/A	N/A
OneSpin 360 (2013_12)	Yes	Yes	Yes	N/A	N/A	N/A

a.   **Note:** Support for Aldec simulators is offered by Aldec.

b.   **Note:** Most Vivado IPs can only be synthesized by Vivado synthesis, because the RTL source can include encrypted files. To use these IPs in a third party synthesis flow, the synthesized netlist can be exported from the Vivado tool in a suitable format for use in the third-party synthesis project.

c.   **Note:** Contact Synopsys for availability of Synplify Overlay or Service Pack.

d.   **Note:**Cadence Encounter Conformal Support is for RTL2Gate using Synopsys Synplify only.

Note: System Generator support is restricted to operating systems that are compatible with The MathWorks MATLAB and Simulink tools.

System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

The lab exercises require the installation of MATLAB 2014a (or later) and Vivado Design Suite 2014.2 (or later).

System Memory Recommendations

For memory recommendations for the Vivado Design Suite tools, see:
http://www.xilinx.com/design-tools/vivado/memory.htm.

Operating Systems and Available Memory

The Microsoft Windows and Linux operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs might encounter this limitation. The Vivado Design Suite has optimized memory and enabled support for applications to increase RAM memory available to Xilinx tools.

Linux

For 32-bit Red Hat Enterprise Linux systems, the operating system can use the hugemem kernel to allocate 4 GB to each process. More information can be found on the Red Hat support site at http://www.redhat.com/docs/manuals/enterprise/.

Cable Installation Requirements

Platform Cable USB II is a high-performance cable that enables Xilinx design tools to program and configure target hardware.

Note: The Xilinx Parallel Cable IV is no longer supported for debugging or programming.

RECOMMENDED: *To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.*

The cable is officially supported on the 32-bit and 64-bit versions of the following operating systems: Windows-7, Red Hat Linux Enterprise, and SUSE Linux Enterprise 11. Additional platform specific notes are as follows:

- Root privileges are required.

- SUSE Linux Enterprise 11: The fxload software package is required to ensure correct Platform Cable USB II operation. The fxload package is not automatically installed on SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.

- Linux LibUSB support: Support for Platform Cable USB II based upon the LibUSB package is now available from the Xilinx website, see Answer Record 29310.

For additional information regarding Xilinx cables, refer to the following documents:

- *USB Cable Installation Guide* (UG344) [Ref 8]
- *Platform Cable USB II Data Sheet* (DS593) [Ref 9]

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Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

Table 2-3: **Equipment and Permissions Requirements**

Item	Requirement
Directory permissions	Write permissions must exist for all directories containing design files to be edited.
Monitor	16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels.
Drive	You must have a DVD-ROM for Vivado Design Suite (if you have received a DVD, rather than downloading from the web).
Ports	To program devices, you must have an available parallel or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable. **Note:** Installation of the cable driver software requires Windows-7. If you are not using one of these operating systems, the cables might not work properly.

Note: X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

Download and Installation

This guide explains how to download and install the Vivado® Design Suite tools, which includes the Vivado Integrated Design Environment (IDE), High Level Synthesis tool, and System Generator for DSP.

Downloading the Vivado Design Suite Tools

Xilinx® Design Tools users can customize, download and install only those tools and devices required prior to download. Users will download and launch a lightweight installer (< 50 MB) from our website that will guide the user through the customization, download and installation process. This reduces the download size and speeds up the download & installation process considerably.

You will continue to have the choice of downloading a single file full product installation from our website.

Both download options are available on the Xilinx website: http://www.xilinx.com/support/download/index.htm

Most files in the Xilinx Download Center are downloaded using the Akamai download manager. For the optimum download experience:

• Allow pop-ups from entitlenow.com.

• Set security settings to allow for secure and non-secure items to be displayed on the same page.7000 AP Soc

• Allow the Akamai download manager to run Java processes.

To download the Xilinx Design Tools:

1. Select the **Design Tools** tab in the web page.

2. Under the Version heading, click the version of the tools you want to download.

3. Click the link for the installer you want to download.

Note: The 32-bit installer will only work on 32-bit operating systems and is not supported on 64-bit machines.

Installing the Vivado Design Suite Tools

This section explains the installation process for all platforms for the Vivado Design Suite.

Installation Preparation

IMPORTANT: *Before starting installation the follow steps must be completed:*

- Check the links in Important Information section in Chapter 1 for any installation issues pertaining to your system or configuration.

- Make sure your system meets the requirements described in Chapter 2, Architecture Support and Requirements.

- Disable anti-virus software to reduce installation time.

- Make sure you have the necessary privileges for the system on which the design tools will be installed. Some components, such as programming cable device drivers, require administrator-level permissions.

- Close all open programs before you begin installation.

- The Vivado Design Suite installer does not set global environment variables, such as XILINX, on Windows.

- When running `xsetup.exe` from a 32-bit machine onto the network location of a 64-bit machine, the tools install the 32-bit executables onto that machine and not the 64-bit executables.

Full Product Download and DVD

If you downloaded the full product installation, decompress the file and run xsetup (for Linux) or xsetup.exe (for Windows) to launch the installation. If you received a DVD, launch xsetup(.exe) directly.

RECOMMENDED: *Xilinx recommends the use of 7-zip or WinZip (v.15.0 or newer) to decompress the downloaded tar.gz file.*

Lightweight Installer Download

If you downloaded the lightweight installer, launch the downloaded file. You are prompted to log in and use your regular Xilinx login credentials to continue with the installation process.
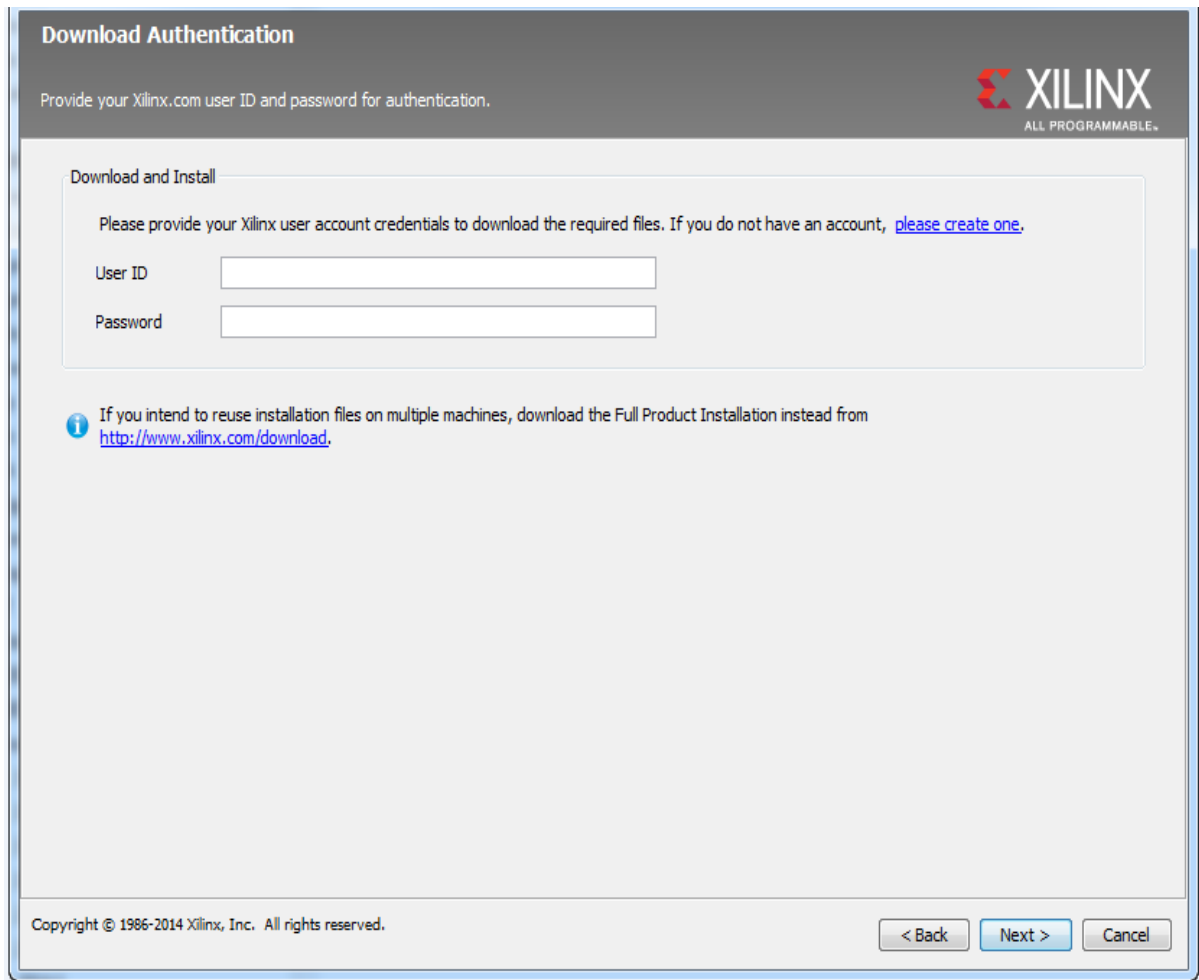
Figure 3-1: **Vivado Design Suite Installation - Select Installation Source**

Connectivity

The installer connects to the internet through the system proxy settings in Windows. These settings can be found under **Control Panel > Network and Internet > Internet Options**. For Linux users, the installer uses Firefox browser proxy settings (when explicitly set) to determine connectivity.

Figure 3-2: **Vivado Design Suite Installation - Connectivity**

If there are connectivity issues, verify the following:

1. If you are using alternate proxy settings to the ones referred to, select the **Manual Proxy Configuration** option to specify the settings.
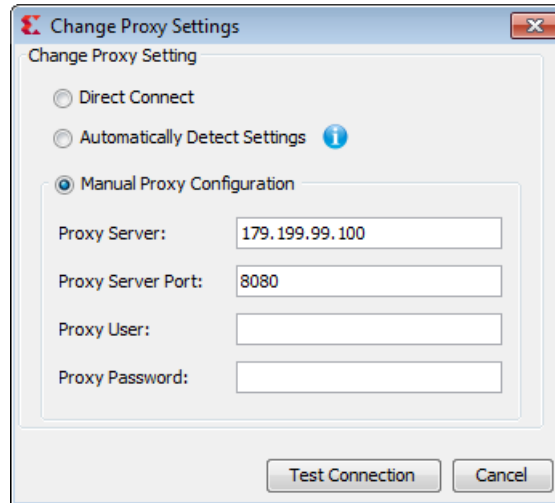

Figure 3-3: **Vivado Design Suite Installation - Change Proxy Settings**

2. Check if your company firewall requires a proxy authentication with a username and password. If so, select the **Manual Proxy Configuration** option in the dialog box above.

3. For Linux users, if either the **Use System settings** or the **Auto detect settings** option is selected in the Firefox browser, you must manually set the proxy in installer.

License Agreements

Carefully read the license agreements before continuing with the installation. If you do not agree to the terms and conditions, cancel the installation and contact Xilinx.

Edition Selection

Select the edition or standalone tool that is required. You can also install Software Development Kit (SDK) as part of the Vivado WebPACK, System and Design editions.
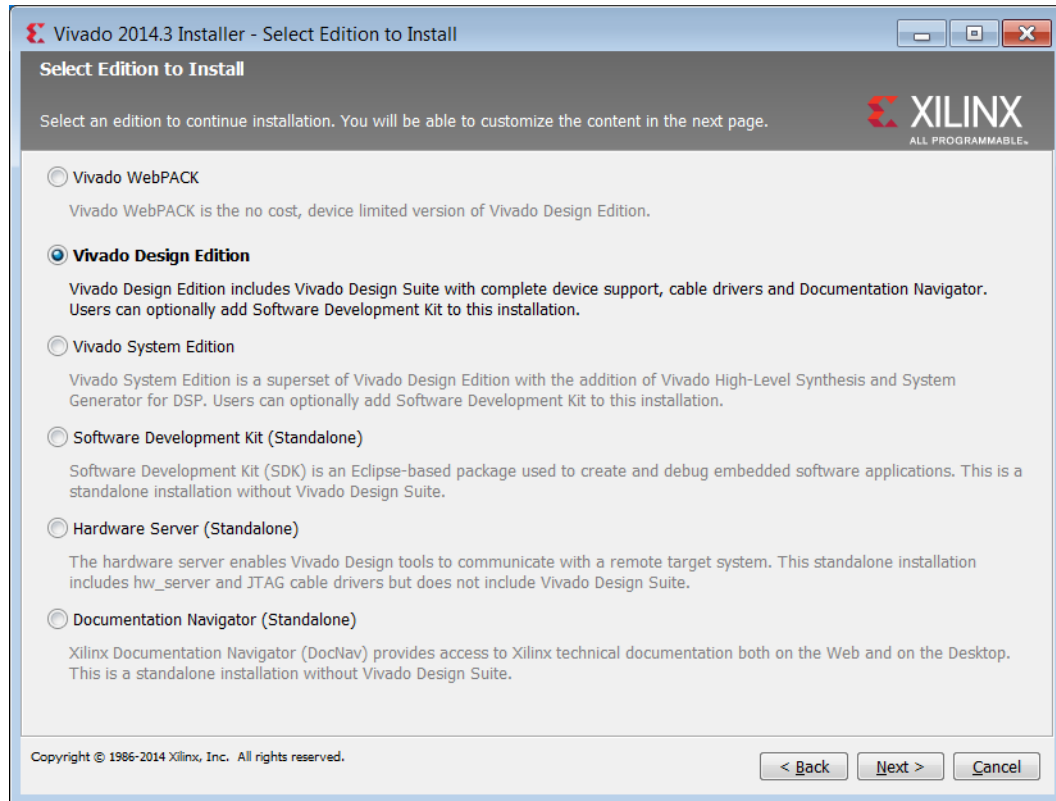
Figure 3-4: **Vivado Design Suite Installation - Select Products**

Vivado WebPACK and Design edition users will also be able to upgrade to a higher edition post installation. See Adding Additional Tools and Devices, page 20 for more details.

Tools, Devices, and Options

Customize the installation by choosing the design tools, device families and installation options. Selecting only what you need helps to minimize the time taken to download and install the product. You will be able to add to this installation later by clicking **Add Design Tools or Devices** from either the operating system Start Menu or the **Vivado > Help** menu.
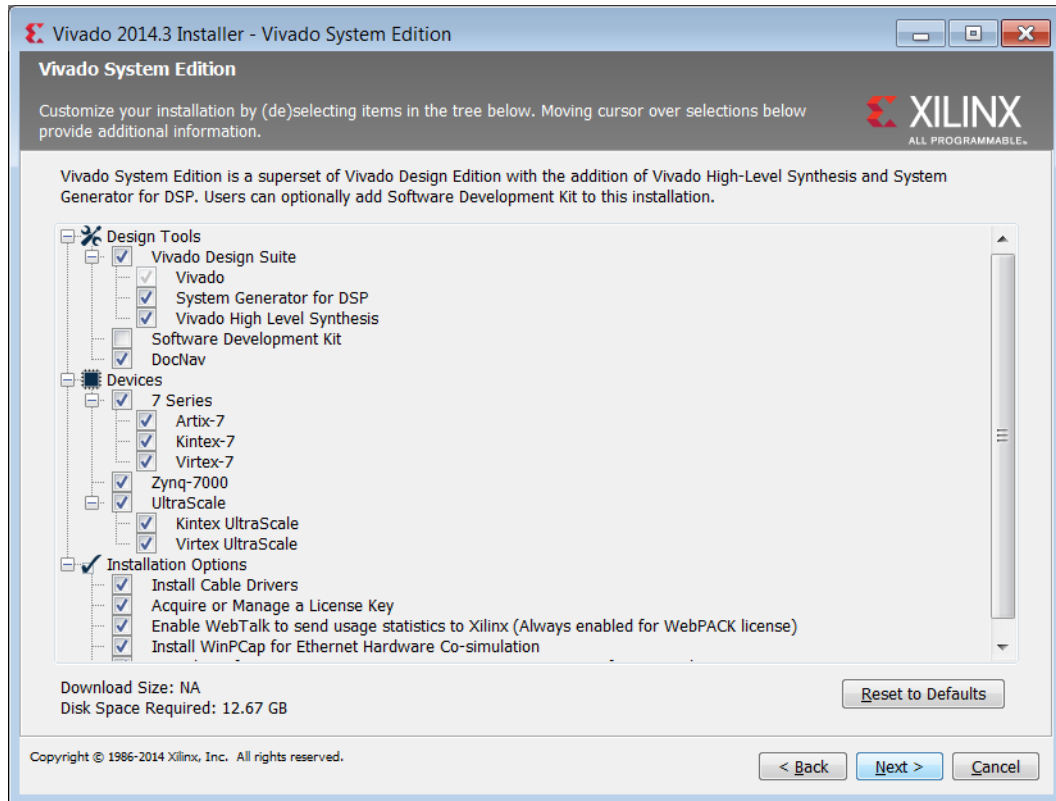
Send Feedback

Figure 3-5: **Vivado Design Suite Installation - Vivado System Edition**

Shortcuts and File Associations

You can customize the creation of the program group entries (Start Menu) and the creation of desktop shortcuts. Optionally, you can also create file associations to launch Vivado project files directly with this version of Vivado. The shortcut creation and file association options can be applied to the current user or all users.

Adding Additional Tools and Devices

Starting in 2014.2, you can incrementally add additional tools, devices or even upgrade Vivado editions post-install. This is useful for users that have chosen to install a subset of devices and/or tools.

To add new tools or devices:

• **Start Menu > Xilinx Design Tools > Vivado <version> > Add Design Tools** or **Devices**.

• Launch **Vivado > Help > Add Design Tools** or **Devices**.

If you have installed the Vivado WebPACK or Design Edition, you are presented with the option to upgrade the edition.
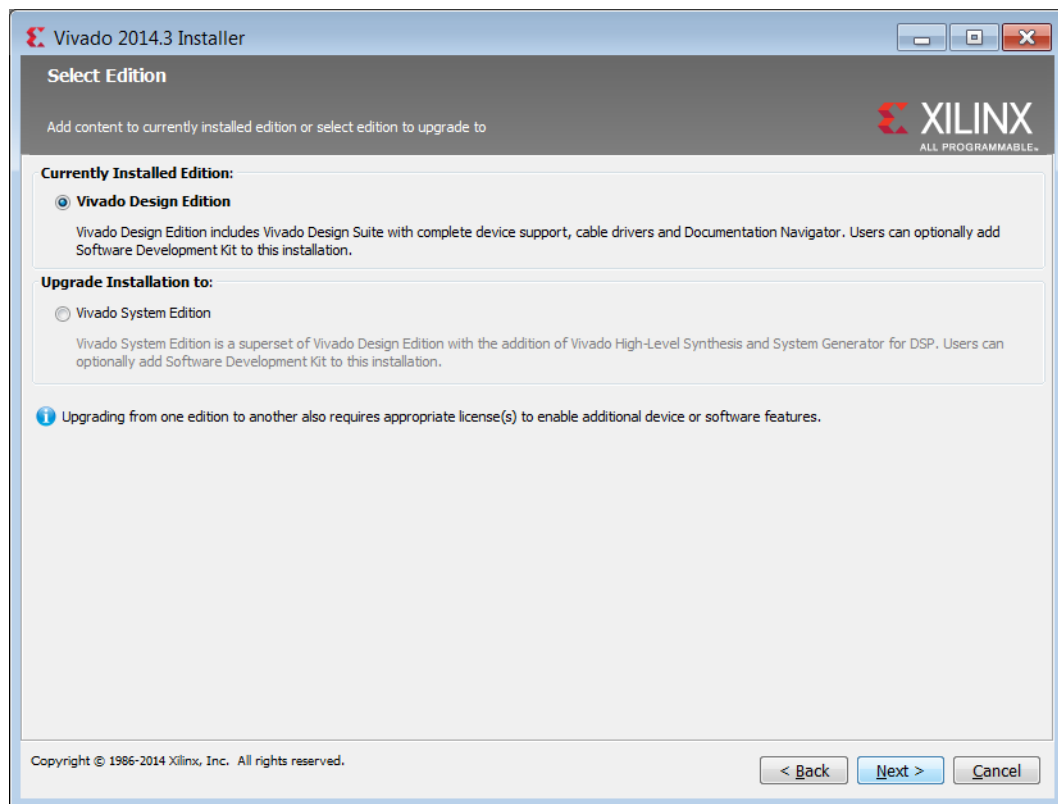

Figure 3-6: **Vivado Design Suite Installation - Select Edition**

Based on the above selection, you are presented with all available tools and devices that can be added to the current installation.
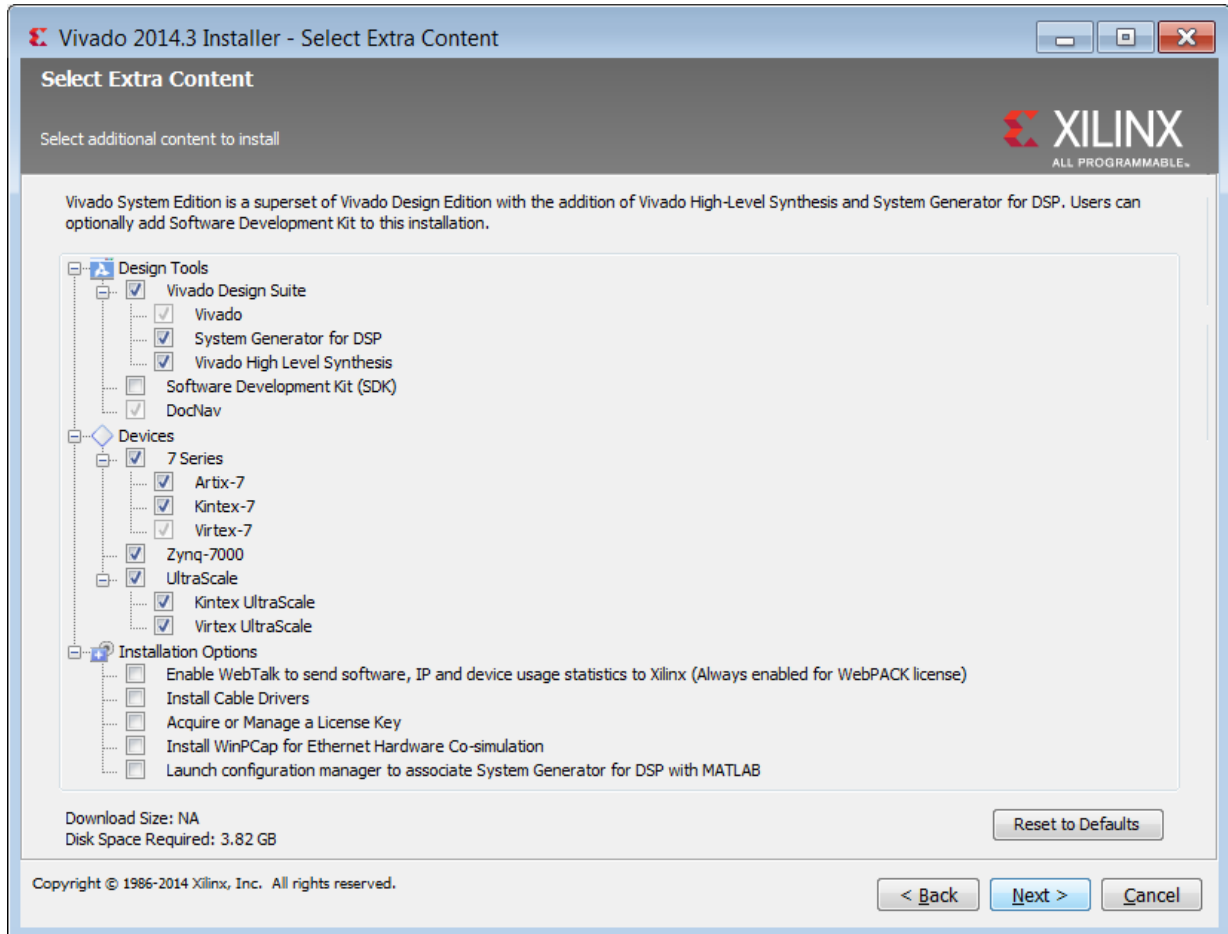
Figure 3-7: **Vivado Design Suite Installation - Select Extra Content**

Network Installations

Installing to a network location provides a way for client machines to access the design tools by pointing to it on the network drive. To run the design tools on the network, the client machines must be set up correctly to ensure the environment variables, registry, and program groups all point to the network. The following sections describe the procedure for network setups.

Linux Clients

You must source `settings32.(c)sh` or `settings64.(c)sh` (whichever is appropriate for your operating system) from the area in which the design tools are installed. This sets up the environment to point to this installed location.

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To run the design tools from a remotely installed location, run an X Windows display manager, and include a DISPLAY environment variable. Define `DISPLAY` as the name of your display. DISPLAY is typically `unix:0.0`. For example, the following syntax allows you to run the tools on the host named bigben and to display the graphics on the local monitor of the machine called mynode.

```
setenv DISPLAY mynode:0.0
xhost = bigbenPC Clients
```

Microsoft Windows Clients

1. Install design tools to a PC network server. Make sure your users know the location of the design tools and have access to the installation directory, and they have Administrator privileges for the following steps.

2. From the local client machine, browse to the following directory: `network_install_location\.xinstall\Vivado_<version>` and run the program `networkShortcutSetup.exe`.

    Running this program sets up the Windows settings batch files and **Program Group** or **Desktop** shortcuts to run the Xilinx tools from the remote location.

3. From the client machine, launch the Vivado Design Suite tools by clicking the **Program Group** or **Desktop** shortcuts, or by running the applications on the network drive.

Installing to a Mounted Network Drive

Xilinx design tools are designed to be installed in a directory under ROOT (typically `C:\Xilinx`). The installer normally presents this option when installing to a local driver.

To work around this issue, either specify a UNC path (for example, `\\network_loc\Xilinx\`) or define your target installation directory as `\Xilinx` under the network mount point (For example: `N:\Xilinx`).

Windows 7 default security levels do not allow you to select remote mapped drives. To install Xilinx Design Tools on remote mapped drives, you must change your account control settings using the following steps:

1. Open the Windows Control Panel, from the Windows Start menu, and select 'User Accounts'. If your Control Panel Uses 'Category View', click 'User Accounts' on two successive screens

2. Click 'Change User Account Control settings' and allow the program to make changes.

3. Click and slide the slide-bar down to the second to lowest setting (as seen in the following figure).
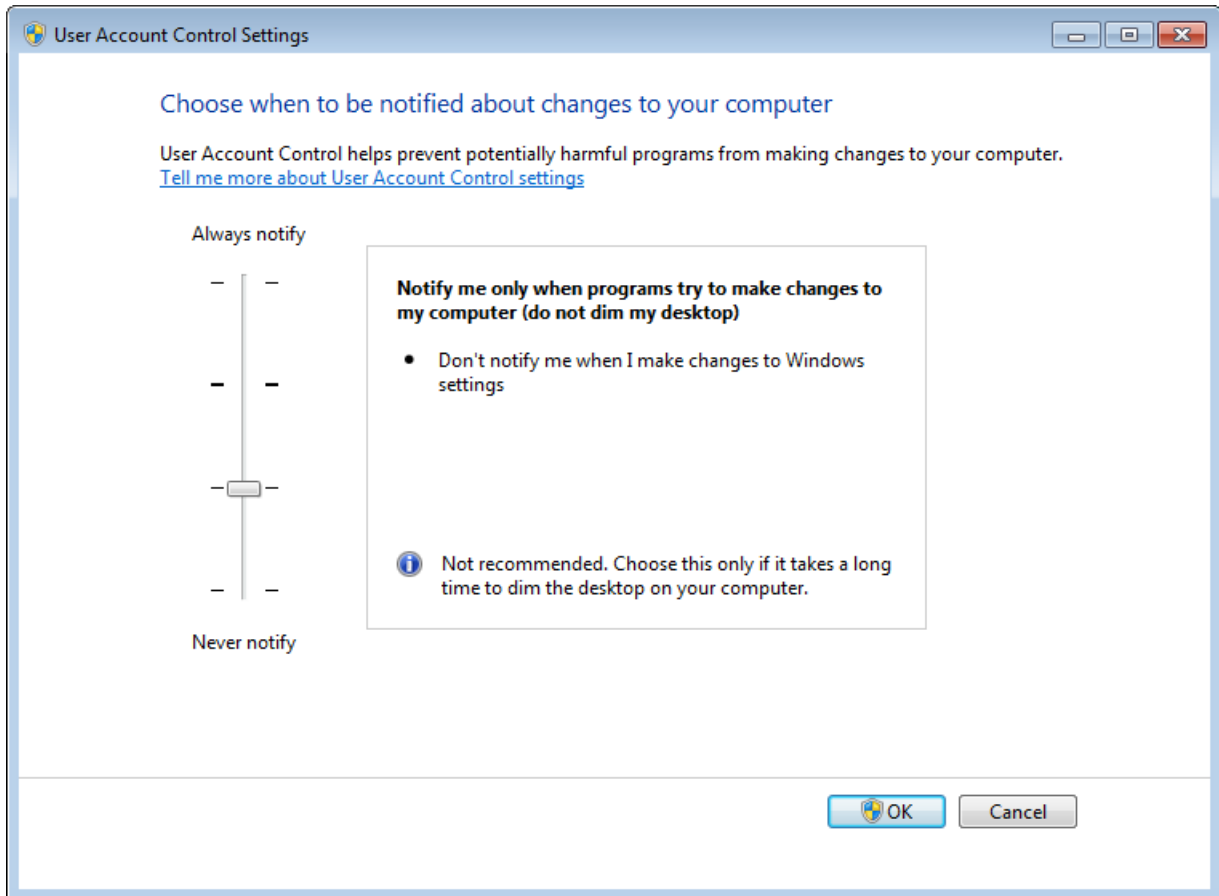
4. Click **OK**.

Figure 3-8: **Vivado Design Suite Installation - User Account Control Settings**

RECOMMENDED: *Xilinx recommends that you revisit this procedure to restore your settings to their previous state after installation.*

Note: You are not able to browse to the remote mapped drives using the Xilinx installer. You need to manually type in your installation path which contains a mapped network drive.

Obtaining Quarterly Releases

Xilinx releases quarterly versions of the Vivado Design Suite tools throughout the year. Each quarterly version contains device support updates, new features and bug fixes. The following sections describe how to obtain updates through the Xilinx Information Center.

Xilinx Information Center

Xilinx Information Center (XIC) is the next generation replacement of XilinxNotify. This functionality resides in the task bar (Windows) and periodically checks for new releases and updates from Xilinx. Users can view and dismiss notifications as well as update installations.

Send Feedback

In addition, XIC now includes a cockpit from which you can manage all of your Xilinx tool installations. Update, check licenses or uninstall all from the new Manage Installs tab.
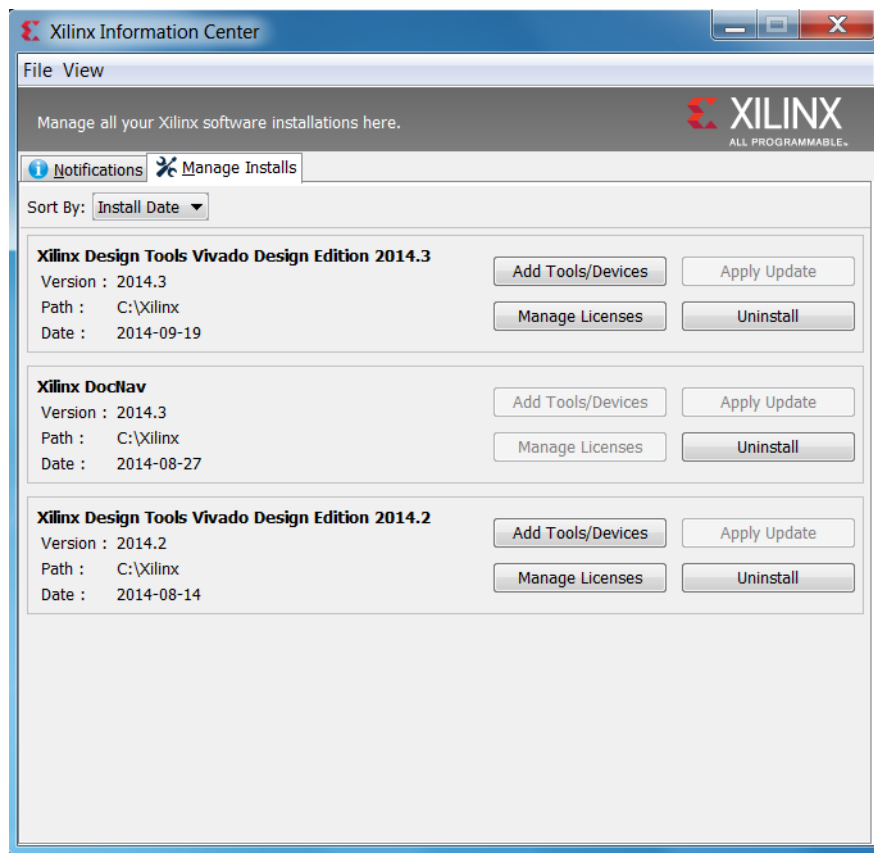

Figure 3-9: **Xilinx Information Center (XIC)**

Uninstalling the Vivado Design Suite Tool

Before uninstalling, make sure to have moved any project files you want to keep outside your Xilinx installation directory structure, or they are deleted.

Note: Xilinx Documentation Navigator is not removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. You need to uninstall it separately if it is no longer required.

Uninstallation

Before uninstalling, make sure to have moved any project files you want to keep outside your Xilinx installation directory structure, or they will be deleted. See below for information on uninstalling Documentation Navigator and Xilinx Information Center.

Uninstalling Documentation Navigator

Xilinx Documentation Navigator will not be removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. If it is no longer required, you will need to uninstall separately either from the Start Menu program group entry 'Uninstall DocNav' or through the corresponding entry in the 'Uninstall or change a program' control panel option (for Windows).

Uninstalling Xilinx Information Center

Xilinx Information Center will not be removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. If it is no longer required, you will need to uninstall separately through the corresponding entry in the 'Uninstall or change a program' control panel option (for Windows).

Uninstalling on Microsoft Windows

To uninstall the Vivado Design Suite tool product, launch the uninstaller from the launcher menu: select **Applications > Xilinx Design Tools > Vivado 2014.4 > Uninstall**.

Uninstalling on Linux

To uninstall any Xilinx product, select the Uninstall item from that product's Start Menu folder. For instance, to uninstall Vivado Design Suite: Edition, select **Start > All Programs > Xilinx Design Tools > Vivado 2014.4 > Uninstall**.

If you do not have a program group entry, use the command line option to uninstall:
`<install_path>\.xinstall\Vivado_2014.4\ xsetup.exe -Uninstall`

Alternatively, use the corresponding entry in the Uninstall or change a program control panel option (for Windows).

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WebTalk

The WebTalk feature helps Xilinx understand how you use Xilinx® FPGA devices, software, and intellectual property (IP). The information collected and transmitted by WebTalk allows Xilinx to improve the features most important to you as part of our ongoing effort to provide products that meet your current and future needs. When enabled, WebTalk provides information on your use of the Vivado® Design Suite tools.

WebTalk Participation

Your participation in WebTalk is voluntary except in the following cases:

• You are using a WebPack™ license.

• You are using pre-release software or devices.

In these cases, WebTalk data collection and transmission always occurs, regardless of your preference settings. For all other cases, data is not transmitted if you disable WebTalk.

The following table summarizes WebTalk behavior for data transmission to Xilinx from your post-route design, based on your Xilinx license, WebTalk install preference, and user preference settings.

Table 4-1:   **WebTalk Behavior for Bitstream Generation or Route Design Flow**

Early Access Devices	License	WebTalk Install Preference Selected as "Enabled"	WebTalk User Preference Selected as "Enabled"	Send WebTalk Data to Xilinx
Yes	X	X	X	Yes
No	WebPACK™	X	X	Yes
No	Edition License	No	X	No
No	Edition License	Yes	No	No
No	Edition License	Yes	Yes	Yes

Note: If the device is a WebPACK device, the Tools first look for a WebPACK license.

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Setting WebTalk Install Preference

You can enable or disable WebTalk globally during or after installation as described below. During installation you can enable or disable WebTalk installation options by checking or unchecking the **Enable WebTalk to send software, IP and device usage statistics to Xilinx (Always enabled for WebPACK license)** checkbox.
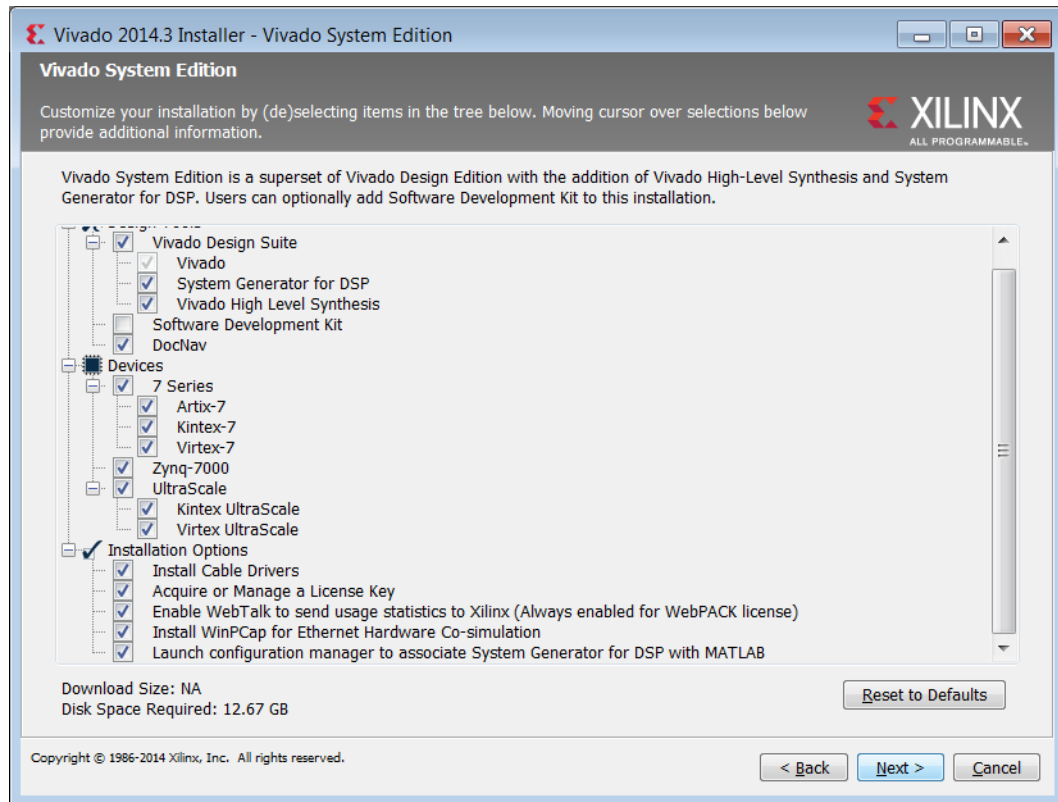

Figure 4-1: **WebTalk Install Options**

You can enable or disable WebTalk installation options using the Tcl command `config_webtalk`:

```
config_webtalk -install on|off
```

- `on` turns WebTalk on for the installation.

- `off` turns WebTalk off for the installation.

Install settings are saved in the following location:

- **Windows 7**: `<install dir>/vivado/data/webtalk/webtalksettings`

- **Linux**: `<install dir>/vivado/data/webtalk/webtalksettings`

Note: You need administrator privileges to write to the install location.

Setting WebTalk User Preferences

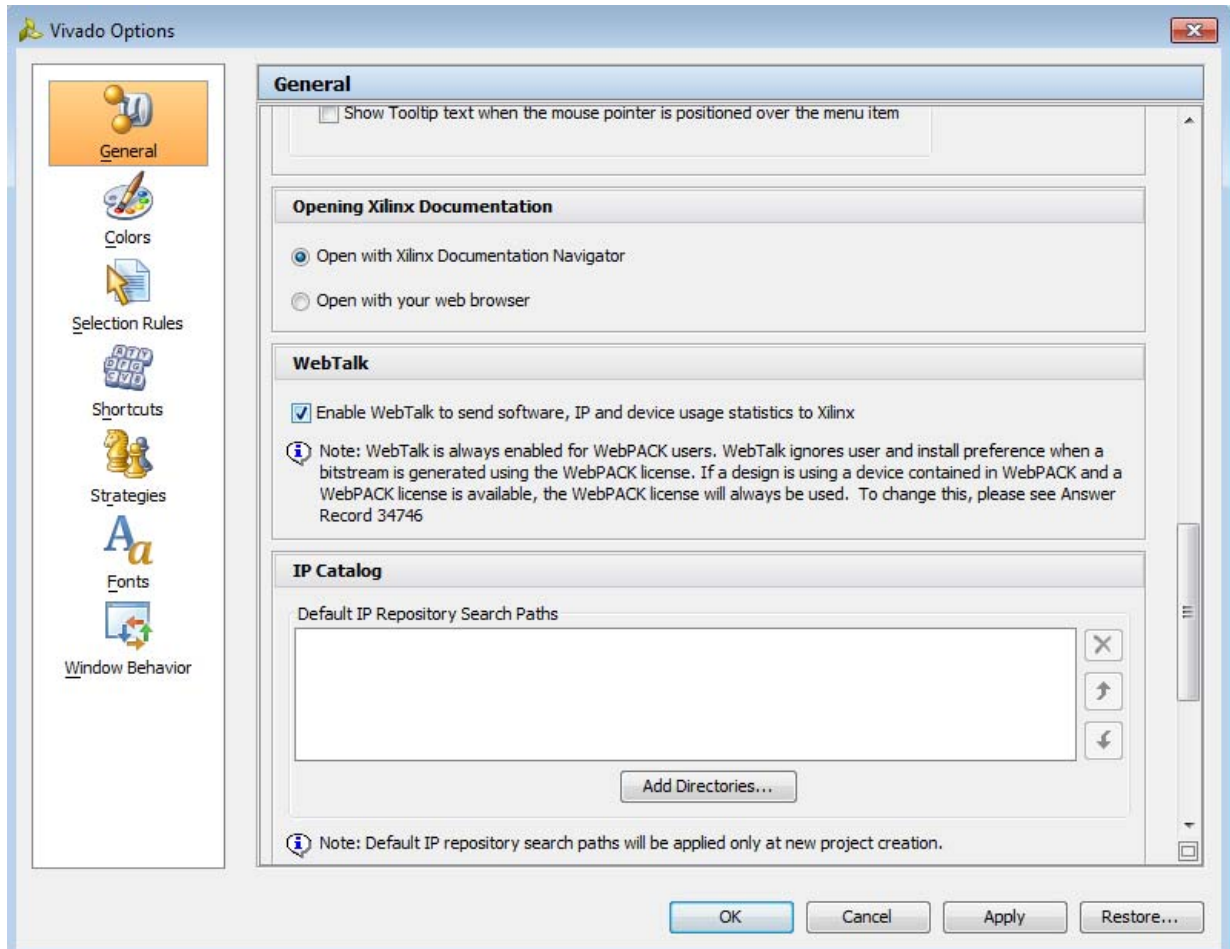You can enable or disable WebTalk user options by selecting **Tools > Options > General** as shown below.

Figure 4-2: **WebTalk User Preferences**

After installation, you can enable or disable WebTalk user options using the `config_webtalk` Tcl command:

```
config_webtalk -user on|off
```

* `on` turns WebTalk on for the current user.

* `off` turns WebTalk off for the current user.

User settings are saved in the following location:

- **Windows 7**:

  `%APPDATA%\Xilinx\Common\<version>\webtalk`

  where:

  `%APPDATA%` is:

  `C:\Users\<user>\AppData\Roaming`

- **Linux**:

  `%APPDATA%/.Xilinx/Common/<version>/webtalk`

  where:

  `%APPDATA%` is:

  `/home/<user>`

Checking WebTalk Install and User Preferences

You can also use the `config_webtalk` Tcl command to check the current status of WebTalk settings. The command line option `-info` reports the values for the install setting and the user setting:

`config_webtalk -info`

Types of Data Collected

WebTalk does not collect your design netlist or any other proprietary information that can be used to reverse engineer your design. The data Xilinx collects through WebTalk includes:

- Software version

- Platform information (for example, operating system, speed and number of processors, and main memory)

- Unique project ID

- Authorization code

- Date of generation

- Targeted device and family information

Send Feedback

For more information on the type of data that is collected, see the Xilinx Design Tools WebTalk web page [Ref 12]. To see the specific WebTalk data collected for your design, open the `usage_statistics_webtalk.xml` file in the project directory. You can also open the `usage_statistics_webtalk.xml` file for easy viewing of the data transmitted to Xilinx.

Transmission of Data

WebTalk is invoked after bitstream or route design compilation. WebTalk bundles the collected data in an `usage_statistics_webtalk.xml` file and sends this file to Xilinx by https (hypertext transfer protocol secure) post. Every new compilation for a given design overwrites the previous `usage_statistics_webtalk.xml` file. WebTalk also writes an HTML file equivalent `usage_statistics_webtalk.html` file for easy viewing of the data transmitted to Xilinx. WebTalk also writes to the `vivado.log` (or `runme.log`) file that contains additional information about whether the file was successfully transmitted to Xilinx.

Send Feedback

Obtaining and Managing a License

The Xilinx® Product Licensing site is an online service for licensing and administering evaluation and full copies of Xilinx design tools and intellectual property (IP) products. This chapter describes the FLEXnet license generation functionality of the Product Licensing Site.

Licensing Overview

Two Product Licensing Methodologies

There are now two ways in which Xilinx enforces the Xilinx End-User License Agreement at run time in the Xilinx design tools.

- **Certificate-based licenses**: This is the license enforcement method Xilinx introduced for the ISE® Design Suite in the ISE® 11.1 release. A certificate, commonly referred to as a "license file (`.lic`)" is issued from the Xilinx Product Licensing Site. The certificate is matched to a given machine, server or licensing dongle using the user entering a host-id which uniquely identifies the machine. This license certificate must remain present on the machine and in the license search path, because the Vivado tools need access to this file to check for a valid license feature during runtime.

- **Activation licenses**: Instead of requiring a file to be present to authorize a machine, Activation uses a trusted area on the client or servers hard-drive to store the authorization credentials. This trusted storage area will automatically be installed and initialized beginning with the Vivado 2014.4 installer. When the Vivado tools look for a license feature, they are allowed to run if this trusted storage area contains the proper authorization. Since activation-based licenses do not use a license file, they will not work with USB license dongles.

Certificate Licensing Terminology

- **Host ID**: An identifier, placed within certificate licenses, which binds the license to the computer using this identifier. Typical identifiers are: Hard-drive volume ID, Ethernet port MAC address, or USB Dongle ID.

- **Node-Locked License**: A node-locked license allows for the use of a single seat of a product entitlement on a specific machine.

Send Feedback

- **Floating License**: A floating license resides on a network server and enables applications to check out a license when they are invoked. At any one time, the number of licenses for simultaneous users is restricted to the number of license seats purchased.

- **License Rehosting**: The act of changing the host ID of a generated license due to machine hardware changes, hard-drive failure or the moving of a license from one machine to another.

- **License Deletion**: The act of removing a license from a machine, and having the entitlement placed back into the Xilinx Product Licensing Account.

- **Affidavit of Destruction**: A click through agreement by which you certify that the license file (.lic) for a rehosted or deleted license will be destroyed and no longer used.

Activation Licensing Terminology

- **Client License**: A client license allows for the use of a single seat of a product entitlement on a specific machine. This is the activation-based equivalent of a certificate-based node-locked license.

- **Server License**: A server license is the activation-based equivalent of a certificate-based floating license. A server license resides on a network server and enables applications to check out a license when they are invoked. At any one time, the number of licenses for simultaneous users is restricted to the number of license seats purchased.

- **Trusted Storage**: The area where activation license host information and authorizations are stored.

- **Request Creation**: Activation licensing is based upon a request/fulfillment system. A request for a new license must first be recorded into trusted storage. This is done automatically by the Vivado License Manager whenever you use the **Connect Now** or **Save Information** buttons on the Obtain a License screen. After a request identifier is created, it is sent to the Xilinx Product Licensing Site along with the host information. When a license is generated on the Licensing Site, a fulfillment XML file is created with this same request identifier. When the activation fulfillment XML file is loaded into trusted storage by **VLM's Activate License** button, activation will be successful only if the request identifier on the fulfillment matches the one stored in trusted storage. Once the license is activated, the request becomes inactive and a new request can be made for additional licenses.

- **Return License**: With activation, license rehosting, license deletion and affidavits of destruction are no longer necessary. Activation features a methodology by which you can initiate a return of a license to Xilinx from the client or server machine. When the return request is made, the license is disabled on the local machine, and a return request is sent to the Xilinx Product Licensing Site. Once processed, the return request causes an entitlement to be placed back in your Product Licensing Account, and a message is sent to trusted storage to remove the returned license from the machine.

License Compatibility

The Vivado 2014.2 release and later recognizes both certificate and activation-based licenses. If the license versions and dates are valid for the tool version being used, it does not matter whether the license is certificate or activation-based. For example, a certificate-based license issued during a previous Vivado release, which is still within the 1-year subscription period will authorize Vivado 2014.2 or later software. No conversion to a new license methodology is necessary during the remainder of a previous subscription period.

Activation Licensing Transition

During the Vivado 2014 release cycle, activation-based licensing is the default for all customers upon purchasing a new Vivado Design Suite tool subscription. In the past, tool subscribers received a single certificate license that enabled both ISE and Vivado. Beginning in 2014.2, new Edition purchases will receive two license entitlements, a certificate-based entitlement that can be used with ISE 14.7 or previous versions, and an activation entitlement for Vivado tools. IP licenses are not transitioning to activation entitlements at this time, so will continue to be certificate-based.

Differences with Activation Licenses

To authorize the trusted storage area, activation records need to be sent from the Xilinx Product Licensing Site to the client or server machine. Currently, this is done by using XML files with encrypted authorizations. When you generate an Activation license, you receive an XML file by email, much like you might have received a certificate file (`.lic`) in the past. The difference is that certificate .lic files need to be continually accessed by the Xilinx software, and so must be retained and in a valid license search path. The XML activation record is used to load the authorization into the trusted storage area. After the authorization has been loaded, the XML activation record is no longer needed.

To generate licenses based on activation entitlements, a request for a license must first be made into the client or server computer's trusted storage area. For client (node-locked) activation license requests, Vivado License Manager or the command-line utility `xlicclientmgr` must be used. For server (floating) license requests, the command-line utility `xlicsrvrmgr` must be used. For more information on the `xlicclientmgr` or `xlicsrvrmgr` utilities, see the Using Xlicclientmgr Command-Line Utility or Using Xlicsrvrmgr Command-Line Utility section.

After this request is processed, a URL to the Xilinx Product Licensing Site will be generated and will contain the id of the request along with specific machine identification information of the Xilinx Product Licensing Site. This URL should be placed into a web browser, and if activation entitlements exist, they are accessible in the Activation-Based Licenses section of the Create New Licenses tab of the Xilinx Product Licensing Site.

Send Feedback

If you enter the Xilinx Product Licensing Site directly or through older Xilinx license managers, the machine identification necessary to generate an activation-based license will not be present. In this case, the Activation-Based Licenses section of the website will be inactive, and only certificate licenses will be available for generation.

See the 'Creating A License Key' section of this chapter for step-by-step instruction.

Managing Licenses On Your Machine

Using Vivado License Manager

Access to Vivado® License Manager is provided on computers with the Xilinx Vivado tools loaded.
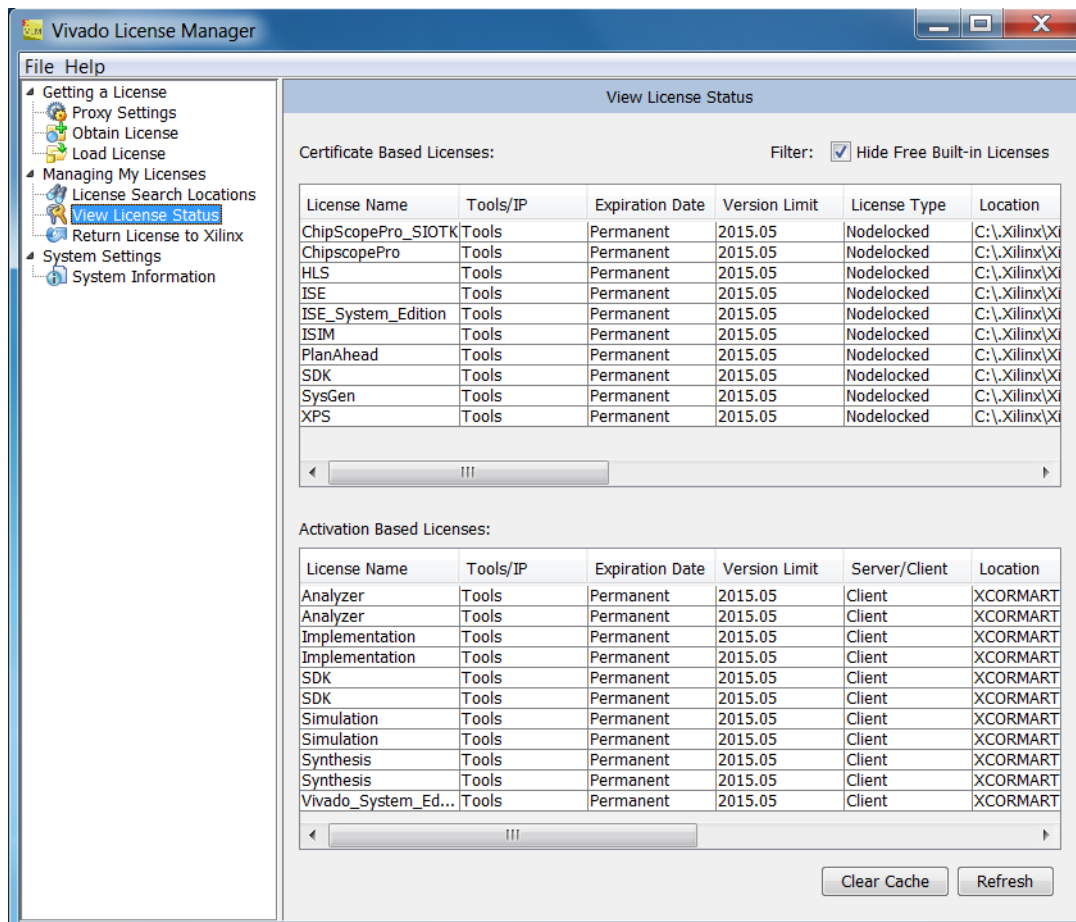
Figure 5-1: **Vivado License Manager**

To open the Vivado License Manager:

- On Linux, type `VLM` from a command-line shell that has the Xilinx environment loaded. On Windows 7 or earlier, you can run this from the Start menu at **Start > Xilinx Design Tools > Vivado 2014.4 > Manage Xilinx licenses**.

- On Windows 8.1, run the **Manage Xilinx Licenses** app from the full listing of Apps on your Start screen. You can also run Vivado License Manager from the Help menu of Vivado: **Help > Obtain A License Key** or **Help > Manage License**.

The typical tasks that Vivado License Manager is used for are:

- **Obtaining A License**: Choose from several license options and go to the Xilinx Product Licensing Site to complete the license generation process. To generate a license for an activation-based entitlement, Vivado License Manager should be used to access the Xilinx Product Licensing Site. This can be done on the **Obtain a License** screen by pressing **Connect Now**, if an internet connection is present, or by pressing **Save Information** if one is not. **Save Information** will save the information that Vivado License Manager normally passes to the Xilinx Product Licensing Site through parameters on the URL, into an HTML file for later use.

- **Viewing License Status**: See which licenses are visible to the local machine. This is a useful view for debugging licensing issues.

- **Loading Licenses Onto a Local Machine**: After a certificate license (`.lic`) or Activation fulfillment (`.xml`) file has been received, they can be placed into the appropriate location on the machine. For step-by-step instructions, see the Installing Your License key section for your license type below

- **Returning a License to Xilinx**: (Activation-based licenses only) If a license is no longer needed on a local machine, it can be returned to Xilinx and the entitlement credited back to the licensing account.

- **Viewing and Setting (Windows) License Search Locations**: Vivado tools will look in several default locations to try to find authorization to run. If your license is located elsewhere on the machine or on a floating license server, a path to that license must be specified.

RECOMMENDED: *It is recommended that the* `XILINXD_LICENSE_FILE` *environment variable be used to specify Xilinx license file locations.* `LM_LICENSE_FILE` *can also be used, but is mainly intended for non-Xilinx or legacy license path use.*

Using Xlicclientmgr Command-Line Utility

Xlicclientmgr is a command-line utility for creating Activation license requests and otherwise managing a client (node-lock) computer's trusted storage area. See the details on the Xlicsrvrmgr utility below for creating and interacting with a server (floating) computer's trusted storage area.

Xlicclientmgr can do many of the same functions the graphical Vivado License Manager utility can do, but is limited to servicing activation licenses. `Xlicclientmgr` is located in the `<Install Directory>\Vivado\2014.4\bin` directory of a Xilinx tool installation.

Key Xlicclientmgr Command-Line Flags

*   `-help all`: Prints usage information for xlicclientmgr.

*   `-v or -v "format=long"`: Displays a list or detailed list of the contents of the machine's trusted storage area.

*   `-cr <XML RequestFileName> [-r fulfillmentID]`: Creates a request in trusted storage. This is the command used to request an activation license from Xilinx. It will create an activation request in XML format, as well as an HTML file containing a URL with information for use with the Xilinx Product Licensing Site. If `–r` is used, it will create a request to return the license with the specified fulfillment ID to Xilinx.

*   `-p <responseFIleName>`: Process XML file into trusted storage. This is essentially the same command run by the **Activate License** button on Vivado License Manager's Load License screen.

*   `-returnTransaction "request=<requestFileName>" "response=<responseFileName>" "proxy=<host:port> [<proxy userId> <proxy passwd>]"`: Transmits a return request from local machine to the Xilinx Product Licensing Site.

    Note: A return request must already exist in the form of an XML file. This return request must have already been created by a previous run of `xlicclientmgr` using `–cr` and `–r` options together.

Using Xlicsrvrmgr Command-Line Utility

The Xlicsvrmgr is a command-line utility for creating Activation license requests and otherwise managing a floating license server computer's trusted storage area.For floating license generation on activation-based entitlements, the OMS website must be accessed by first running the Xlicsvrmgr utility. Vivado License Manager supports client (node-lock) activation transactions only, but floating server license requests require xlicsrvrmgr.

The Xlicsrvrmgr is contained in the License Management Tools download located at: http://www.xilinx.com/download/index.htm. The utility is also located in the `<Install Directory>\Vivado\2014.4\bin` directory of a Xilinx tool installation.

Before Running Xlicsrvrmgr The First Time

If this is the first time `xlicsrvrmgr` is to be run on a floating license server, then you will need to ensure that the computer's trusted-storage area, where activation authorizations are stored, is first installed and initialized. In the License Management Tools download, you will find an initialization utility that varies by OS. Run the commands as specified below from the `<OS><bitwidth>.o` directory where the License Manage Tools were unzipped. (For Example: `c:\servertools\win64.o\`):

- Windows:installanchorservice.exe xilinxd Xilinx-Design-Suite-Software

- Linux: `install_fnp.sh`

Key Xlicsrvrmgr Command-Line Flags

- `-help all`: Prints usage information for xlicsrvrmgr.

- `-v or -v "format=long"`: Displays a list or detailed list of the contents of the machine's trusted storage.

- `-cr <XML RequestFileName> [-r fulfillmentID]`: Creates a request in trusted storage.

  This is the command used to request an activation license from Xilinx. It will create an activation request in XML format, as well as an HTML file containing a URL with information for use with the Xilinx Product Licensing Site. If `-r` is used, it will create a request to return the license with the specified fulfillment ID to Xilinx.

  Note: If you wish to create a new activation license for a floating license server, this -cr command must be run and the URL in the resulting HTML file must be used to access the Xilinx Product Licensing Site. If you enter the product licensing site directly or through links, the Activation section of the website will be inactive.

- `-p <responseFIleName>`: Process XML file into trusted storage.

- `-returnTransaction "request=<requestFileName>" "response=<responseFileName>" "proxy=<host:port> [<proxy userId> <proxy passwd>]"`: Transmits a return request from local machine to the Xilinx Product Licensing Site.

Note: A return request must already exist in the form of an XML file. This return request must have already been created by a previous run of xlicclientmgr using `-cr` and `-r` options together.
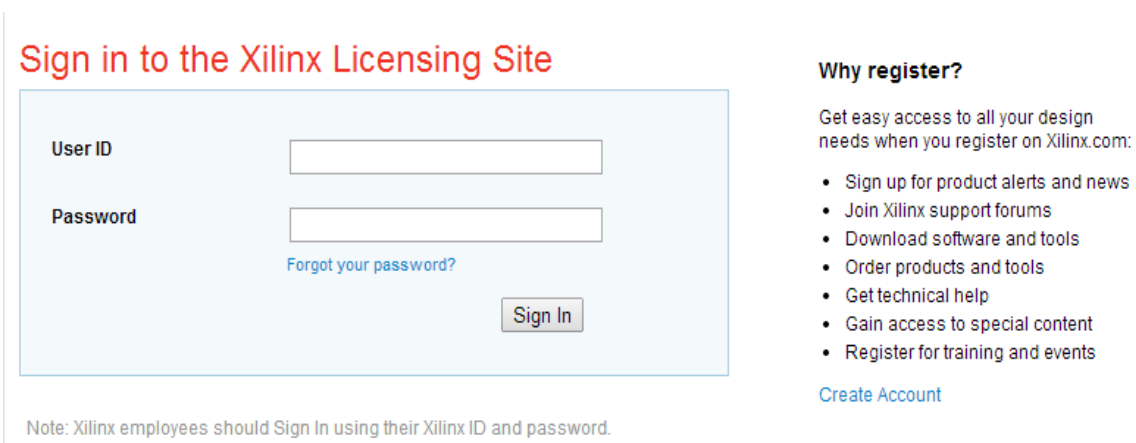
Using the Xilinx Product Licensing Site

The Xilinx Product Licensing site is where both certificate and activation-based licenses are generated, where certificate-based licenses are modified and where information about license orders reside. As mentioned earlier, creation of activation-based licenses requires

you to access the Xilinx Product Licensing Site from the Vivado License Manager or appropriate command-line utility.

You can access the Xilinx Product Licensing Site in various ways depending upon the type of license being generated.

- If you purchased products which use certificate-based licenses, follow the link included in your order confirmation email. It provides direct access to an account containing your product entitlements.

- If you purchased products which use activation-based licenses, use Vivado License Manager, xlicclientmgr or xlicsrvrmgr to generate your license request. The license request information is then sent from the Vivado License Manager or command-line tools through a URL to access the account containing your product entitlements.

- To evaluate the Vivado® Design Suite products, go to http://www.xilinx.com/products/design_tools/vivado/vivado-webpack.htm.

- To evaluate IP products, go to http://www.xilinx.com/ipcenter and follow the Evaluate link on the IP product page of interest.

- To access the Product Licensing Site directly, go to http://www.xilinx.com/getlicense. By accessing the site this way, you will not be able to create activation-based licenses, but you will be able to create certificate-based licenses as well as perform license account management functions.

    When entering the Xilinx Product Licensing Site, you must first register or enter your registration information.

Figure 5-2: **Xilinx Product Licensing Site - Sign In Page**

You must first sign in. If you already have a Xilinx user account, enter your user ID and password, and then confirm your contact information is current. If you do not have an account, click the **Create Account** button.

Send Feedback

Creating a License Key

The Create New Licenses screen on the Product Licensing Site is the starting point for license generation. The design tools and IP product entitlements you have purchased or wish to evaluate are shown in the product entitlement table.

Note: If there are entitlements in the Activation Based Licenses section of this tab, but the section is inactive, the most likely cause is that you did not enter into the Xilinx Product Licensing Site in the correct manner. In order for the Activation Based Licenses section to be active, the Product Licensing site must receive specific request and machine identification information generated by the machine on which the license is to be installed.

To generate this information:

- From a full Vivado Design Suite installation (2014.2 or later), see the instructions for Using Vivado License Manager or Using Xlicclientmgr Command-Line Utility in the Managing Licenses On Your Machine section of this chapter.

- For license servers, see the instructions for Using Xlicsrvrmgr Command-Line Utility in the Managing Licenses On Your Machine section of this chapter.

Figure 5-3: **Create New License**

Selecting Products

To begin the license generation process for products you have purchased or want to evaluate:

1. Select a product licensing account from the Account drop-down list.

   Note: This selection is not available if you are entitled to evaluation or free products only.

2. Enter product voucher codes for design tools or IP product licenses purchased with kits or for tools purchased from the Xilinx online store (optional).

3. Add evaluation or no-charge IP product entitlements to the product entitlement table (optional).

4. Make your product selections from the product entitlement table.

Entitlements are grouped into two broad categories: certificate-based or activation-based licensing. The type of product entitlements available are Full (purchased), No Charge, or Evaluation. Full and No Charge licenses have a subscription period of one year. Design tool evaluation is for 30 days and IP evaluations are for 120 days.

Floating/server and node-locked/client licenses cannot be combined in the same license file. Selecting an entitlement that contains only one license type causes the **Generate** button for the other license type to become inactive. Likewise certificate-based and activation-based entitlements cannot be generated at the same time. Selecting an entitlement in one license area causes the other license area to become inactive for the remainder of the license generation session.

For design tools, available seats represents the number of seats available for licensing over the total number of seats purchased. For IP, seats are managed according to the terms of the site wide license agreement.

Products with a status of Current are within their warranty period. Products with a status of Expired have a warranty period end date that has passed. If seats are available, licenses can be generated for either Current or Expired product entitlements.

The Vivado Design Suite: 30-Day System Edition evaluation product entitlement provides access to all the capabilities in the Vivado Design Tools. This product entitlement is automatically included in your product licensing account.

Product vouchers for design tools and IP product licenses can be shipped with a Xilinx or partner development board or design kit. If you have a product voucher card, you can enter the voucher code on the card into the associated text field and click Redeem Now. This places the corresponding design tools or IP product entitlement in the product entitlement table which you can use to generate a license key.

To add Evaluation and No Charge IP to the list of product entitlements, click the **Search Now** button in the Add Evaluation and No Charge IP Cores section of the page. This opens an IP product finder tool.
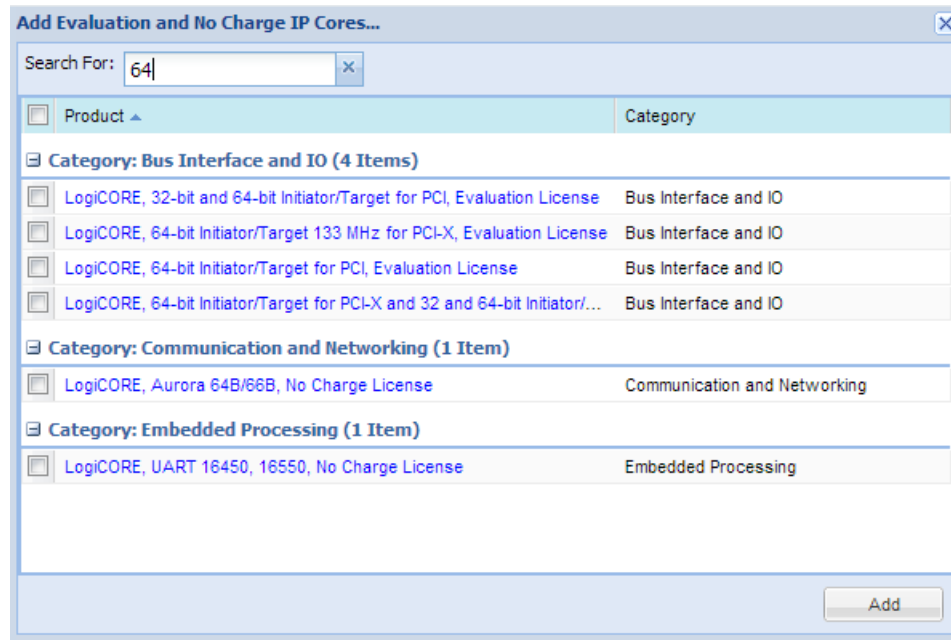
Figure 5-4: **IP Product Selector**

Generating a License

After one or more licenses are selected on the Create New Licenses page, click the **Generate License** or **Activate License** button corresponding to the type of license file you are generating (client/node-locked or server/floating). For certificate-based licenses, the license generation form shown below appears.

The step-by-step instructions below are for generating a floating certificate-based license as this process contains a superset of all other license generation flows. Exceptions for node-locked and activation-based licenses will be noted as appropriate.

Send Feedback

Figure 5-5: **Generate Floating License**

To generate a floating, certificate-based license:

1. Select the number of seats required for each product license.

   This is for server/floating licenses only. All client/node-locked licenses are for one seat. The number of seats available for a product entitlement is automatically maintained by the system. The Requested Seats field is populated, by default, with zero, although you are allowed to enter any number up to the full number of seats remaining on the product entitlement. A product is removed from the product entitlement table once all seats have been activated.

2. Enter system information.

Send Feedback

For floating certificate-based licenses, the first field is redundancy. A triple-redundant server configuration, also known as a triad, provides a fail over for the license manager software. As long as two of the three servers are running, the license manager can continue to run. This does not apply to node-locked licenses.

The system information is pre-populated in the Host ID drop-down menu if you arrived at the Product Licensing Site from a link within the Vivado License Manager. If you do not have pre-populated system information, or if you want to add a different host, select the **Add a host** option.

Figure 5-6: **Add a Host**

The Host ID value uniquely identifies the machine to which your design tools or IP is licensed. You can choose a Host ID Type to be a MAC address, a hard drive serial number or a dongle ID.

For activation-based licenses, all required system information is passed from the Vivado License Manager, or the command-line tools, via the web-browser's URL. There is no need to manually enter host information for either client or server-based activation licenses.

Note: Not all host ID types are supported for all operating systems. The easiest way to obtain your host ID is to run Vivado License Manager on the machine that serves as the license host.

3. Add a comment.

   Adding a comment to the license key file makes it easier for an administrator to track the allocation of design tools and IP product entitlements among users.

4. Click **Next**.

   The Review License Request form opens.
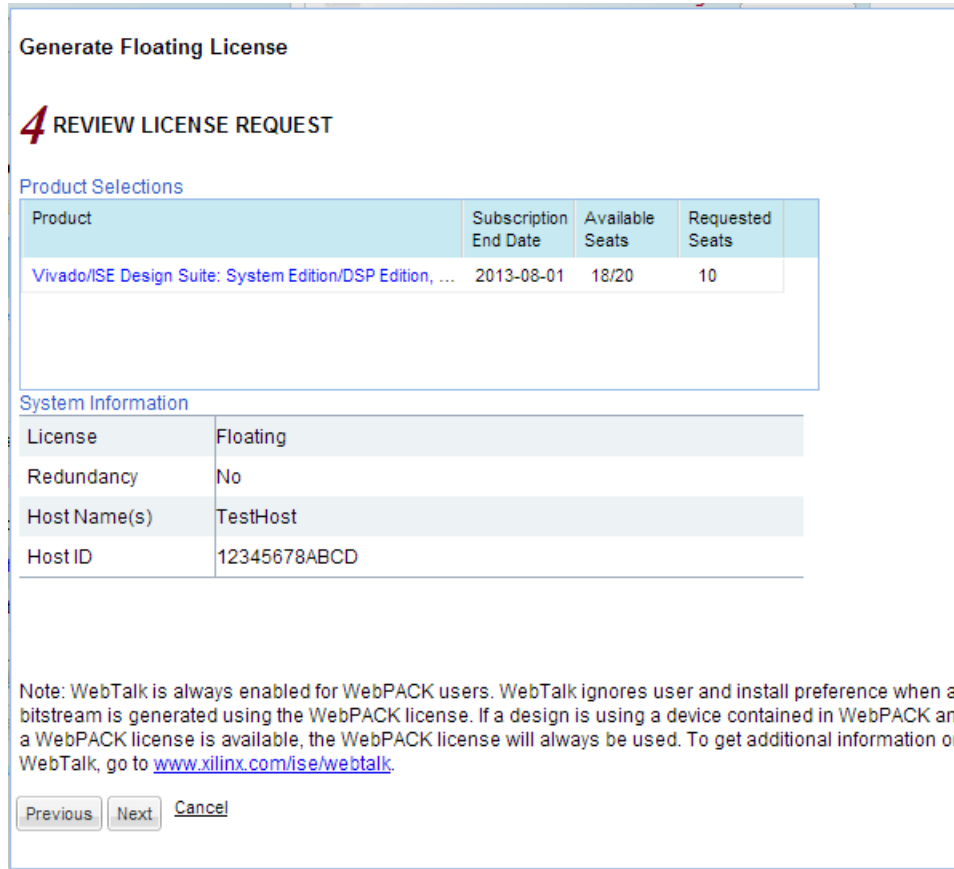
Figure 5-7: **Review License Request**

5. Review your selections.

6. If you are satisfied with your selections, click **Next**.

End-User License Agreements

Xilinx Design Tools and No Charge IP product End User License Agreements (EULAs) are agreed to during the product installation process. A complete copy of this license agreement is located at: `<install directory>/.xinstall/Vivado_2014.4/data/unified_xilinx_eulas.txt`

If you license IP products, you must accept the terms of the associated IP product EULAs before the license file can be generated.

Third-Party Licenses

A complete copy of the third-party licenses is located at: `<install_directory>/.xinstall/Vivado_2014.4/data/unified_3rd_party_eula.txt`

Send Feedback

License Generation Confirmation

When you finish generating the licenses, you will receive a confirmation message summarizing your licensing activity.
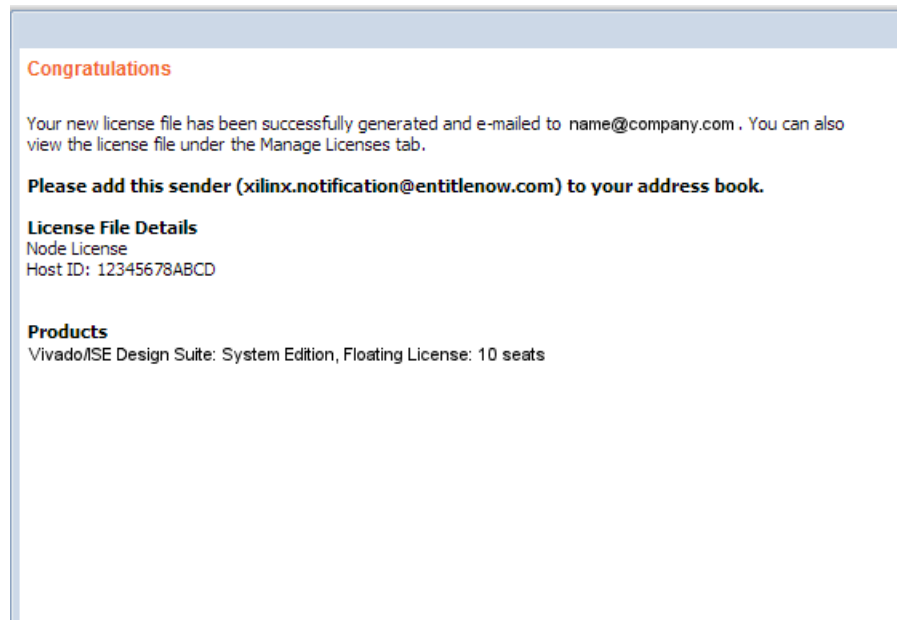
Figure 5-8:   **License Generation Confirmation**

You will also receive a license generation confirmation email. This message contains the generated license key file as an attachment. Add xilinx.notification@entitlenow.com as a trusted sender in your email address book.

If you do not receive your license by email, you can download it directly from the Xilinx Licensing Site. See the Managing Licenses on the Xilinx Product Licensing Site section for details

Installing Your License Key

The following sections describe installing different types of licenses.

Certificate-Based Node Lock or Activation-Based Client License Installation

After generating a license file, you will receive an e-mail from 'xilinx.notification@entitlenow.com'.

Send Feedback

1. Save the license file (`.lic`) or the activation fulfillment file (`.xml`) attached to the e-mail to a temporary director y on your local system.

2. Run the Vivado License Manager:

   ○ For Windows 7 or earlier: **Select Start > All Programs > Xilinx Design Tools > Vivado 2014.4 > Manage Xilinx Licenses**.

   ○ For Windows 8.1: Run the **Manage Xilinx Licenses** app from the full listing of Apps on your Start screen.

   ○ For Linux: Type vlm in a command-line shell.

3. On the left hand pane of Vivado License Manager, expand **Getting a License** and choose **Load License**.

4. If you received a certificate license (`.lic`) file, click the **Copy License** button on the Load License screen. If you received an activation license fulfillment file (.xml), click the **Activate License** button.

5. Browse to either your license file (`Xilinx.lic`) or your activation fulfillment (`Xilinx_License.xml`) and click **Open**.

6. For certificate licenses, this action copies the license file to the `<Homedrive (typically C)>:\.Xilinx (Windows)` or `<Home>/.Xilinx` directory of your computer where it will be automatically found by the Xilinx tools. For activation-based licenses, this action loads your activation fulfillment into trusted storage, where it is verified and the machine authorized for the corresponding tools.

Working with Floating Licenses

Floating License Installation on Servers

⭐ **IMPORTANT:** *In order to serve activation licenses, the xilinxd license daemon and lmgrd executable must both be at Flex version 11.11.0. Previous versions of Xilinx tools used 11.6.0, and this will not work for Activation floating licenses.*

For existing FLEXnet license servers serving certificate-based licenses, a common practice is to copy the contents of the license file, mailed from `xilinx.notification@entitlenow.com`, into the existing license file on your FLEXnet server.

For existing FLEXnet license servers serving activation-based licenses, load the license into trusted storage using the command: `xlicsrvrmgr -p <responseFIleName>`

Note: Restart the floating license server to ensure the new Xilinx licenses are enabled.

For New License Servers

1. Download the appropriate Xilinx FLEXnet license utilities for your server's operating system from the Xilinx Download Center at http://www.xilinx.com/download/index.htm.

2. Unzip these utilities into a destination directory. Xilinx recommends you place this directory into your application search path.

3. Once the FLEXnet utilities are installed, run the following commands to start the floating license server:

   - Linux

     - `<Server Tool directory>/bin` (or `bin64`)`/lin/lmgrd -c` `<path_to_license>/Xilinx.lic -l <path_to_license>/log1.log`

   - Windows

     - `< Server Tool director y>\bin\nt (or nt64)\lmgrd -c` `<path_to_license>\Xilinx.lic -l <path_to_license>\log1.log`

For activation-based licenses, the actual licenses to be served will reside in the computer's trusted storage area. However, lmgrd requires a license file in order to specify the server's hostname, port and license daemon. If you are also serving a Xilinx certificate-based license file, this .lic file will have the necessary information. If you are only serving activation-based licenses, you will need a basic license file.

To create this:

1. From a command shell containing a path to the Xilinx server tools run lmutil lmhostid

2. Choose one of the host id's produced by the previous command and create a file, perhaps called "Xilinx_Server.lic", which contains the following text:

   ```
   SERVER <host_name> <host_id> <port>
   USE_SERVER
   VENDOR xilinxd
   ```

3. For port number, the Xilinx default is 2100, although any unique port number can be used.

4. Save this license file, and use this filename in the `-c` option of the lmgrd command-line.

Client Machines Pointing to a Floating License

1. Run the Vivado License Manager (VLM).

2. Click the Manage Xilinx Licenses tab.

3. On the Manage Xilinx Licenses tab, enter the network path to the license server in the port@server format into the `XILINXD_LICENSE_FILE` field.

4. Click **Set**. The default Xilinx port number is 2100.

Send Feedback

For Linux operating systems, licensing environment variables cannot be set using the Vivado License Manager (VLM). The environment variable fields are read only, so they are grayed out and there are no **Set** buttons. The environment variable must be set using the appropriate OS shell and commands.

Managing Licenses on the Xilinx Product Licensing Site

The Xilinx Product Licensing Site tracks the licenses that you have generated. Select the Manage Licenses tab to see all licenses generated in your product licensing account.

Figure 5-9: **Manage Licenses**

Use the Manage Licenses page to perform the actions described below.

Exploring and Retrieving Your Existing Licenses

Information regarding the licenses in your product licensing account are displayed in a split-section view. Click a row in the master view in the top table, to see detailed information about the licenses in the detail view in the bottom table. The detail view table displays:

- A list of product entitlements enabled by file.

- Comments associated with the file.

The detail view table gives you the ability to:

- Download - If your license or activation fulfillment file does not arrive via email you can download it here. ⊕

- Email - Have the license or activation fulfillment file emailed to you or another user. ✉

- View - Gives you the ability to view the actual license file. 📄

- Delete (Certificate-based Licenses only) - Delete the license file. Once a file is deleted the entitlement will then become available on the Create New License page and can be regenerated for another host ID. 🗑

- View the end user license agreement (IP only).

Modifying Licenses

Activation-based licenses cannot be modified on the Xilinx Product Licensing Site. To modify an activation-based license, first use the Return License to Xilinx page in the Vivado License Manager or create a return request in the appropriate command-line license manager. Once you return an activation-based license, you'll see that the entitlement count on the Xilinx Product Licensing Site's Create New Licenses tab has been incremented by the number of seats you have returned. A new activation-based license can now be generated for a different machine, for the same machine with more seats, different features, or other changes.

To modify an existing certificated-based license, select the license file in the master view. You can modify a certificated-based license as follows:

Delete an entire license file and place entitlement back into your account

1. From the Manage Licenses Tab (see Figure 5-9), select the license file you wish to delete.

2. Click the **Delete** button 🗑 located below and to the left of the license file details.

3. Click the **Accept** button to accept the Affidavit of Destruction.

Note: This will delete all license seats in the entire license file and return the entitlements to your account.

Rehost: Change the node-locked or license server host ID for a license file

1. From the Manage Licenses Tab (see Figure 5-9), select the license file you wish to rehost.

2. Click the **Modify License** button. The Modify License screen appears.

3. Go to **System Information**.

4. Change or add new Host ID and/or Host Name by using the drop-down list and text entry boxes respectively.

5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Add additional seats to an existing licensed product entitlement

1. From the Manage Licenses Tab (see Figure 5-9), select the license file to which you wish to add seats.

2. Click the **Modify License** button. The Modify License screen appears.

3. Go to **Product Selection**.

4. For floating licenses, you will be able to change the Requested Seats field and add seats up to the total number of seats available in your entitlement.

5. Click **Next** twice. No Affidavit of Destruction is required for adding seats.

Remove seats from an existing licensed product entitlement

1. From the Manage Licenses Tab (see Figure 5-9), select the license file from which you wish to remove seats.

2. Click the **Modify License** button. The Modify License screen appears.

3. Go to **Product Selection**.

4. For floating licenses, you will be able to change the Requested Seats field and reduce the number of seats that will be authorized by this license file.

5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Add additional product entitlements to a license key file

1. From the Manage Licenses Tab (see Figure 5-9), select the license file to which you wish to add features/entitlements.

2. Click the **Modify License** button. The Modify License screen appears.

3. Go to **Product Selection**.

4. Check boxes of any new entitlements you wish to add to this license file.

5. Click **Next** twice. No Affidavit of Destruction is required for adding features.

Delete product entitlements from a license key file

1. From the Manage Licenses Tab (see Figure 5-9), select the license file to which you wish to delete features/entitlements.

2. Click the **Modify License** button. The Modify License screen appears.

Send Feedback

3. Go to **Product Selection**.

4. Check boxes of any entitlements you wish to remove from this license file.

5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Modifying a key file uses the same input form as when the license key file was created, except that additional product entitlements of the same license type (floating or node-locked) are made available for adding to the license file.

If, during any of the modification steps, you receive a message that you have exceeded your number of rehost attempts, email cs_1@xilinx.com to request additional rehost options.

Reclaiming Deleted License Components

A product entitlement is deleted when one of the following occurs:

• Changing the license server host for a license key file.

• Removing seats from an existing licensed product entitlement.

• Deleting product entitlements from a license key file.

When you delete seats or remove products from your certificate-based license files, the entitlement is essentially "put back" or reallocated into your licensing account. You will find that the number of entitled seats in the Create New Licenses tab of your account is incremented by the same number of seats you deleted previously from existing license files.

Before the reallocation of entitlement occurs, you must first agree to an Affidavit of Destruction. This legal agreement is required to ensure the deactivated product entitlements are no longer being used.

The number of allocation operations is recorded for each user. Administrators are allowed to reallocate product entitlements five times per major release. End users are allowed to reallocate product entitlements three times per major release.

What Happens to Your License Key File

Each time a license is generated for a product entitlement, a FLEXnet increment line and corresponding package line is added to the license key file. When a license key file is modified to add seats for an existing or new product entitlement, additional increment or package lines are added to the license key file.

When a license key file is rehosted or is modified to delete seats or product entitlements, the corresponding increment lines are regenerated or removed from the modified license key file.

Legacy Licensing

If you wish to obtain a license for Releases 10.1 or earlier, click the **Legacy Licensing** tab.

Figure 5-10: **Legacy Licensing**

Then complete the following steps for the respective versions:

10.1 and Prior Versions

1. Select the version you desire. You will be prompted to verify your contact information.

2. Fill out the requested form with the required information to receive your registration IDs. Your registration ID will be displayed on the screen and emailed for your records.

3. Go to the Xilinx download center, click the **Archive** link under the **Version** column on the left side of the page to select the product you desire.

4. During the download process you are prompted to insert your registration ID to complete the download process.

Your Licensing Account

Product Licensing Accounts

When you purchase a design tool edition or IP product from Xilinx, you are purchasing a license to use and receive updates for that product for one year. The license to use Xilinx deign tools and IP products is managed through the use of product entitlements. A product entitlement is the determination of:

- Which product was purchased

- The number of seats purchased

- The license type (certificate or activation-based, floating or node-locked)

- The product subscription period (product updates are provided throughout the year)

In addition to managing the product entitlements for your purchased design tools and IP, you can also access product entitlements for No Charge or Evaluation products. Full and No Charge licenses have a subscription period of one year. Design tools evaluations are for 30 days, and IP evaluations are for 120 days.

Generating a license from a product entitlement results in one or more license keys being generated by the website. When installed, the license keys enable the use of the design tools and IP that were purchased or are being evaluated. Your product entitlements and resulting license key files are managed in a product licensing account on the Xilinx website.

Product licensing accounts are specific to the individual listed on the Xilinx Software Purchase Order, who is either the end user or administrator of the design tools. All purchases made can be managed in the same product licensing account if a single administrator is named. A company site can have multiple accounts managed by different administrators. The latter is helpful if a site has multiple design teams working on differing projects with different budget pools.

Note: A license can be generated for a product entitlement that has expired; however, it only enables product releases up to the subscription end date. Applying a product update made available after the subscription end date of your license will result in a licensing error the next time the tool is used.

LogiCORE IP License Generation in the Xilinx Design Tools

Any LogiCORE™ IP and design tools entitlements you have purchased appear in your list of entitled products when you log into the Product Licensing Site. Currently, all IP entitlements will generate certificate-based licenses. Licenses for Evaluation and No Charge IP are available on the site in a separate area. Licenses for all your certificate-based design tools and IP can now be generated in one pass. They are emailed to you in a single license file.

User Types and Actions

There are three user types for the Product Licensing Site: customer account administrator, end user, and no-charge user.

Customer Account Administrator

An example of a typical customer account administrator is a CAD tools manager. Every product licensing account must have at least one customer account administrator. A customer account administrator can manage more than one product licensing account.

The responsibilities as the customer account administrator include:

* Generating node-locked or floating licenses for Xilinx design tools and IP products.

* Adding and removing users from the product licensing account.

* Assigning administrative privileges to other users.

* Ordering product DVDs (if desired).

The original customer account administrator is the Ship To contact identified during the product ordering process. That person receives an email with instructions on how to download and license each purchased product. The customer account administrator must follow the link in the email, to ensure access to the purchased products.

End User

Adding end users to a product licensing account allows an engineer or design team member the flexibility to manage and generate license keys on their own. The end user can generate license keys for node-locked products entitlements within the account as well as evaluation and "no charge" license keys for design tools and IP products. A customer account administrator can also configure the end user account to allow an end user to generate floating licenses. An end user cannot:

* View or generate floating license keys by default. This privilege can be assigned to them by the customer account administrator.

* View the license keys generated by other users.

* Add or remove other users to or from the product licensing account.

No-Charge User

No-Charge users can:

*   Generate a 30-day free evaluation license key that enables Vivado System Edition.

*   Generate a 30-day free evaluation license that enables Vivado HLS.

*   Generate license keys for evaluation and no charge IP products.

*   Generate a WebPACK™ tool license that enables WebPACK features in both ISE and Vivado.

*   Request a Xilinx Design Tools DVD package with one of the following shipping options:

    ◦   Free Shipping (2-4 Weeks)

    ◦   Standard (2-3 Days)

    ◦   Overnight

All user types can download products electronically and request a Xilinx Design Tools DVD.

Note: A customer who is already licensed for a full version of a Xilinx Design Tools product edition can evaluate other Xilinx Design Tools product editions or IP. These product entitlements are made available in the same product licensing account.

Changing Xilinx User Account Information

It is important to keep your Xilinx User Account up to date. As you change companies, addresses or emails might change.

Modifying your Corporate Email Address

1. Go to www.xilinx.com.

2. Click **Sign In**.

3. Expand **Personal Information**.

4. Enter your new corporate email address in the **Enter new Corporate email address** box.

5. Click **Save Profile** button for changes to take effect.

Understanding Your Tool and IP Orders

The Orders tab will display information regarding the purchasing orders that created the entitlements you see in this account.

Figure 5-11:   **Order Information**

• Xilinx order numbers are listed on the left panel of the screen.

• Order details populate on the right panel of the screen when you highlight specific order.

• You might only select one order at a time.

• The order's shipping address information is visible even when product is delivered electronically.

Managing User Access to Product Licensing Account

The responsibility of administering a product licensing account can be transferred or shared with another user. The ability to add or remove users from a product licensing account is managed under the Manage Users tab.
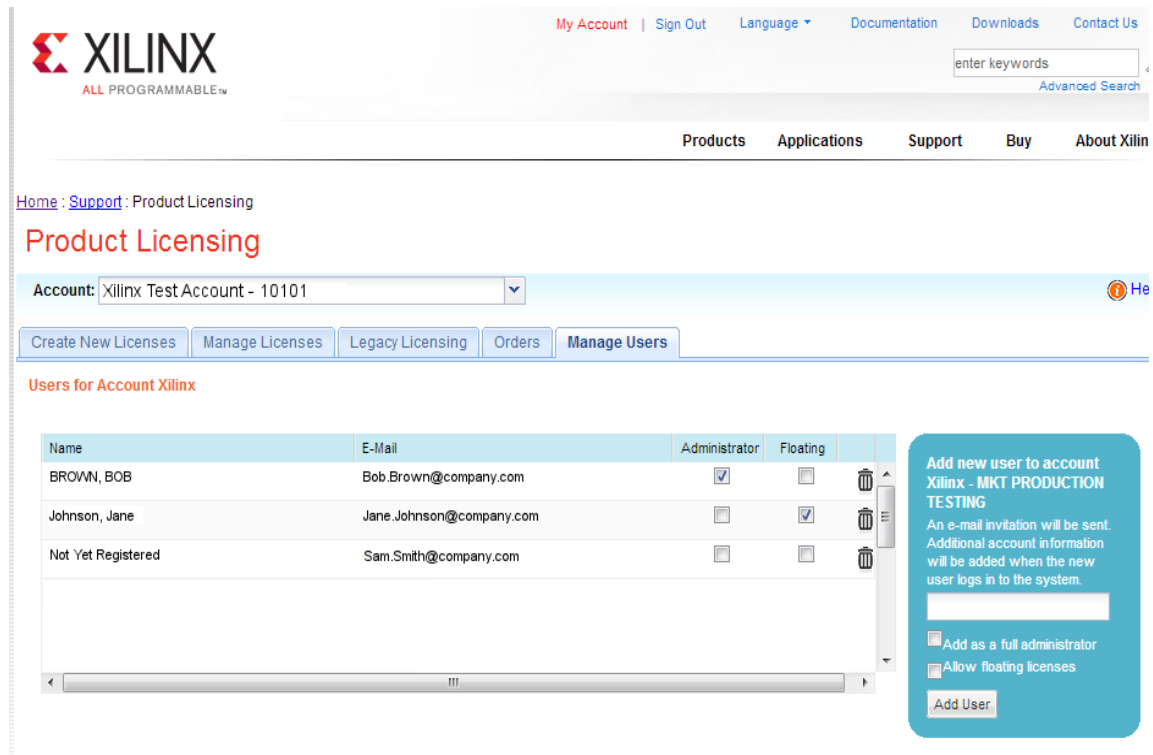
Figure 5-12: **Manage Users**

Adding Users

To add a user to your product licensing account:

• Type in the corporate email address of the new user.

• Check **Add as a full administrator**, to grant the new user customer account administrative privileges. Check **Allow Floating Licenses**, to grant the new user the ability to generate Floating Licenses, but not have full administrative privileges.

Note: The email address you provide must be the same email address the user supplied or supplies when creating their Xilinx account. If not, you might not be properly recognized when logging in.

If added users have already logged into the Product Licensing Site, their name appears in the user list. If they have never been to the site, the words Not Yet Registered appears in the space for their name. After they registered, their name is filled in.

In some instances, a customer account administrator might wish to have design team members administer license key files for their own use. By leaving both Add as full administrator and Allow Floating Licenses check boxes unchecked, you grant the user the following restricted privileges:

- User can generate node-locked license keys only.

- User can view and modify only those license key files they generated for themselves.

- User cannot manage users.

If you check Allow Floating Licenses only, the restriction on node-locked keys is lifted, but the others remain. You cannot check both boxes because it is not allowed. Full administrators already have floating license generation capability.

Removing Users

To remove administrative or floating license generation privileges from a user, uncheck the **Administrator** or **Floating** check box for that user.

To remove a user from a product licensing account, click the **Delete** button 🗑 for that user.

Send Feedback

Older Release Notes

Vivado 2014.3

What's New

Vivado® Design Suite 2014.3 features expanded support for Virtex® UltraScale™ devices including 2x faster run time. Enjoy a 20% run time improvement in the implementation phase for 7 series devices, and enhancements to Vivado IP integrator, High-Level Synthesis (HLS), Software Development Kit (SDK), and ECO flows. Enhance your embedded design productivity by following the new *UltraFast Embedded Design Methodology Guide* (UG1046) [Ref 1].

Device Support

This release introduces the public availability of the Kintex® UltraScale™ and Virtex® UltraScale™ devices.

Table 6-1: **Vivado 2014.3 Device Support**

Production Level	Vivado 2014.3 Device Support
General Access	• Kintex and Virtex® UltraScale: ◦ XCKU035, XCK U040, XCKU060, XCKU075, XCKU100, XCKU115, XCVU065, XCVU080, and XCVU095
Early Access	• Virtex UltraScale SSI devices: ◦ XCVU125, XCVU160, XCVU190 and XCVU440 • Contact Xilinx Field Application Engineer for access to these devices.
Bitstream Generation	• Bitstream generation for UltraScale devices are limited to: ◦ XCVU095 and XCKU060

Note: Part names aligned to silicon availability: XCKU040 ES1 is no longer supported and Multiple ES1 parts changed to ES2. Use the XCKU040 ES1 part along with 2014.2.

Licensing

• Virtual Machine support for Activation-based licenses

- Virtual Machines are now supported for both client and server activation licenses. If you are using a VM machine, ensure that you are using Vivado 2014.3 or later utilities to initiate license generation.

- Introducing One-Step activation licensing

  - If using **Vivado License Manager**, for client (node-locked) licenses, and connected to the internet, Vivado License Manager downloads and install activation licenses automatically.

Vivado System Edition Products

Vivado High-Level Synthesis

- Average: 10% better Fmax, 5% lower LUT utilization

- Improved QoR

  - Enhanced DSP block support.

  - Optimized control structures for loops.

  - New advanced user control for operator latency (can be used to model memory port latency).

- AXI4 interface enhancements:

  - Automatic aggregation for burst access for `m_axi`

  - Automatic byte access for improved performance for `m_axi`

  - User controllable register map for `s_axilite`

  - Support for arrays in register maps for `s_axilite`

- Improved modeling for arbitrary precision types, size information can be accessed.

- Upgraded Eclipse Environment.

- Main page is context sensitive and now directly accessible from the directive editor.

System Generator for DSP

- Enhanced Ethernet Hardware Co-simulation includes free-running clock support and board part block labeling.

- Expanded support for multiple asynchronous clock domains through metastability registers or user-defined RTL allows for a more complete system-level design.

- Improved AXI4-Stream interface handling for user-defined RTL import (Black Box).

- Improved cross-probing between your model and the Waveform Viewer enables faster debug and verification.

- Upgraded performance models for Cordic and DSP48 Macros decreases simulation run times.

- Improved caching support accelerates simulation modeling of complex IP.

- Super sample rate FIR Compiler implements gigahertz sample rate filters.

- Support for MATLAB® 2014B.

Vivado Design Edition Tools

Partial Reconfiguration

- Initial support for UltraScale devices.

  ◦ Supports implementation for KU040 and VU095 devices only.

  ◦ Bitstream generation disabled until ES2 silicon (Virtex UltraScale) or production silicon (Kintex UltraScale) is available.

- New bitstream generation features added.

  ◦ Per-frame CRC option inserts CRC values for partial bitstream integrity checking.

  ◦ Request only specific partial bitstreams with the use of `write_bitstream -cell`.

- For more information, see the *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909) and the *Vivado Design Suite Tutorial: Partial Reconfiguration* (UG947).

Vivado IP Flows

- Multiple stability improvements.

Vivado IP Integrator

- Multiple Design Assistance automations can now be run simultaneously.

  ◦ Vivado knows the correct order to run the automations.

  ◦ Fewer clicks are now required to complete a design.

- New support for directly connecting the following interfaces.

  ◦ AXI4 to AXI4-Stream

  ◦ AXI4-Lite to AXI4-Stream

- Sparse connectivity now supported.

  ◦ The memory map can be set so that some peripherals are not accessible from all masters.

  ◦ Can greatly reduce area of the required interconnect.

- Board interfaces can now be dragged and dropped directly onto the IP integrator canvas.

- **Show interface connections only** mode toolbar button added to only show interface connections to simplify the view of the design and focus on interface connections.

Vivado IP Catalog

- New options to group by taxonomy and/or repository.

- Repository management accessible by right-clicking in the IP Catalog.

- Select **Alliance Partner IP** now listed in the IP Catalog.

- All versions of custom IP show in the catalog (previously only the latest version was shown).

Vivado IP Packager

- Custom interface definition creation available through the GUI.

- Multiple ease-of-use changes to the wizard.

Vivado Physical Implementation Tools

- Placement and Routing:

  ○ Improved, faster core algorithms

    - 20% average faster 7 series run time versus 2014.2.

    - 2X faster UltraScale run time versus 2014.2.

    - Physical Optimization (`phys_opt_design`) is now multi-threaded.

  ○ UltraScale-specific improvements

    - Average 7% better Fmax for monolithic devices.

    - Average 11% better Fmax for SSIT devices.

    - Post-route Physical Optimization (`phys_opt_design`) now enabled.

    - Placer directives tuned for UltraScale, new directive **AltWLDrivenPlacement**.

  ○ Interactive routing: new option `-auto_delay` for full timing-driven routing of individual pins and nets,

- New command `report_cdc` (Tcl only) analyzes safe and unknown CDC topologies

  ○ Identifies recommended and commonly used safe topologies like single and multi-bit synchronizers, asynchronous clear/preset synchronizer, clock enable, Mux and Mux-hold CDC structures.

  ○ Other topologies reported as unknown.

- Classifies severity as a critical or warning or information type.

- Power Analysis: Final stage of re-architecting Report Power completed in 2014.3

  - 10x faster run time compared to 2013.4.

  - Over 50% less memory consumed.

  - Improved accuracy: results are on average within +/-16% of actual hardware measurements for vectorless analysis (No SAIF file input but with realistic switching activity specified for primary inputs and control signals).

  - New `report_power -type` option to specify toggle rates across output types, for example FPGA logic registers, output ports, block RAM enables, and serial transceivers.

- ECO flow using Tcl commands

  - When modifying a design with placement, it is no longer necessary to unplace cells before connecting them using the `connect_net` command. This restriction prevented potentially illegal connections or illegal placement. In 2014.3, after a design is modified, DRC automatically detects illegal conditions and prevents continuation of the design flow.

- `report_design_analysis` (Tcl only) adds insight into timing closure issues

  - Use `-timing` option for analysis of physical characteristics of timing paths.

  - Use `-complexity` for design complexity metrics of top design or submodules.

- `report_synchronizer_mtbf` (Tcl only, UltraScale only)

  - MTBF calculations for individual CDC synchronizer circuits.

  - Provides overall MTBF and guidance when MTBF cannot be calculated.

Static Timing Analysis

- Run time improvement of 2x in 2014.3 versus 2014.2.

- Saved Timing Summary Improves Run time:

  - Timing summary reports can now be saved and restored using `.rpx` files.

  - `report_timing_summary` can use the restored report instead of running again.

  - `rpx` reports are static – they do not update to reflect the in-memory design.

  - Other reports support the `rpx` format in the 2015.x release and future releases.

- Saving and Restoring Timing Reports:

  - Project-based flow

    - Implemented timing summary report automatically saved.

    - Opening the implemented design restores the timing summary.

Send Feedback

- Scripted flow

    - Generate an `.rpx` file using the `-rpx` flag:
      `report_timing_summary -delay_type min_max -max_paths 10 -input_pins -name timing_1 -rpx  timing_1.rpx.`

    - Use **File >Open Interactive Report** to restore timing results in the Vivado Integrated Design Environment (IDE).

- Timing Constraints wizard:

    ◦ New **Back** button removes constraints from the in-memory design

    ◦ User data persists

    ◦ Invalid constraints are properly restored to their initial state

RTL Synthesis

- Multicore support on Linux for 25% faster synthesis run time on average.

- Two new built-in strategy options:

    ◦ Area reduction with 10% less LUTs on average.

    ◦ Performance optimization with 3-4% better Fmax on average.

- Beta support for VHDL 2008 (see details in answer record <u>Answer Record 62005</u>.)

- New default value `auto` for `control_set_opt_threshold`.

- Improved automatic finite state machine (FSM) encoding selection.

- New inference patterns for DSP block inference.

- New attributes to control clock enable and synchronous resets (`direct_enable` and `direct_reset`).

- New automatic cascade chain pipelining for UltraScale BRAMs.

- Better handling of `MARK_DEBUG` across levels of hierarchy.

Vivado Debug

- Debug Probe renaming at run time

    ◦ Rename probes on multiple ILA/VIO cores.

    ◦ Names persist in waveform window.

    ◦ Ability to view original probe names.

- Improvements to Setup Debug wizard

    ◦ New find for nets to debug.

    ◦ Aligns with the standard Vivado Find dialog box.

- MARK_DEBUG and DONT_TOUCH can be decoupled in implemented design

- Persistence of Hardware Manager settings

- Improved hardware connection

  ◦ Auto Connect to local target.

  ◦ Not dependent on vcse_server.

  ◦ New open hardware target flow.

Vivado Device Programmer

- Flash Programming

  ◦ Erase, blank check, programming and verify.

- Battery-backed block RAM for encryption key

- eFUSE programming and readback

  ◦ Encryption key

  ◦ User bits

  ◦ Device DNA

- FPGA readback and verify

Vivado Simulator

- New Waveform Database

  ◦ Lower memory and disk footprint

  ◦ Faster tracing

  ◦ Cross-platform support

  ◦ Version migration

  ◦ Fault tolerant

- Simulation run time reduction (average of 1.5X) and memory usage reduction (average of 2X)

- SystemVerilog Direct Programming Interface (DPI)

  ◦ Enables SystemVerilog to interface with C (similar to PLI in Verilog).

SDK

- Create Bootgen command now includes edit mode.

- SDK includes support for new hardware handoff file (`*.hdf`) as well as the existing XML format.

- New format to support Linux application creation through the sysroot of the Linux file system, and an option to provide a selected tool chain.

- See the What's New in SDK topic in the 2014.3 SDK Help for more information on what's new in SDK.

Important Information

Updates to Existing IP

The following table lists current updates to existing IP for the 2014.3 release.

Table 6-2: **Existing IP Updates**

Existing IP	Existing IP Updates
10G Ethernet MAC	• New optional 32-bit low latency and size reduced IP • Added Zynq®-7000 AP Soc and 7 series defense grade devices
AXI 10G Ethernet MAC	• 10G Ethernet MAC and 10GBASE-KR or 10GBASE-R • Available in IP Integrator and IP Catalog • Added UltraScale Kintex® device support • Added Zynq-7000 AP Soc and 7 series defense grade devices
10GBASE-R	• New optional 32-bit low latency and size reduced IP • Added Zynq-7000 AP Soc and 7 series defense grade devices
AXI Ethernet Subsystem	• Added optional non processor mode (No AXI Buffer) • Available in IP Integrator and IP Catalog • TEMAC + 1000BASE-X with optional hardware timestamping for UltraScale Kintex® and 7 series
PCI Express®	• AXI-MM support for Gen3 PCI Express hard block (Virtex7 XT/HT). • Package Migration section in User Guide for UltraScale FPGA devices. • Tandem PCIe/PROM support (Beta) for UltraScale FPGA devices.
Aurora	• Additional UltraScale FPGA device support. • Simulation support with Labtools enabled. • AXI4-Lite to DRP interface compliance (Aurora 64b66b).

Note: Part names aligned to silicon availability: XCKU040 ES1 is no longer supported and Multiple ES1 parts changed to ES2.

Implementation Tools

Limitations involving register mapping to UltraScale SSIT Laguna (SSI Technology for 3-D ICs) registers:

- Automatic placement of registers into Laguna registers is not yet supported. Manual placement can be achieved by assigning registers to appropriate LOCs and BELs within Laguna tiles. Drag-and-drop placement is supported in the IDE.

- A Laguna **TX_REG** register cannot directly drive a Laguna **RX_REG** register across an SLR boundary as it might create a hold time violation that cannot be fixed by the tools. This restriction might be relaxed in the future for certain situations but in 2014.3 it results in a `place_design` error.

Known issues using `report_synchronizer_mtbf`:

- You might encounter an issue when you use **XDC** to set **ASYNC_REG** instead of HDL attributes. After a design or design checkpoint is saved and re-opened, the `report_synchronizer_mtbf` fails as the tools cannot locate the synchronizers specified using **XDC ASYNC_REG** properties. Instead, you must run `report_synchronizer_mtbf` in the same run before saving the checkpoint. If using a project flow, add a tcl.post script to run `report_synchronizer_mtbf` after the route_design step. This limitation will be fixed in a future release. Synchronizers specified using **ASYNC_REG** in HDL are not affected.

- The command does not detect invalid **MTBF** in the case where there is a timing violation from the final **ASYNC_REG** synchronizer stage. This issue will be fixed in a later release.

Documentation Navigator

- New integrated **Web Search Results** tab that searches for documents on Xilinx Support.

- Support for Design Hubs in the main Catalog View.
  - Guided learning curve with recommended key concepts and FAQs.

- New **Send Feedback** link added to each Design Hub.

Vivado Design Suite Documentation Update

In the 2014.3 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2014.3 documentation suite.

Licensing

Activation licensing is not supported for USB dongles, on floating servers running SOLARIS OS, or on triple-redundant server configurations.

IP Known Issues and Change List

• For Xilinx IP known issues, see the *IP Release Notes Guide* (XTP025) [Ref 7].

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 59464

Vivado 2014.2

What's New

Vivado® Design Suite 2014.2 features new device support across multiple tools, as well as several tool enhancements.

Device Support

This release introduces the public availability of the Kintex® UltraScale™ devices.

Table 6-3: **Vivado 2014.2 Device Support**

Production Level	Vivado 2014.2 Device Support
Production Ready	• Defense Grade Artix®-7Q: ◦ XQ7A50T • Defense Grade Zynq®-7000 AP Soc: ◦ XQ7Z045 + RF900 Package • XA Zynq®-7000 AP Soc: ◦ XA7Z030 + FBG484 Package
General Access	• Virtex® UltraScale: ◦ XCVU065, XCVU080, XCVU095 and XCVU125
Early Access	• Kintex UltraScale SSI devices: ◦ XCKU100 and XCKU115 • Virtex UltraScale devices: ◦ XCVU160 and XCVU440 • Contact Xilinx Field Application Engineer for access to these devices.

Vivado System Edition Products

System Generator for DSP

- Improved simulation performance.

  ◦ Waveform Viewer conversion times shortened up to 90%.

  ◦ Opens System Generator blocks 50% faster.

  ◦ Decreased simulation initialization times by up to 80% for models with multiple FFTs and other complex IP.

  ◦ New fast MCode model improves performance of MultAdd by over 90%.

- Updated WinPCap to 4.1.3 for Ethernet Hardware Co-Simulation support in Windows 8.1.

- Better support for Linux with improved library compatibility See Answer Record 59236.

- Blockset Features:

  ◦ Reduction operator supported on Logical block when single input is selected.

  ◦ Ability to configure LFSR block as maximal length code generator.

Vivado Design Edition Tools

Partial Reconfiguration

- Partial Reconfiguration has extended device support to include the two smallest Artix-7 devices: 7A50T and 7A35T. All 7 series and Zynq SoC devices are now supported.

- For more information, see the *Vivado Design Suite User Guide: Partial Reconfiguration (UG909)* and the *Vivado Design Suite Tutorial: Partial Reconfiguration (UG947)*.

Tandem Configuration for Xilinx PCIe IP

- Support for the Zynq SoC 7Z100 device has been added.

- For more information, see the PCI Express IP Product Guides – PG054 for Gen2 PCIe IP or PG023 for Gen3 PCIe IP.

Vivado IP Flows

- Multiple stability improvements.

Vivado IP Integrator

- A number of DRCs that were run during generation have been moved into the `validate_bd_design` step to catch these issues earlier in the flow.

- Multiple stability improvements.

Send Feedback

Vivado Physical Implementation Tools

- To improve runtime, the default behavior of placer and router timing summary has changed. In 2013.4, both the placer and router reported a timing summary in the log with WNS based on signoff timing from the static timing engine. Beginning with the 2014.2 release, the placer and router no longer report signoff timing by default. You must ensure that `report_timing_summary` is run after `route_design` to generate the signoff timing results.

- Specific Improvements:

  ◦ The placer reports an estimated timing summary.

  ◦ The router reports a timing summary with estimated WNS which might be more pessimistic than actual timing. So it is possible for the router WNS to be negative while the actual WNS is positive. You must check the actual signoff timing using `report_timing_summary`.

  ◦ If the router reports estimated WNS that is negative, the message is a warning, not a critical warning.

  ◦ To restore 2013.4 and prior command behavior (signoff WNS reported) you can specify the `-timing_summary` option for `place_design` and `route_design`.

  ◦ Implementation runs in Vivado projects should see little impact due to these changes because the timing summary report is still generated after routing. The `report_timing_summary` command generates a critical warning message if signoff timing is violated.

Static Timing Analysis

- 25% runtime improvement for `report_timing_summary` and `check_timing`.

SDK

- Create Bootgen command now includes edit mode.

- WebTalk is now integrated in the Vivado Design Suite plus the SDK package, standalone SDK will be supported by WebTalk in a future release.

- SDK includes support for new hardware handoff file (`*.hdf`) as well as the existing XML format.

- New format to support Linux application creation through the sysroot of the Linux file system, and an option to provide a selected tool chain.

- See the 2014.2 Help Contents for more information on What's new in SDK at: http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/SDK_Doc/index.html.

Send Feedback

Important Information

Windows XP Support

For Vivado 2014.2, Windows XP is supported. However, beginning with the Vivado 2014.3 release, Windows XP will no longer be supported. This is due, in large part, to Microsoft's termination of Windows XP support on April 8, 2014.

Vivado Design Suite Documentation Update

In the 2014.2 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2014.2 documentation suite.

IP Known Issues and Change List

• For Xilinx IP known issues, see the *IP Release Notes Guide (XTP025)* [Ref 7].

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 59464

Vivado 2014.1

What's New

Vivado® Design Suite 2014.1 increases your productivity with faster runtimes, improved quality of results, automation of the UltraFast Design Methodology, and hardware acceleration of OpenCL kernels through Vivado High-Level Synthesis (HLS).

Device Support

This release introduces the public availability of the Kintex® UltraScale™ devices.

Table 6-4: **Vivado 2014.1 Device Support**

Production Level	Vivado 2014.1 Device Support

Production Ready	• Artix®-7:
	  ◦ XC7A35T and XC7A50T
	• XA Artix®-7:
	  ◦ XA7A50T, XA7A35T, and XA7A75T
	• Zynq®-7000 AP Soc:
	• XC7Z015

General Access	• Kintex® UltraScale: ◦ XCKU035, XCKU040, XCKU060, and XCKU075

Early Access	• Kintex UltraScale SSI devices:
	  ◦ XCKU100 and XCKU115
	• Virtex UltraScale devices:
	  ◦ XCVU065, XCVU080, XCVU095, XCVU125, and XCVU160
	• Contact a Xilinx Field Application Engineer for access to these devices.

Xilinx Tcl Store

Xilinx is taking another large step forward in designer productivity by hosting an open-source repository for sharing Tool Command Language (Tcl) scripts. The Xilinx Tcl Store makes it easy to find and share Tcl scripts contributed by the development community. With the power of Tcl, these scripts extend the core functionality of the Vivado Design Suite, further enhancing productivity and ease of use. All of the Tcl code published in the repository is free and redistributable under a BSD based open source license model.

The Xilinx Tcl store is accessed directly from the Vivado Integrated Design Environment (IDE), the Tcl Store enables users to select and install collections of Tcl scripts called apps directly from within the tool. After installed, these apps appear like built-in Vivado commands, right down to the help infrastructure. Vivado supports different versions of apps using standard package facilities of Tcl, so if a newer version is released you can choose to upgrade with a single mouse click.

The Xilinx Tcl Store is intended to make it easier to find and use well-crafted Tcl scripts developed and supported by the user community, much like Linux. Tcl scripting is a little more advanced than selecting IDE buttons. However, it is easy to learn. Documentation and user guides provide details on specific commands from the Tcl API and can be found on www.xilinx.com/support.

Licensing

For new purchases of the Vivado Licenses beginning in 2014.1, Vivado Licenses use an activation-based licensing scheme. Activation-based licensing offers robust security and return features, as well as pave the way for future licensing enhancements. See Obtaining and Managing a License chapter for more detailed licensing information.

Project Infrastructure

- Improved revision control support by allowing a standalone project .xpr file that was checked into source control to recreate the project.

- Improved constraint management of xdc files – so that constraints such as physical and configuration constraints will not make synthesis runs go out of date.

- Added regular expression support for message suppression Tcl commands.

- Discontinued support for Xilinx Platform Studio (XPS) integration with Vivado.

Vivado System Edition Products

Vivado High-Level Synthesis

- Enhanced support for AXI4, master and slave Lite interface can now be specified directly using the INTERFACE directive.

- QoR (quality of results) improvements with automatic loop pipelining and associative-math operations for floating-point calculations.

- New linear algebra library for matrix operations.

- Reduced disk space requirements for C/RTL cosimulation.

- Vivado® simulator is now default for C/RTL cosimulation.

System Generator for DSP

- Enhanced functionality with support for multiple clocks and asynchronous clock domain crossing.

- Faster analysis with cross-probing between MATLAB® variables and the Wavescope signal viewer.

- Improved Hardware cosimulation capabilities with Ethernet point-to-point support for VC707 and KC705 boards.

- Support for MATLAB 2014.a.

  ◦ See Answer Record 59236 for important installation information.

Vivado Design Edition Tools

Partial Reconfiguration

- Partial Reconfiguration has extended device support to include the following:

  ◦ All Virtex®-7 HT devices (7VH870T and 7VX580T)

  ◦ All Zynq® SoC devices (adding the 7Z100 and 7Z015)

  ◦ Three Artix®-7 devices (7A200T, 7A100T and 7A75T)

- Native encryption support for partial bit files is now available.

- Floorplanning capabilities have been enhanced to automatically consider partial reconfiguration design rules. Pblocks can be set to snap to legal reconfigurable boundaries by setting the SNAPPING_MODE property.

- For more information, see the *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909) and the *Vivado Design Suite Tutorial: Partial Reconfiguration* (UG947).

Tandem Configuration for Xilinx PCIe IP

Tandem Configuration is the Xilinx solution for fast configuration of PCIe® designs to meet enumeration needs within open PCIe systems. New features in 2014.1 include:

- Support for Zynq SoC devices

  ◦ Tandem PROM is the only supported variant

  ◦ 7Z045 and 7Z030 devices supported

- Four additional devices have moved to production status

  ◦ 7K420T

  ◦ 7VX330T

  ◦ 7VX415T

  ◦ 7VX980T

- The Tandem Configuration IP core has been included within the IP Integrator. This core, which is specifically the AXI streaming variant, can be added to a design within IP integrator.

- For more information, see the PCI® Express IP Product Guides – PG054 for Gen2 PCIe IP, or PG023 for Gen3 PCIe IP.

Send Feedback

Integrated Design Environment (IDE)

- Redesigned Getting Started Page.

    - Direct access to recent projects and checkpoints.

    - Added links to Open Hardware Manager and Xilinx Tcl Store.

- Timing Constraints wizard: An automated tool that guides users to create timing constraints for clocks, I/O and clock domain crossing constraints.

- Integrated support for submitting runs to load sharing server management software using LSF (linux only).

- Schematic magnify function shows bit level details of bus connections.

- Simplified the icons in hierarchial sources view (HSV) to improve clarity of source types.

- New `updatemem` command for block RAM initialization for UltraScale MicroBlaze™ based designs.

Vivado IP Flows

- LSF Support on Linux:

    - For improved run time, Linux users can now leverage LSF (Load Sharing Facility) to execute multiple Out Of Context (OOC) runs in parallel on multiple machines

- Create and Package IP Flows:

    - Simplified IP packager summary

    - Automated generation of IP customization TCL

    - Duplicate IP detection in the IP catalog

    - Unified display of ports and interfaces

    - Enhanced Parameter Handling

        - Clear differentiation of Visible versus Hidden parameters

        - Ability to create customization only parameters

    - IP Customization

        - Presentation and layout control

        - Page naming support

        - Explicit control of widgets

    - Create Peripheral wizard

        - Interrupt support added

- Improved BFM demonstration design

- Added JTAG2AXI based demonstration design

Vivado IP Integrator

• New "Signals" tab allows drag and drop connection, visualization and management of clock and reset domains in a design.

  ◦ Groups of clocks and/or resets can be connected at one time

  ◦ Enables easier visualization of designs with multiple clock domains

• New automated board interface tab allowing quick connection to interfaces available on supported development boards.

• Remote locations are now supported when creating and managing a BD source.

• Designer Assistance now provides an option for users to specify a clock domain instead of assuming a default domain.

• During an IP upgrade, IP Integrator now knows when IP port/interface names have changed and will automatically connect changed port/interface names instead of issuing a critical warning as in Vivado 2013.4.

• In 2014.1, the Concat IP block was upgraded from V1.0 to V2.0.

  ◦ Version 1.0 of the xlconcat block reverses the order from input to output

  ◦ Version 2.0 preserves the order of input signals on the output

    Note: Upgrading from V1.0 to V2.0 will re-wire input connections to preserve the overall the signal order on the output

• Connected pins on symbols can be hidden to simplify a diagram. The options is available on the "Layers" tab of "Block Design Options".

• Designer Assistance now automatically creates unique Processor System Reset blocks for each clock domain to ensure the reset is synchronized to the clock.

• Multiple blocks have new symbols in IP Integrator to make the diagrams easier to understand.

• Access is now available to clock multiply and divide values for various PLLs in the Zynq® PS providing better control and flexibility for users

Vivado Physical Implementation Tools

• Performance and Run Time improvements.

  ◦ Average 5% better Fmax across all device families.

  ◦ Average 25% faster overall Implementation run time compared to 2013.4.

Send Feedback

- ◦ Placer and router multithreading now can use up to 8 CPUs.

- ◦ Average 2.5% better Fmax on 7 Series FPGAs SSIT devices.

- Physical Optimization (phys_opt_design) can now be run after routing for 7 series FPGA device targets for "last-mile" timing closure. See *Vivado Design Suite User Guide: Implementation* (UG904) for more details.

- Three new Implementation Strategies added:

  - ◦ Performance_ExplorePostRoutePhysOpt (adds Post-Route phys_opt_design to Performance_Explore).

  - ◦ Flow_RunPostRoutePhysOpt (adds Post-Route phys_opt_design to FlowRunPhysOpt).

  - ◦ Performance_Retiming (more aggressive replication and retiming).

    Note: Placer directives are currently not supported for UltraScale.

- The route_design -re_entrant options to enable and disable interactive routing have been deprecated. The mode of operation, either normal or interactive is handled automatically by the router.

- New reporting command report_ram_utilization to report details of logical resources used to implement memory arrays.

- LUTs paired using LUTNM, HLUTNM, and SOFT_HLUTNM can be uncombined after synthesis.

- opt_design: New directive NoBramPowerOpt for skipping block RAM Power optimization during opt_design.

- To improve run time, the default behavior of placer and router timing summary has changed. In 2013.4, both the placer and router reported a timing summary with WNS in the log. In 2014, the report_timing_summary command reports the timing summary message for projects. The message is still a critical warning when timing is not met.

  - ◦ The placer reports a timing summary based on its internal timing estimates rather than calling the static timing engine.

  - ◦ The router also reports a timing summary based on its internal timing estimates which might be more pessimistic than actual timing. So it is possible for the router WNS to be negative while the actual WNS is positive. You must check the actual timing using report_timing or report_timing_summary.

  - ◦ To restore 2013.4 command behavior where the static timing engine is used for reporting the timing summary, you must specify the -timing_summary option for place_design and route_design.

Send Feedback

Static Timing Analysis

- Timing Constraints wizard: An automated tool that guides users to create timing constraints for clocks, I/O and CDC.

- Enhancements:

  ○ check_timing: Issues classified as high, medium and info only for ease of use to enable you to focus on fixing only high and medium issues.

  ○ Three new Timing DRC's added.

    - Detecting combinatorial loops.

    - Detecting overridden set_max_delay -datapath_only constraints.

    - Detecting invalid generated clock waveform on gigabit transceiver (GT).

- A new option '-summary' has been added to report_exceptions command that will generate a table with the total of exceptions and the total number of endpoints covered for setup, hold and minimum pulse width checks.

RTL Synthesis

- Enhanced safe state implementation for finite state machines with both error detection and correction (using Hamming encoding)

- Support for asymmetric read and write port bit width RAM inference (can be mapped onto multiple blocks)

- Quality of results improvements with area optimization taking into account levels of logic, new XOR, ternary adders and large equality comparator optimizations

- DSP inference improvements with support for substracter in pre-adder to enable complex multiplier inference

- Inferred XORs can be mapped onto UltraScale DSP48 blocks

- New global options max_bram and max_dsp to control number of block inferred

- New clock_buffer_type and io_buffer_type attributes

- New methodology DRCs message

Vivado Debug

- ILA core QoR improvements: Basic and advanced triggering supports 300+ MHz

- Multiple windows in waveform

- Repetitive triggering

- Trigger state machine syntax check

- Reduced run time for debug cores

Send Feedback

- Analog data display for System Monitor

- Ease of Use Improvements

  ◦ Clock divider control for debug hub

  ◦ Improved create debug core wizard

  ◦ Create debug wizard in Flow Nav

Vivado Programmer

- Flash creation and indirect programming capabilities

- 1.7x faster SPI programming compared to iMPACT

- 1.9x faster BPI programming compared to iMPACT

- New Tcl command (calc_config_time) to estimate configuration time

- Remote hardware server standalone installation

SDK

- The Target Connection Feature is implemented for any connections to the board. This includes the following additional changes:

  ◦ The Configure JTAG Settings feature is deprecated.

  ◦ All features such as Program FPGA and Debug Launch now include the Target Connection.

- The SDK log is now visible in the main interface.

- A new Performance Analysis feature is implemented. You can use this to display ARM®performance and AXI performance in both tabular and visual modes.

- New Regenerate BSP Sources feature allows you to regenerate the BSP on demand. Previously the BSP was automatically generated; now you can choose to regenerate it.

Important Information

Updates to Existing IP

Table 6-5, page 81 lists current Existing IP Updates for the 2014.1 release.

Table 6-5: **Existing IP Updates**

Existing IP	Existing IP Updates
10G Ethernet MAC	• Added Priority Flow Control(PFC) • Reduced CRC Latency • Added UltraScale Kintex® device support
AXI 10G Ethernet MAC	• Added Priority Flow Control(PFC) • Reduced CRC latency • Added 1588 hardware timestamping transparent clock support
Tri-mode Ethernet MAC	• Added Priority Flow Control(PFC) • Added UltraScale Kintex® device support
1000BASE-X/SGMII	• Added UltraScale Kintex® device support
AXI Ethernet	• Added 1588 hardware timestamping transparent clock support • Added UltraScale Kintex® device support
PCI Express	• UltraScale Kintex public access • All widths/speeds supported • Root Port enabled • IP integrator support
Aurora	• UltraScale Kintex support • IP integrator support

Vivado Design Suite Documentation Update

In the 2014.1 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. These documents will be available in the first few weeks after the release. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2014.1 documentation suite.

IP Known Issues and Change List

• For Xilinx IP known issues, see the *IP Release Notes Guide (XTP025)* [Ref 7].

• For a detailed change list of Xilinx IP Cores in 2014.1, see Answer Record 59464.

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 55120

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Xilinx Documentation Navigator

You can view Xilinx tool and hardware documentation in the Xilinx Documentation Navigator or on the Xilinx website. The Documentation Navigator is integrated with the Vivado® Design Suite and it provides a catalog of Xilinx documentation and videos.

For more information about the Documentation Navigator, see the *Vivado Design Suite User Guide: Getting Started* (UG910).

Licenses and End User License Agreements

The third-party licenses govern the use of certain third-party technology included in and/or distributed in connection with the Xilinx design tools. Each license applies only to the applicable technology expressly governed by such license and not to any other technology. You must accept the terms of the End User License Agreements (EULAs) for Xilinx design tools and third-party products before license files can be generated.

To view the third-party license details and EULA, see http://www.xilinx.com/cgi-bin/docs/rdoc?v=2014.4;d=ug763_tplg.pdf.

To view the Xilinx design tools license details and EULA, see
http://www.xilinx.com/cgi-bin/docs/rdoc?v=2014.4;d=end-user-license-agreement.pdf.

References

1. *UltraFast Embedded Design Methodology Guide* (UG1046)

2. *Vivado Design Suite User Guide: Logic Simulation* (UG900)

3. *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909)

4. *Vivado Design Suite Tutorial: Partial Reconfiguration* (UG947)

5. *Vivado Design Suite User Guide: Hierarchical Design* (UG905)

6. *Vivado Design Suite Tutorial: Hierarchical Design* (UG946)

7. *IP Release Notes Guide* (XTP025)

8. *USB Cable Installation Guide* (UG344)

9. *Platform Cable USB II Data Sheet* (DS593)

10. *Parallel Cable IV Data Sheet* (DS097)

11. Xilinx Download Center (http://www.xilinx.com/support/download/index.htm)

12. Xilinx Design Tools WebTalk page (http://www.origin.xilinx.com/ise/webtalk/)

13. *Vivado Design Suite Video Tutorials* (www.xilinx.com/training/vivado/index.htm)

14. *Vivado Design Suite Documentation*
    (www.xilinx.com/support/documentation/dt_vivado2014-4.htm)

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