# Vivado Design Suite User Guide

## *Release Notes, Installation, and Licensing*

**UG973 (v2013.2) June 19, 2013**

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# Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 06/19/2013 | 2013.2 | Added details to the Release Notes 2013.2 in Chapter 1, and Older Release Notes in Chapter 6. |
| 04/15/2013 | 2013.1 | Added details to Vivado XDC Changes in Chapter 1, and noted the use of Vivado synthesis for Xilinx IP in Compatible Third-Party Tools in Chapter 2. |
| 03/20/2013 | 2013.1 | Initial Xilinx release. |

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*Chapter 1*

# Release Notes 2013.2

## What's New

Vivado® Design Suite 2013.2 accelerates both time to integration and system-level design. System-level designers benefit from public access to the Vivado IP Integrator a device and platform aware interactive, graphical environment that provides IP-aware automated IP subsystem generation. Vivado High Level Synthesis and System Generator for DSP are now also integrated into Vivado IP integrator providing a comprehensive development environment for All Programmable FPGA and SoCs. Also, get through your integration work faster with improved run-times and new end-to-end debug capabilities.

### Device Support

The following devices are production ready:

- Zynq®-7000 devices
  - 7Z010, 7Z020, and 7Z100
- Defense Grade Zynq-7000Q
  - 7Z010, 7Z020, and 7Z030
- Defense-Grade Virtex®-7Q
  - VX690T and VX980T
- Defense-Grade Artix-7Q
  - A100T and A200T
- XA Artix®-7
  - A100T

# Vivado System Edition Products

## Vivado High-Level Synthesis

- Video libraries with OpenCV interfaces are enhanced with support for 12 additional functions.
  - hls::CornerHarris, hls::EqualizeHist, hls::FASTX, hls::GaussianBlur, hls::Harris
  - hls::HoughLines2, hls::Integral, hls::InitUndistortRectifyMap, hls::PaintMask
  - hls::Remap, hls::Resize, hls::Sobel
- Adders can now be targeted for implementation in a DSP48 directly from Vivado HLS.
  - Previously, the implementation of adders or subtractors in a DSP48 was left to RTL Synthesis. With the new core AddSub_DSP users can now specify, inside Vivado HLS, that the addition or subtraction be performed using a DSP48.
- The Xilinx FFT core can now be instantiated directly into the C/C++ source code. This feature is Beta. Contact your local Xilinx FAE for details on how to use this feature.

## System Generator for DSP

- Tools Integration
  - Introducing Vivado® IP Integrator support in System Generator for DSP.
    - Model packaged as an IP with support for gateway inputs and outputs to be packaged as interfaces or raw ports.
    - Capability to specify AXI4-Stream interface in Gateway blocks and to infer AXI4-Lite and AXI4-Stream interfaces from named Gateway blocks.
    - System Generator generates example RTL Vivado project and example IP Integrator block diagram to enable easy evaluation of packaged IP.
    - New System Generator IP Integrator integration tutorial available with System Generator tutorials.
  - Introducing support for MATLAB® and Simulink® release R2013a.
- Blockset Enhancements
  - Support added for FIR Compiler v7.1 with introduction of area, speed and custom optimization options.
  - Model upgrade flow now includes port and parameter checks to the HTML report.
  - Enhanced caching to speedup subsequent model compilation.

# Vivado Design Edition Tools

## Interactive Design Environment

- View file compile order in the Sources Compile Order tab
  - Select between Synthesis, Implementation, and Simulation
  - Reflects file order from report_compile_order command
- Manually reset message counts

## Power

- Support for Zynq-7000 - Includes the processor subsystem and the programmable logic.
- Modelling of the power down mode for XADC blocks in 7 series devices.

## Vivado IP Integrator

- Full production release. Now available with every seat of Vivado Design Suite
- Automated IP upgrade flow for migrating a design to the latest IP version
- Cross-probing is now enabled on IP integrator generated errors and warnings
- Integration with System Generator generated IP
- Synthesis run times for IP integrator generated designs are up to 4x faster
- ECC (error-correcting code) is now supported in MicroBlaze™ within IP integrator

## Vivado IP Catalog

- Bottom-up synthesis enabled in project based designs to reduce synthesis run times
  - IP that have not changed will not be resynthesized
- Significant enhancements to the "Manage IP" Flow
  - Creation and management of IP simplified. An IP project is automatically created to manage the netlisting of IP.
  - Easy generation of a synthesized design checkpoint (DCP) for IP to enable IP use in blackbox flows using third party synthesis tools
  - DCP for IP and the Verilog stub files are now co-located with the XCI File for the IP
  - Scripts are delivered for compiling IP simulation sources for behavioral simulation using third party simulators
- Improved handling of IP Constraints

- IP DCP contains the netlist and constraints for the IP
- Constraints are scoped automatically

### Vivado Simulation

- Run time improvement
  - Enabled user control to choose compilation rerun in Vivado simulator. See the *Vivado Design Suite User Guide: Logic Simulation* (UG900).
- Improved post processing automation for simulation
  - Post TCL hook capability added. See the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

### Static Timing Analysis

- Rename tool-generated clocks: create_generated_clock -name option
- Create clock constraints interactively from clock network reports
  - New right-click menus
  - Create clocks and generated clocks

### Vivado I/O Planner

- Increased SSN analysis resolution
  - Enabled temperature grade based SSN analysis

### Vivado Debug

- Device support:
  - Added support for Zynq 7Z100
  - Added support for 7 Series XQ package & speed grade changes
  - Added support for Virtex®-7 HT General ES devices (7VHT580T and 7VHT870T)
- Target Communication Framework (TCF) agent (hw_server):
  - Added Xilinx Platform Cable USB JTAG cable support
  - Auto start of TCF agent (hw_server)
  - Auto discovery of JTAG cables
- Serial I/O Debug:
  - Vivado serial I/O analyzer support for IBERT 7 Series GTZ 3.0
- Added support for debugging multiple FPGAs in the same JTAG chain

## Tandem Configuration for Xilinx PCIe IP

Tandem Configuration can be used to meet the fast enumeration requirements for PCI™ Express. A two stage bitstream is delivered to the FPGA. The first stage configures the Xilinx PCIe® IP and all design elements to allow this IP to independently function as quickly as possible. Stage two completes the device configuration while the PCIe link remains functional. Two variations are available: Tandem PROM loads both stages from the same flash device, and Tandem PCIe loads stage two over the PCIe link. All PCIe configurations are supported up to X8Gen3.

- Tandem Configuration is now released with production status, for both Tandem PROM and Tandem PCIe. Devices with this status include:
  - XC7K325T-FFG900
  - XC7VX485T-FFG1761 (PCIE X1Y0 location required)
  - XC7VX690T-FFG1761 (PCIE X0Y1 location required)
- Tandem Configuration is available as beta for additional devices, for both Tandem PROM and Tandem PCIe. Hardware testing for these devices has been limited.
  - XC7K160T-FFG676
  - XC7K410T-FFG676
  - XC7VX415T-FFG1158 (PCIE X0Y0 location recommended)
  - XC7VX550T-FFG1158 (PCIE X0Y1 location recommended)
- For more information, see PG054 (version 2.1) for Gen2 PCIe IP, or PG023 (version 2.1) for Gen3 PCIe IP.

# Important Information

## Migrating Vivado Designs from Vivado Design Suite 2013.1 to 2013.2

*Table 1-1:* **Specifics for Migrating Vivado Designs to Vivado Design Suite 2013.2**

| Change in 2013.2 | Impact on Designs | Resolution |
|---|---|---|
| Xilinx 2013.1 IP: Constraints are processed in a different order by the 2013.2 tools. | • In 2013.2, by default, IP constraints are processed before user constraints, instead of after as in 2013.1.<br>• In 2013.2, the _clocks.xdc file no longer contains clock definitions. Now it contains clock-dependent constraints. Also, the file is now processed after the user constraints by default, instead of before.<br>• Timing failures, critical warnings, or other issues might occur. | Regenerate Xilinx IP in 2013.2. |
| Managed IP flow now automatically creates an IP project. | • IP directories from 2013.1 sessions are not automatically populated in the 2013.2 IP project. | Must manually read the IP .xci through read_ip command at the Tcl Console of the IP Project session. |

## Updates to Existing IP

- AXI Ethernet
  - New IEEE 1588 hardware timestamping for 1-step and 2-step
- AXI Ethernet Lite
  - Virtex-7 in production
- Tri-Mode Ethernet MAC
  - Virtex-7, Artix-7, Zynq-7000 in production
- GMII2RGMII
  - Zynq-7000 in production
- 10G Ethernet MAC, RXAUI, XAUI
  - Virtex-7, Zynq-7000 in production
- PCI32 and PCI64
  - Artix-7 in production

- For a detailed list of Xilinx IP Cores, see the *IP Release Notes Guide* (XTP025) [Ref 2]

# Known Issues

Vivado™ Design Suite Tools Known Issues can be found at Answer Record 55120

# Architecture Support and Requirements

## Operating Systems

Xilinx only supports the following operating systems on x86 and x86-64 processor architectures.

### Microsoft Windows Support

- Windows XP Professional (32-bit and 64-bit), English/Japanese
- Windows 7 Professional (32-bit and 64-bit), English/Japanese
- Windows Server 2008 (64-bit)

### Linux Support

- Red Hat Enterprise Workstation 5 (32-bit and 64-bit)
- Red Hat Enterprise Workstation 6 (32-bit and 64-bit)
- SUSE Linux Enterprise 11 (32-bit and 64-bit)

## Architectures

The following table lists architecture support for commercial products in the Vivado™ Design Suite WebPACK™ tool vs. all other Vivado Design Suite editions. For non-commercial support:

- All Xilinx® Automotive devices are supported in the Vivado Design Suite WebPACK tool.
- Xilinx Defense-Grade FPGA devices are supported where their equivalent commercial part sizes are supported.

*Table 2-1:* **Architecture Support**

| | Vivado WebPACK Tool | Vivado Design Suite (All Other Editions) |
|---|---|---|
| Zynq™ Device | Zynq-7000 Device (Early Access)<br>• XC7Z010, XC7Z020, XC7Z030 | Zynq-7000 Device (Early Access)<br>• All |
| Virtex® FPGA | Virtex-7 FPGA<br>• None | Virtex-7 FPGA<br>• All |
| Kintex™ FPGA | Kintex-7 FPGA<br>• XC7K70T, XC7K160T | Kintex-7 FPGA<br>• All |
| Artix™ FPGA | Artix-7 FPGA<br>• XC7A100T, XC7A200T | Artix-7 FPGA<br>• All |

# Compatible Third-Party Tools

*Table 2-2:* **Compatible Third-Party Tools**

| Third-Party Tool | Red Hat Linux | Red Hat Linux-64 | SUSE Linux | Windows XP 32-bit | Windows XP 64-bit | Windows-7 32-bit | Windows-7 64-bit |
|---|---|---|---|---|---|---|---|
| **Simulation** | | | | | | | |
| Mentor Graphics ModelSim SE/DE (10.1b) | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Mentor Graphics ModelSim PE (10.1b) | N/A | N/A | N/A | Yes | Yes | Yes | Yes |
| Mentor Graphics Questa Advanced Simulator(10.1b) | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Cadence Incisive Enterprise Simulator (IES) (12.2) | Yes | Yes | Yes | N/A | N/A | N/A | N/A |
| Synopsys VCS and VCS MX (G-2012.09) | Yes | Yes | Yes | N/A | N/A | N/A | N/A |
| The MathWorks MATLAB® and Simulink® with Fixed-Point Toolbox (2011a, 2011b, 2012a, 2012b) | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Aldec Active-HDL (9.2)[a] | N/A | N/A | N/A | Yes | Yes | Yes | Yes |
| Aldec Riviera-PRO (2012.10) | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

*Table 2-2:* **Compatible Third-Party Tools**

| Third-Party Tool | Red Hat Linux | Red Hat Linux-64 | SUSE Linux | Windows XP 32-bit | Windows XP 64-bit | Windows-7 32-bit | Windows-7 64-bit |
|---|---|---|---|---|---|---|---|
| **Synthesis**[b] | | | | | | | |
| Synopsys Synplify/Synplify Pro (H-2013.03)[c] | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Mentor Graphics Precision RTL/Plus (2012c) | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| **Equivalence Checking** | | | | | | | |
| Cadence Encounter Conformal (9.1)[d] | Yes | Yes | Yes | N/A | N/A | N/A | N/A |

a. ***Note:*** Support for Aldec simulators is offered by Aldec.

b. ***Note:*** Most Vivado IPs can only be synthesized by Vivado synthesis, because the RTL source may include encrypted files. To use these IPs in a third-party synthesis flow, the synthesized netlist can be exported from the Vivado tool in a suitable format for use in the third-party synthesis project.

c. ***Note:*** Contact Synopsys for availability of Synplify Overlay or Service Pack.

d. ***Note:*** Cadence Encounter Conformal Support is for RTL2Gate using Synopsys Synplify only.

# System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

## System Memory Recommendations

For memory recommendations for the Vivado Design Suite tools, see: http://www.xilinx.com/design-tools/vivado/memory.htm.

### Operating Systems and Available Memory

The Microsoft Windows and Linux® operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs may encounter this limitation. The Vivado Design Suite has optimized memory and enabled support for applications to increase RAM memory available to Xilinx tools.

**Windows XP Professional 32-bit**

Xilinx applications are enabled to take advantage of the memory increase feature on Windows 32-bit systems. You must then modify Windows setting to get access to this larger memory.

The standard Windows OS architecture limits the maximum memory available to a Xilinx process to 2 Gigabyte (GB). In Windows XP Professional, Microsoft created an option to support the ability of an application to address 3 GB of RAM. Xilinx Vivado Design Suite tools have built-in support for this option. To take advantage of this capability, you must also modify your Windows XP OS to enable this feature, which requires that you modify your `boot.ini` file by adding a "/3GB" entry to the end of the "startup" line.

Before enabling 3 GB support for Xilinx applications, read the *Microsoft Knowledge Base Article #328269*. If you upgrade your computer to Windows XP Service Pack 1 (SP1) and you are using the /3GB switch, Windows may not restart without a patch from Microsoft. See Answer Record 17905 for more information.

Additionally, before making this change, read:

- Microsoft Bulletin Q17193 which contains information on "Application Use of 4GT RAM Tuning"
- Microsoft Bulletin Q289022 which contains instructions for editing your `boot.ini` file

**Linux**

For 32-bit Red Hat Enterprise Linux systems, the operating system can use the hugemem kernel to allocate 4 GB to each process. More information can be found on the Red Hat support site at http://www.redhat.com/docs/manuals/enterprise/.

## Cable Installation Requirements

Platform Cable USB II is a high-performance cable that enables Xilinx design tools to program and configure target hardware.

***Note:*** The Xilinx Parallel Cable IV is no longer supported for debugging or programming.

To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.

The cable is officially supported on the 32-bit and 64-bit versions of the following operating systems: Windows XP Professional, Windows-7, Red Hat Linux Enterprise, and SUSE Linux Enterprise 11. Additional platform specific notes are as follows:

- Root privileges are required.
- SUSE Linux Enterprise 11: The fxload software package is required to ensure correct Platform Cable USB II operation. The fxload package is not automatically installed on

SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.

- Linux LibUSB support: Support for Platform Cable USB II based upon the LibUSB package is now available from the Xilinx website, see Answer Record 29310.

For additional information regarding Xilinx cables, refer to the following documents:

- *USB Cable Installation Guide* (UG344) [Ref 3]
- *Platform Cable USB II Data Sheet* (DS593) [Ref 4]
- *Parallel Cable IV Data Sheet* (DS097) [Ref 5]

## Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

*Table 2-3:* **Equipment and Permissions Requirements**

| Item | Requirement |
|---|---|
| Directory permissions | Write permissions must exist for all directories containing design files to be edited. |
| Monitor | 16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels. |
| Drive | You must have a DVD-ROM for Vivado Design Suite (if you have received a DVD, rather than downloading from the web). |
| Ports | To program devices, you must have an available parallel, or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable.<br>***Note:*** Installation of the cable driver software requires Windows XP Pro SP1 (or later), or Windows-7. If you are not using one of these operating systems, the cables may not work properly. |

***Note:*** X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

### Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

# Download and Installation

This guide explains how to download and install the Vivado™ Design Suite tools which includes the Vivado Integrated Design Environment (IDE), High Level Synthesis tool, and System Generator for DSP.

## Downloading the Vivado Design Suite Tools

This section explains how to download the Vivado Design Suite tools.

The Vivado Design Suite tools are available as a standalone download. This results in a smaller and faster download.

***Note:*** Vivado Design Suite 2013.2 offers the following device programming capabilities:

- Connect to JTAG cable and query the device chain
- Directly program a Xilinx® 7 series FPGA device with a BIT file
- Check the various status registers of Xilinx 7 series FPGA devices

For all other capabilities offered by Xilinx ISE Lab Tools and Xilinx ISE Design Suite, you will need to install the standalone version of the Xilinx ISE Lab Tools.

To begin, open an internet browser and navigate to the Xilinx Download Center at http://www.xilinx.com/support/download/index.htm.

Most files in the Xilinx Download Center are downloaded using the Akamai download manager. For the optimum download experience:

- Allow pop-ups from entitlenow.com
- Set security settings to allow for secure and non-secure items to be displayed on the same page
- Allow the Akamai download manager to run Java processes

To download the Xilinx Design Tools:

1. Select the **Design Tools** tab in the web page.
2. Under the Version heading, click the version of the tools you want to download.
3. Click the link for the installer you want to download.

***Note:*** The multiple file download option contains four smaller downloadable archives and is the recommended option for customers who cannot reliably download the larger install files. This option requires all four files listed in the section be downloaded prior to running the installer. See Important Information area of the web page section for more details.

4. Enter your User ID and Password to log into your Xilinx account.

   ***Note:*** If you do not have a Xilinx account, you must create one in order to download products.

   An address verification screen appears.

5. Once the current address is correct, click **Next**.
6. The Akamai download manager launches in your browser to complete the download process. If you have trouble using the Akamai download manager, look on the download page under "Having Trouble Downloading?". You can follow a link to a Xilinx Answer Record which will allow you to obtain the tools without using the download manager.

   Most files in the Xilinx Download Center are packaged using TAR methods. You will need to use software from a third party provider to unpack them. Consult your IT department for assistance. Commonly used tools for TAR files are 7-ZIP, GNU built-in tools, WinZIP, and WinRar. These tools are licensed solely by each respective developer, and not by Xilinx. Xilinx hereby disclaims any warranties, express or implied, including warranties of merchantability, fitness for a particular purpose, or non infringement with respect to these suggested software tools.

# Installing the Vivado Design Suite Tools: Overview for All Platforms

This section explains the installation process for all platforms for the Vivado Design Suite tools. Before installation:

- Disable anti-virus software to reduce installation time.
- Make sure you have the necessary privileges for the system on which the design tools will be installed. Some components, such as programming cable device drivers, require administrator-level permissions.
- Close all open programs before you begin installation.
- Make sure your system meets the requirements described in Chapter 2, Architecture Support and Requirements.
- Check the links in Important Information in Chapter 1 for any installation issues pertaining to your system or configuration.
- The Vivado Design Suite installer does not set global environment variables, such as XILINX, on Windows. To find out if this affects the way you run Xilinx design tools, see "Platform-Specific Installation Instructions."

- When running `xsetup.exe` from a 32-bit machine onto the network location of a 64-bit machine, the tools will install the 32-bit executables onto that machine and not the 64-bit executables.

# Platform-Specific Installation Instructions

This section provides platform-specific instructions for installing the Vivado Design Suite tools.

## Microsoft Windows Installation

How you start installation depends on how you obtained the installation program. See Downloading the Vivado Design Suite Tools for details on your options.

- If you downloaded an installation file, decompress that file and run **`xsetup.exe`**.
- If you downloaded the installation file in multiple parts, decompress the file with the `.zip` extension and run **`xsetup.exe`**. You should not decompress any other files
- If you received a Xilinx Design Tools DVD, load the DVD. If the auto-run feature of your DVD drive is enabled, the setup program should start automatically. If it does not, browse to the DVD in Windows Explorer and run **`xsetup.exe`**.

## Linux Installation

The method of starting the installation depends on how you have obtained the installation program. See Downloading the Vivado Design Suite Tools for details on your options.

- If you have downloaded an installation file, decompress that file and run the **`xsetup`** program contained therein.
- If you downloaded the installation file in multiple parts, decompress the file with the `.zip` extension and run **`xsetup`**. You should not decompress any other files.
- If you have ordered and received a Xilinx Design Tools DVD, load the DVD. Click the setup file in your file manager, or browse to the root of your DVD drive and type **`./xsetup`**.

# Installation Flow

The following section describes important screens you will encounter during the installation process.

***Note:*** For each of the following installation steps, click on the text of any item with a check box next to it to obtain more information. Information is displayed in the "Description" area near the bottom of the screen.

## Select Download Location Directory

This step applies to users who downloaded the installation files in multiple archive files. If you downloaded a single image, skip to Accepting Software Licenses.

This screen lists all the required additional installation files to complete the installation. Users will need to point the tool to a location that contains these files. All the required files should be in the same directory. Once the correct files have been identified, the installer will check the integrity of these files to ensure archives are not corrupt. This process might take a few minutes to complete.

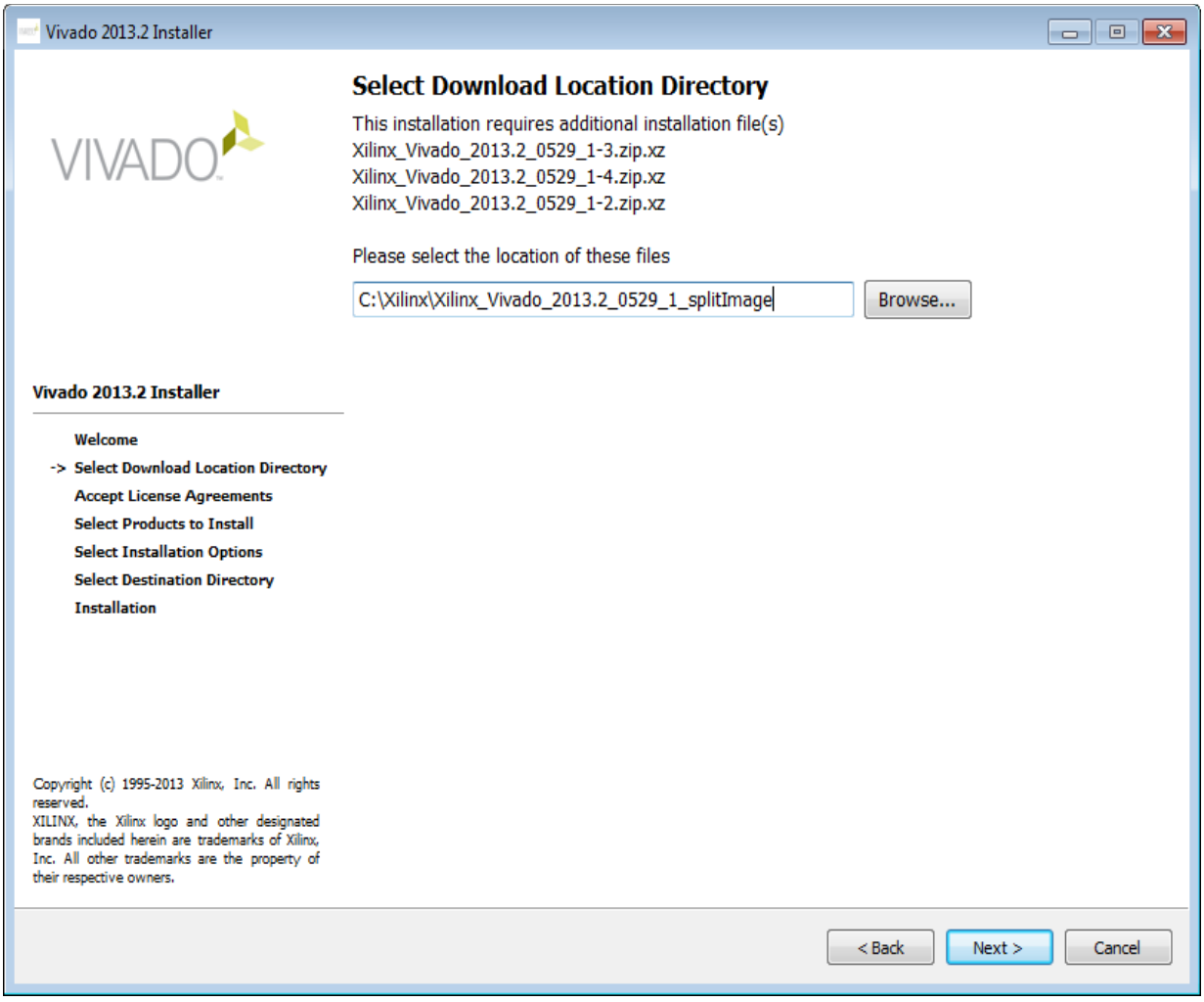


*Figure 3-1:* **Vivado Design Suite Installation - Select Download Location Directory**

## Accepting Software Licenses

You must accept two software license agreements. On each Accept Software Agreement screen:

1. Click **I accept and agree to the terms and conditions above**.
2. Click **Next**.

## Select Xilinx Products to Install

Select the Xilinx products you want to install.

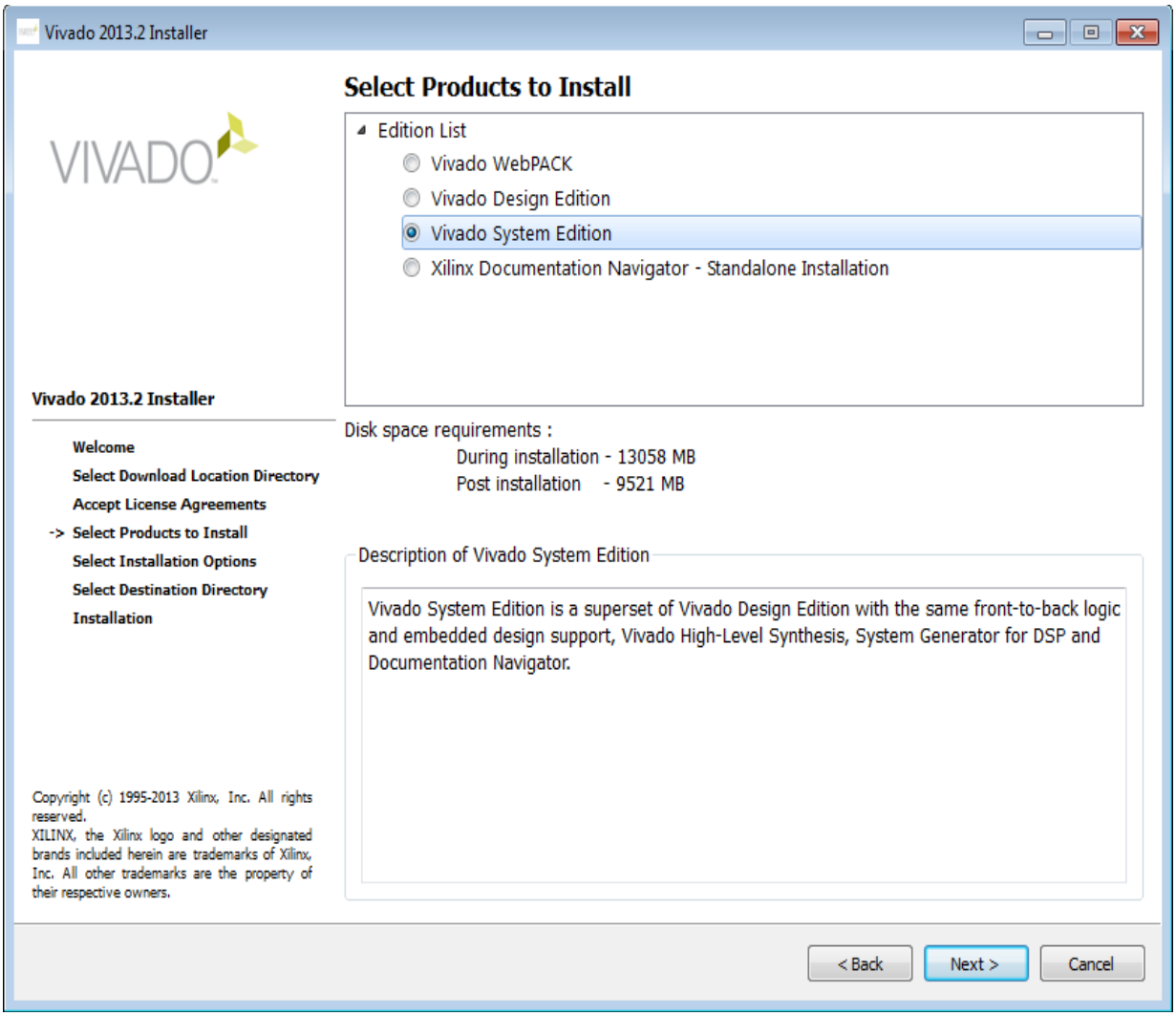


*Figure 3-2:* **Vivado Design Suite Installation - Select Products**

## Select Installation Options

There are several optional installation steps during installation. If selected, these options install toward the end of the installation process, after the main installation has completed.

Select Xilinx Installation Options from the following screen.

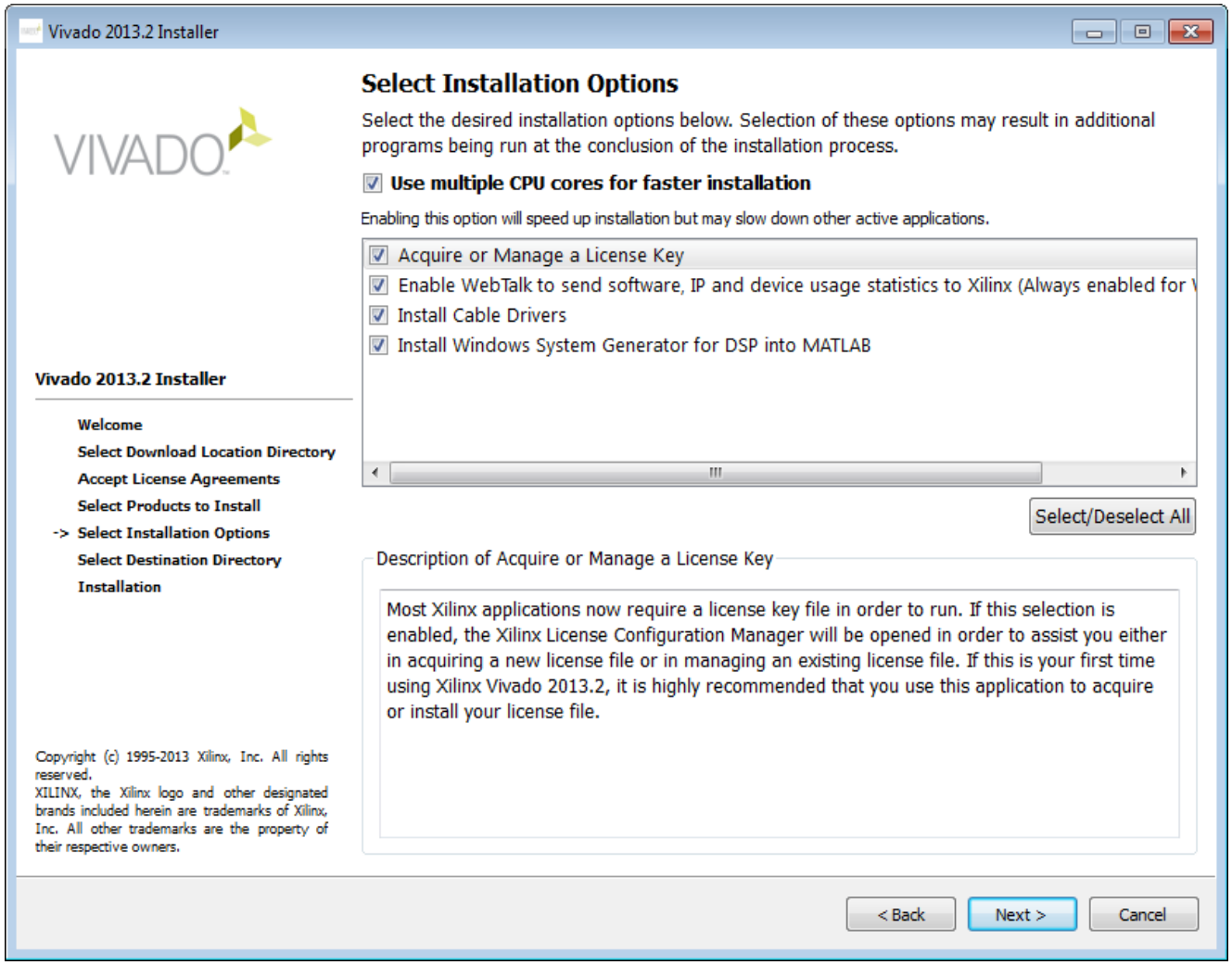


*Figure 3-3:* **Vivado Design Suite Installation - Select Installation Options**

***Note:*** WebTalk is always enabled when using the WebPACK™ tool. If you install an Edition product, the installer allows you to deselect Enable WebTalk. However, if a WebPACK tool license is used to process the design, Enable WebTalk is ignored. Please click on the Enable WebTalk item, in the installer, and read the description box for full details.

## Select Destination Directory

In the Select Destination Directory screen, select the directory in which to install the design tools. Enter a name for the Program Folders list. The installer displays a level of hierarchy

underneath the installation path you specify. The name of the directory varies depending on the type of product you are installing.

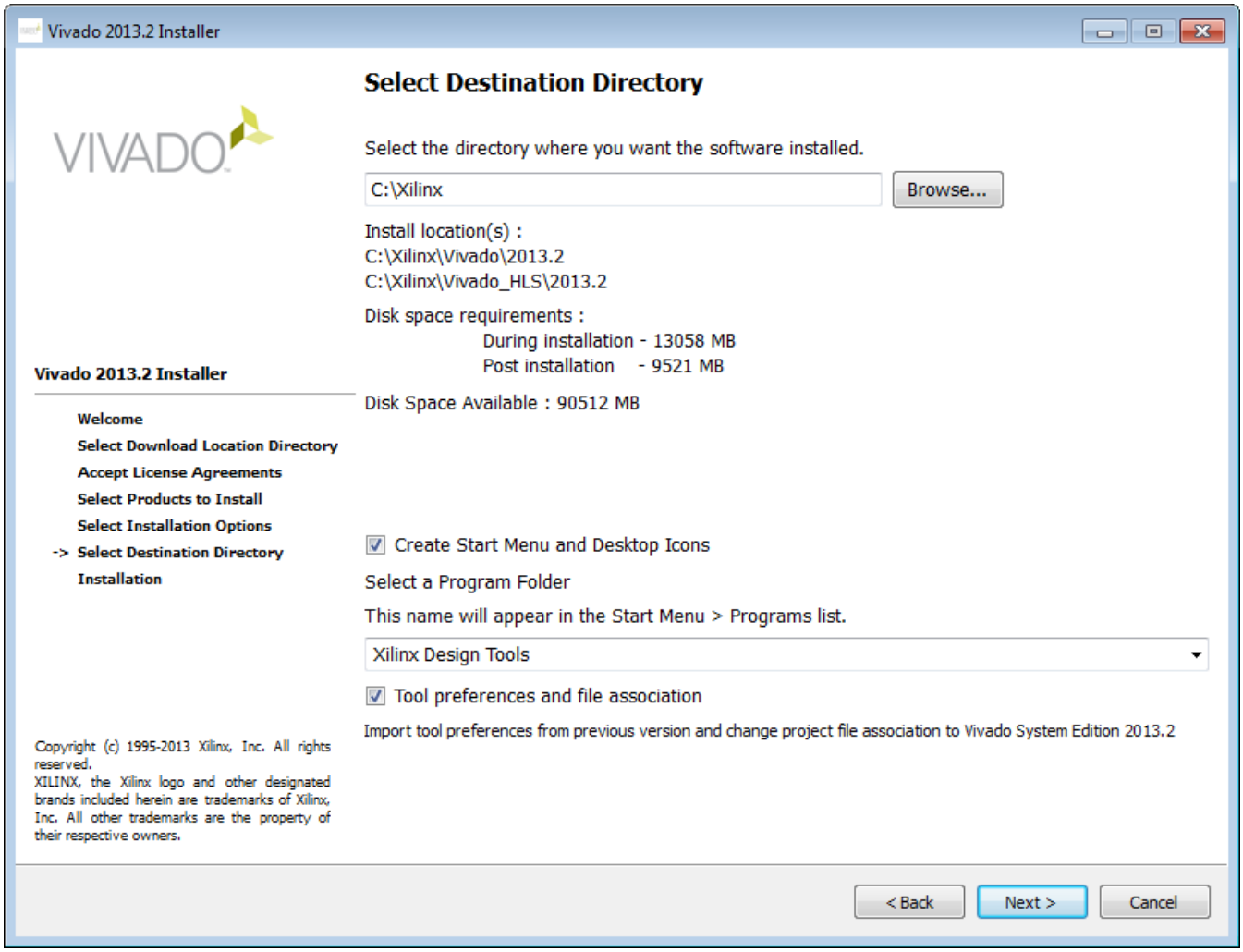


*Figure 3-4:* **Xilinx Design Tools Installation - Select Destination Directory**

## Installation Options Summary

The Installation Options Summary screen summarizes the tools, products, and options to be installed. To begin installation, click **Install**.

Near the end of the installation, the Xilinx License Configuration Manager opens by default. Follow the instructions in the Manager to obtain or locate a license file.

***Note:*** EDK tools require the Cygwin tools distributed by RedHat. A copy of these tools is distributed with the EDK installation.

## Setting Environment Variables

### Microsoft Windows Clients

When installation is complete, the installation program creates an environment variable batch file. All appropriate Desktop and Program Group shortcuts call this file before launching the target application.

To set environment variables in make or script files:

Add **<XILINX installation directory>\settings32.bat** or **settings64.bat** to your script. The numbers 32 or 64 corresponds to the bit-width of the operating system installed on the computer.

### Linux Clients

When installation is complete, the installation program creates an environment variables file.

1. Go to the XILINX installation directory.
2. Type either **source settings32.(c)sh** or **source settings64.(c)sh**, as required for your shell.

To set your environment variables manually or from within your setup script, Xilinx recommends you copy the settings from the appropriate file for your operating system, as listed above. Xilinx environment variables settings are specific to each operating system platform.

# USB FLEXid Dongle Driver Installation

If you purchased a USB FLEXid Dongle for use with the Windows operating systems, you must install the appropriate driver before creating a FLEXnet license for use with it.

1. Install the Xilinx Design Tools first. This installation contains the installer files for the USB FLEXid dongle driver.
2. Run **FLEXId_Dongle_Driver_Installer.exe** from `<Xilinx Installation Directory>\Vivado\2013.2\lds_lite\ISE\bin\nt`.
3. On the Select Options screen, be sure only **FLEXid 9 Drivers** is checked.

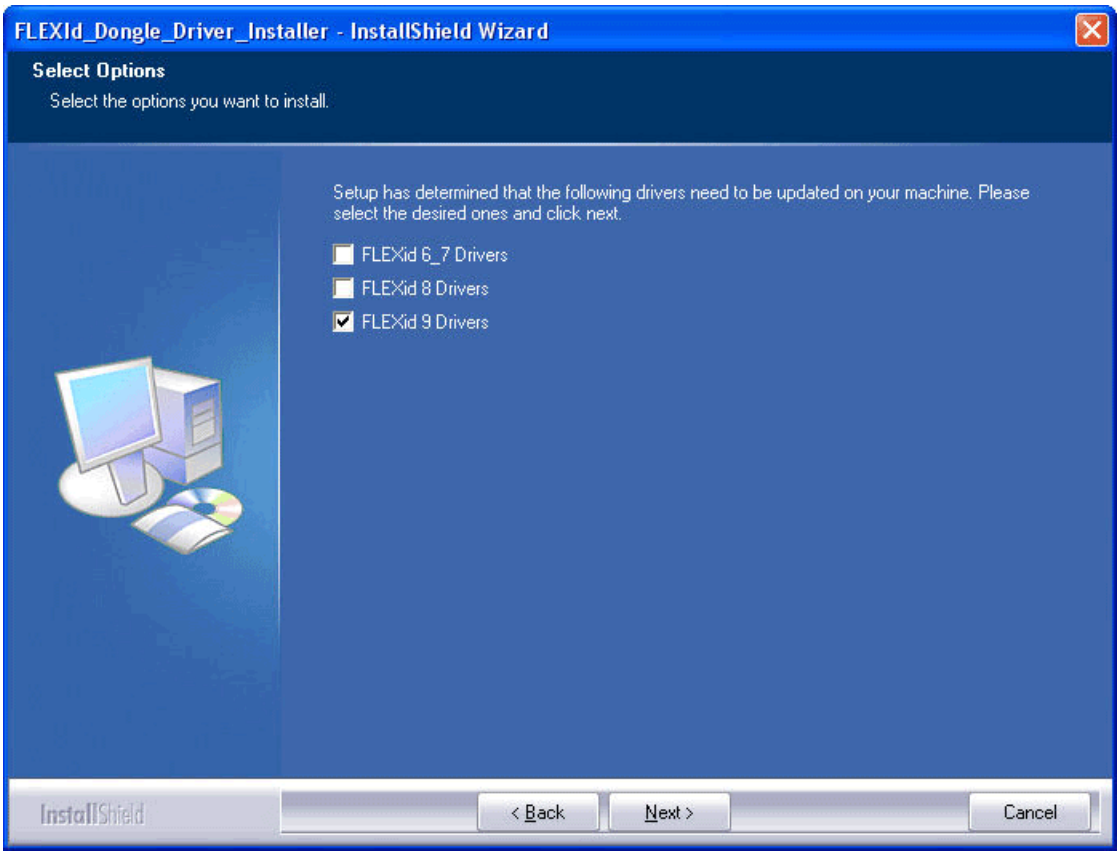


*Figure 3-5:* **Select Options Screen**

4. Click **Next** twice. The driver installs.

After installation, you will need to reboot to ensure the dongle operates correctly.

# Network Installations

Installing to a network location provides a way for client machines to access the design tools by pointing to it on the network drive. To run the design tools on the network, the client machines must be set up correctly to ensure the environment variables, registry, and program groups all point to the network. The following sections describe the procedure for network setups.

## Linux Clients

Each user must source **`settings32.(c)sh`** or **`settings64.(c)sh`** (whichever is appropriate for your operating system) from the $XILINX area in which the design tools are installed. This points the Xilinx environment variable, path, and LD_LIBRARY_PATH to the installed location.

To run the design tools from a remotely installed location, run an X Windows display manager, and include a DISPLAY environment variable. Define DISPLAY as the name of your display. DISPLAY is typically unix:0.0. For example, the following syntax allows you to run the tools on the host named `bigben` and to display the graphics on the local monitor of the machine called `mynode`:

```
setenv DISPLAY mynode:0.0
xhost = bigbenPC Clients
```

## Microsoft Windows Clients

1. Install design tools to a PC network server. Make sure your users know the location of the design tools and have access to the installation directory, and they have Administrator privileges for the following steps.
2. From the local client machine, browse to the following directory: *network_install_location*\Vivado\<version>\bin and run the program **shortcutSetup.bat**.
3. Running this program sets up the Windows settings batch files and Program Group or Desktop shortcuts to run the Xilinx tools from the remote location.
4. From the client machine, launch the Vivado Design Suite tools by clicking the **Program Group** or **Desktop** shortcuts, or by running the applications on the network drive.

## Installing to a Mounted Network Drive

Xilinx design tools are designed to be installed in a directory under ROOT (typically C:\Xilinx). The installer normally presents this option when installing to a local driver. When installing to a mounted network drive, if a subdirectory is not defined, it appears to the Installer as if it is installing to a ROOT directory.

To work around this issue, define your target installation directory as "\Xilinx" under the network mount point (For example: “N:\Xilinx”).

Windows 7 default security levels won’t allow you to select remote mapped drives as an Administrator. In order to install Xilinx Design Tools on remote mapped drives, you need to change your account control settings using the steps below:

1. Open the Windows Control Panel, from the Windows Start menu, and select ‘User Accounts’. If your Control Panel Uses ‘Category View’, you will need to click ‘User Accounts’ on two successive screens
2. Click on ‘Change User Account Control settings’ and allow the program to make changes
3. Click and slider the slider-bar down to the second to lowest setting (as seen in the below figure). Click OK.

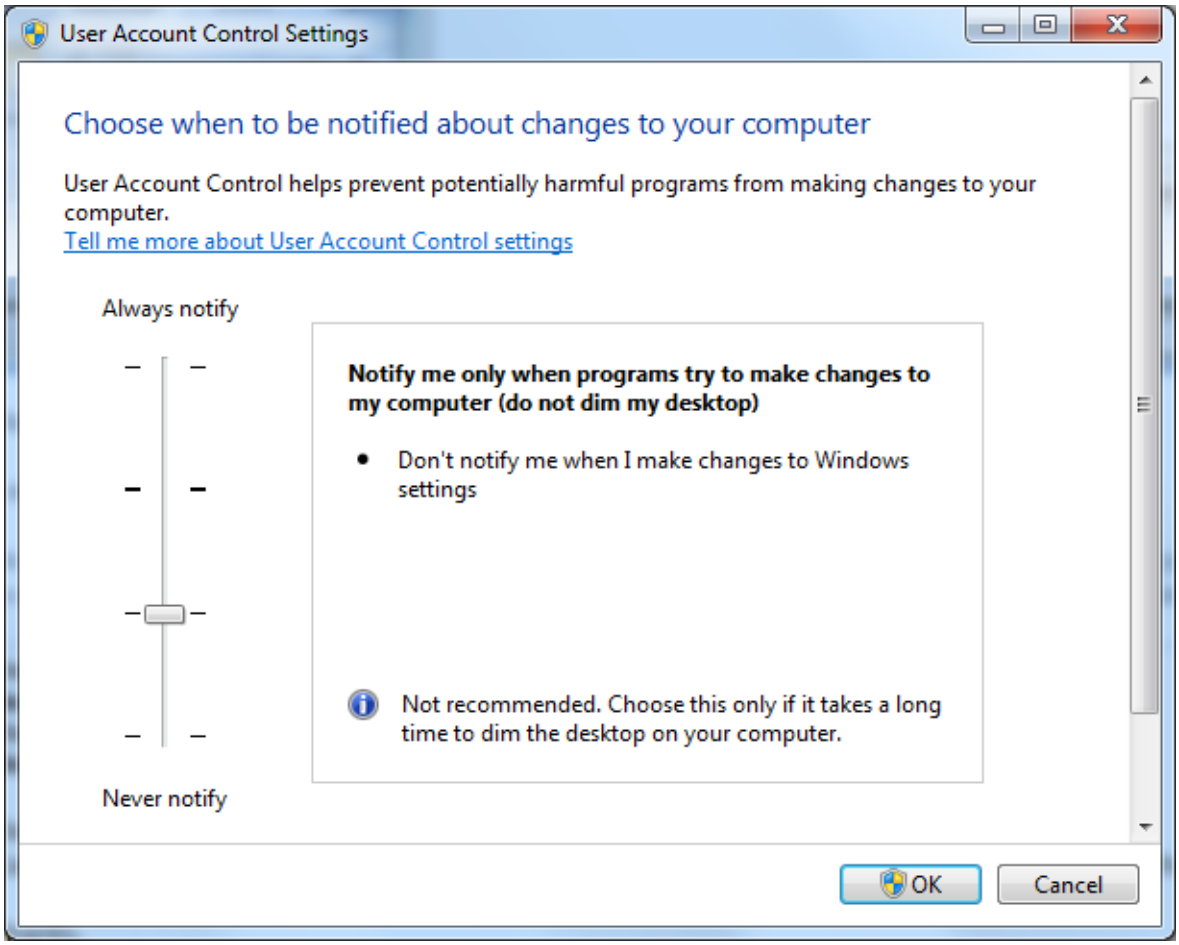


*Figure 3-6:* **User Account Control Settings**

Xilinx recommends you revisit this procedure to restore your settings to their previous state after installation.

***Note:*** You will not be able to browse to remote mapped drives using the Xilinx installer. You will need to manually type in your installation path which contains a mapped network drive.

# Obtaining Quarterly Releases

Xilinx releases quarterly versions of the Vivado Design Suite tools throughout the year. Each quarterly version contains device support updates, new features and bug fixes. The following sections describe how to obtain updates through XilinxNotify and the Download Center.

### XilinxNotify

The XilinxNotify tool is the preferred method of obtaining updates. It provides the following features:

- Compares the latest version of Xilinx design tools updates available on the Xilinx Support website with what you have installed, and notifies you if a newer version is available.
- Provides a Download button allowing you to log in to the Xilinx Download Center. Once you log in, the download of your selected product begins.
- XilinxNotify will run automatic periodic checks at Vivado tools startup time.

  ***Note:*** Select **Edit > Preferences** in the Vivado IDE to control the frequency of the automatic periodic checks.

### Download Center

Quarterly releases for all platforms are regularly made available on the Xilinx Download Center [Ref 6].

## Uninstalling the Vivado Design Suite Tool

Before uninstalling, make sure to have moved any project files you want to keep outside your Xilinx installation directory structure, or they will be deleted.

***Note:*** Xilinx Documentation Navigator will not be removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. You will need to uninstall it separately if it is no longer required.

### Uninstalling on Microsoft Windows

To uninstall any Xilinx product, select the **Uninstall** item from that product's Start Menu folder. For instance, to uninstall the Vivado WebPACK design tools or an Vivado Design Suite: Edition, select **Start > All Programs > Xilinx Design Tools > Vivado 2013.2 > Accessories > Uninstall**.

### Uninstalling on Linux

To uninstall the Vivado Design Suite tool product, launch the uninstaller from the launcher menu, **Applications > Xilinx Design Tools > Vivado 2013.2 > Accessories > Uninstall**.

# WebTalk

The WebTalk feature helps Xilinx understand how you use Xilinx® FPGA devices, software, and intellectual property (IP). The information collected and transmitted by WebTalk allows Xilinx to improve the features most important to you as part of our ongoing effort to provide products that meet your current and future needs. When enabled, WebTalk provides information on your use of the Vivado™ Design Suite tools.

## WebTalk Participation

Your participation in WebTalk is voluntary except in the following cases:

- You are using a WebPack™ license.
- You are using pre-release software or devices.

In these cases, WebTalk data collection and transmission always occurs, regardless of your preference settings. For all other cases, data is not collected or transmitted if you disable WebTalk.

The table below summarizes WebTalk behavior for data transmission to Xilinx from your post-route design, based on your Xilinx license, WebTalk install preference, and user preference settings.

*Table 4-1:* **WebTalk Behavior for Bitstream Generation or Route Design Flow**

| Design Flow | License | WebTalk Install Preference | WebTalk User Preference | WebTalk Data Transmission to Xilinx |
|---|---|---|---|---|
| Bitstream Generation/ Route Design | WebPACK (or pre-release software) | Ignored | Ignored | Yes (Send) |
| Bitstream Generation/ Route Design | Design Edition or System Edition | Enabled | Enabled | Yes (Send) |

*Table 4-1:* **WebTalk Behavior for Bitstream Generation or Route Design Flow**

| Design Flow | License | WebTalk Install Preference | WebTalk User Preference | WebTalk Data Transmission to Xilinx |
|---|---|---|---|---|
| Bitstream Generation/ Route Design | Design Edition or System Edition | Enabled | Disabled | No (Do Not Send) |
| Bitstream Generation/ Route Design | Design Edition or System Edition | Disabled | Ignored | No (Do Not Send) |

***Note:*** WebTalk currently transmits data after Route Design for all devices.

# Setting WebTalk Install Preference

You can enable or disable WebTalk globally during or after installation as described below. During installation you can enable or disable WebTalk installation options by checking or unchecking the **Enable WebTalk to send software, IP and device usage statistics to Xilinx (Always enabled for WebPACK license)** checkbox**.**

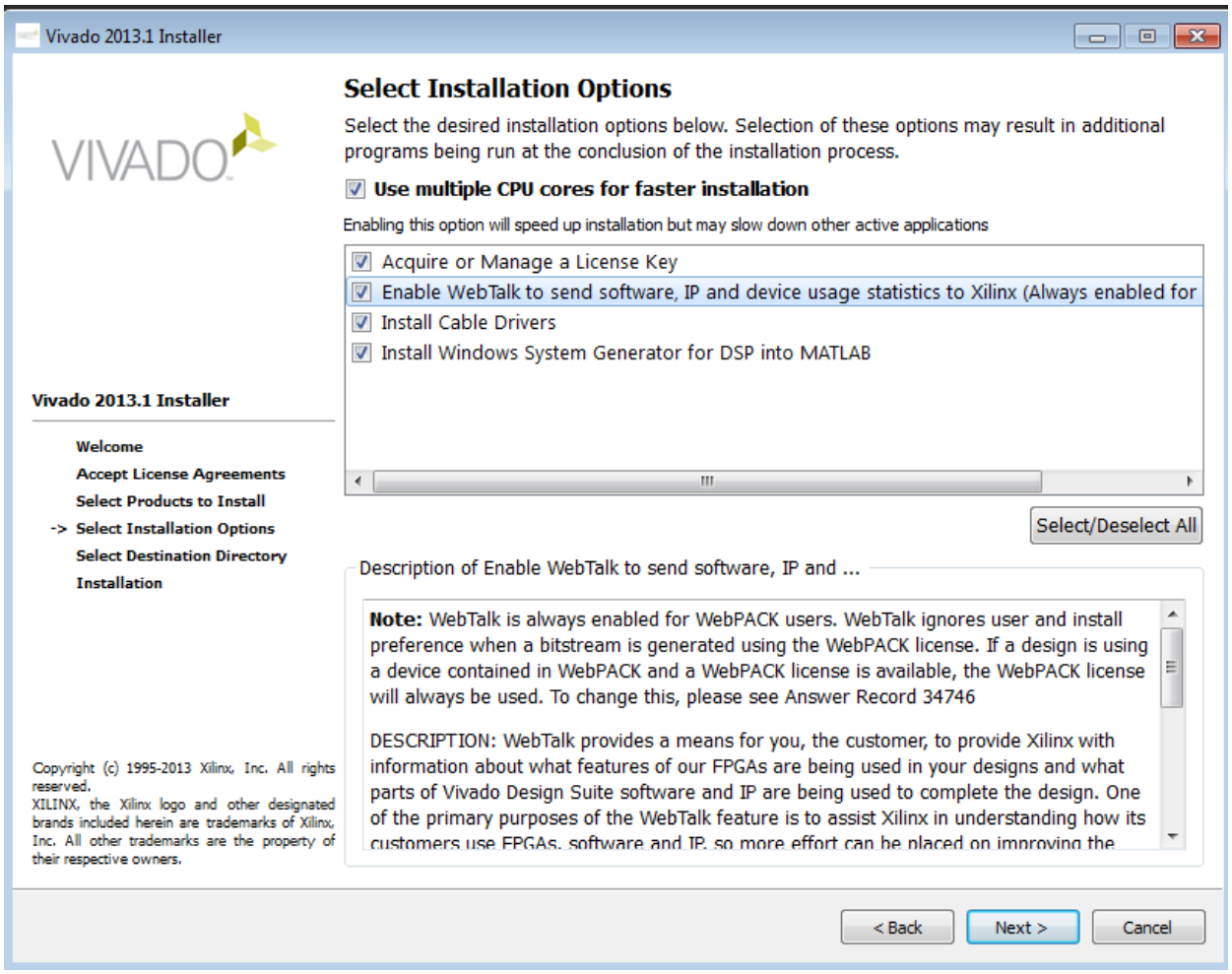


*Figure 4-1:* **WebTalk Install Options**

You can enable or disable WebTalk installation options using the Tcl command **`config_webtalk`**:

**`config_webtalk -install on|off`**

**`on`** turns WebTalk on for the installation.

**`off`** turns WebTalk off for the installation.

Install settings are saved in the following location:

- **Windows 7**: `<install dir>/vivado/data/webtalk/webtalksettings`
- **Linux**: `<install dir>/vivado/data/webtalk/webtalksettings`

***Note:*** You need administrator privileges to write to the install location.

# Setting WebTalk User Preferences

You can enable or disable WebTalk user options by selecting **Tools > Options > General** as shown below.

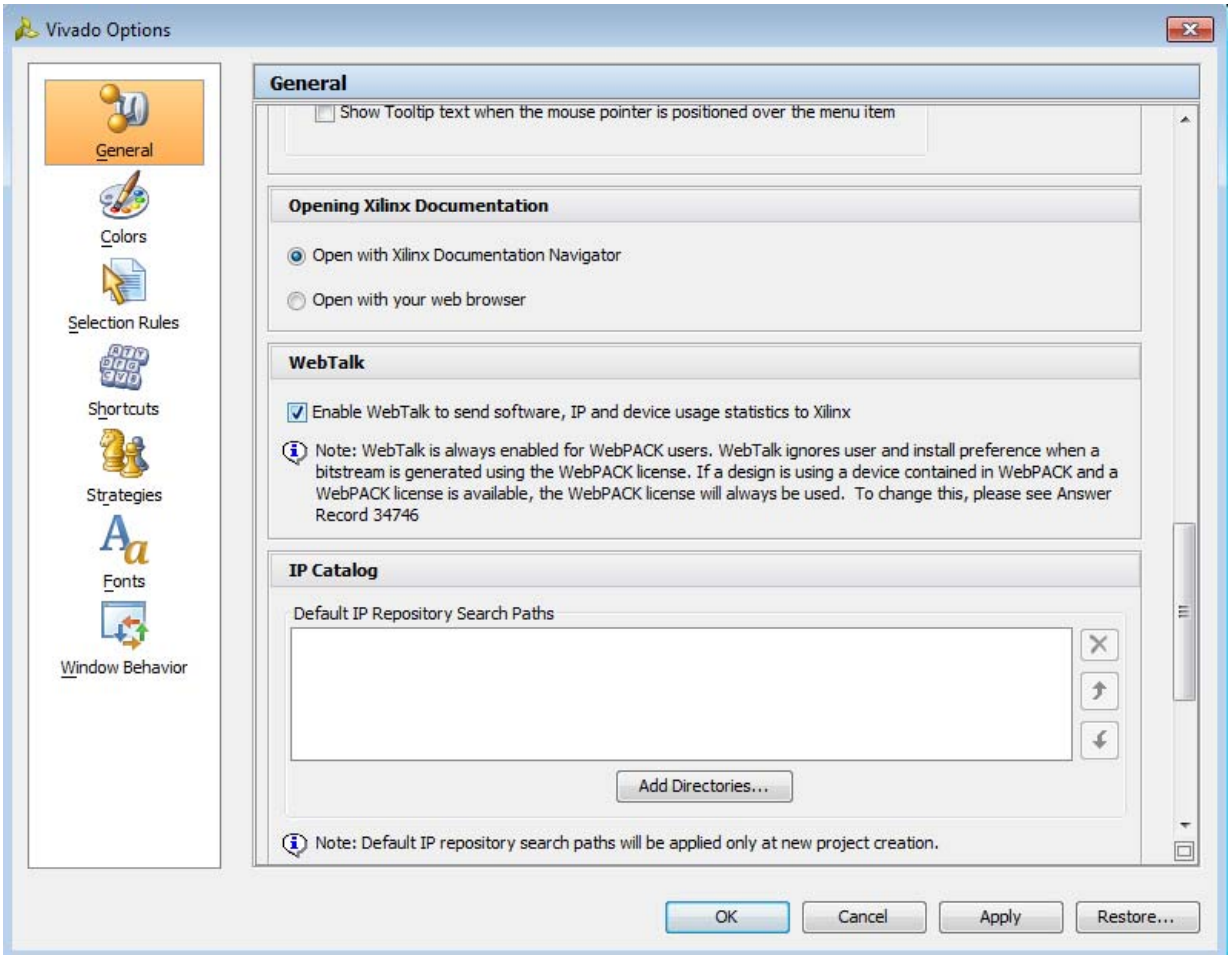


*Figure 4-2:* **WebTalk User Preferences**

After installation, you can enable or disable WebTalk user options using the `config_webtalk` Tcl command:

```
config_webtalk -user on|off
```

`on` turns WebTalk on for the current user.

`off` turns WebTalk off for the current user.

User settings are saved in the following location:

- **Windows 7**:

`%APPDATA%\Xilinx\Common\<version>\webtalk`

where:

`%APPDATA%` is:

`C:\Users\<user>\AppData\Roaming`

- **Linux**:

`%APPDATA%/.Xilinx/Common/<version>/webtalk`

where:

`%APPDATA%` is:

`/home/<user>`

# Checking WebTalk Install and User Preferences

You can also use the **`config_webtalk`** Tcl command to check the current status of WebTalk settings. The command line option **`-info`** reports the values for the install setting and the user setting:

```
config_webtalk -info
```

# Types of Data Collected

WebTalk does not collect your design netlist or any other proprietary information that can be used to reverse engineer your design. The data that Xilinx collects through WebTalk includes:

- Software version
- Platform information (for example, operating system, speed and number of processors, and main memory)
- Unique project ID
- Authorization code
- Date of generation
- Targeted device and family information

For more information on the type of data that is collected, see the Xilinx Design Tools WebTalk page [Ref 7] available from the Xilinx website. To see the specific WebTalk data

collected for your design, open the `usage_statistics_webtalk.xml` file in the project directory. You can also open the `usage_statistics_webtalk.xml` file for easy viewing of the data transmitted to Xilinx.

# Transmission of Data

WebTalk is invoked after bitstream or route design compilation. WebTalk bundles the collected data in an `usage_statistics_webtalk.xml` file and sends this file to Xilinx by https (hypertext transfer protocol secure) post. Every new compilation for a given design overwrites the previous `usage_statistics_webtalk.xml` file. WebTalk also writes an HTML file equivalent `usage_statistics_webtalk.html` file for easy viewing of the data transmitted to Xilinx. WebTalk also writes to the `vivado.log` (or `runme.log`) file that contains additional information about whether the file was successfully transmitted to Xilinx.

# Obtaining and Managing a License

The Xilinx® Product Licensing Site is an online service for licensing and administering evaluation and full copies of Xilinx design tools and intellectual property (IP) products. This chapter describes the FLEXnet license generation functionality of the Product Licensing Site.

## Accessing the Product Licensing Site

You can access the Xilinx Product Licensing Site in various ways depending upon the type of license being generated.

- If you purchased products, follow the link included in your order confirmation email. It will provide direct access to an account containing your product entitlements.
- To evaluate the Vivado™ Design Suite products, go to http://www.xilinx.com/products/design_tools/vivado/vivado/vivado-webpack.htm.
- To evaluate IP products, go to http://www.xilinx.com/ipcenter and follow the Evaluate link on the IP product page of interest.
- To access the Product Licensing Site directly, go to http://www.xilinx.com/getlicense. You must first register or enter your registration information.

*Figure 5-1:* **Xilinx Licensing Sign In Page**

You must first sign in. If you already have a Xilinx user account, enter your user ID and password, and then confirm your contact information is current. If you do not have an account, click the **Create Account** button.

# Changing Xilinx User Account Information

It is important to keep your Xilinx User Account up to date. As you change companies, addresses or emails may change.

## Modifying your Corporate Email Address

1. Go to www.xilinx.com.

*Figure 5-2:* **Xilinx Website**

2. Click **Sign In**.

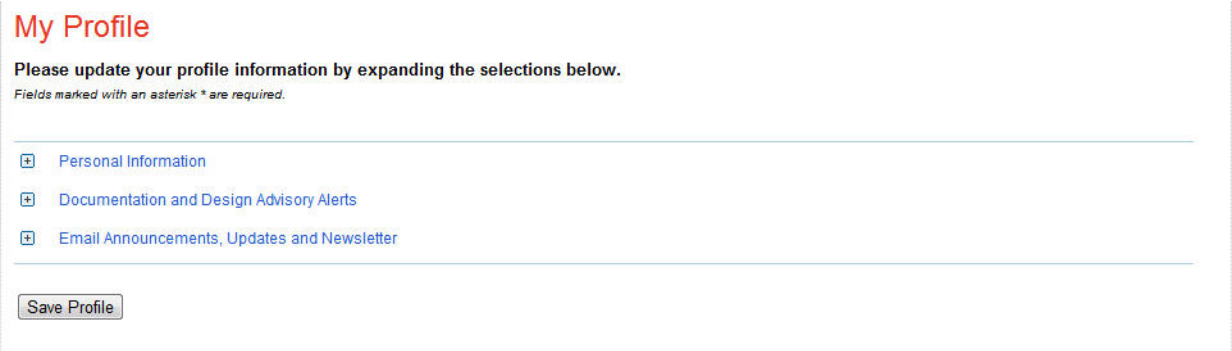


*Figure 5-3:* **Personal Information**

3. Expand **Personal Information**.

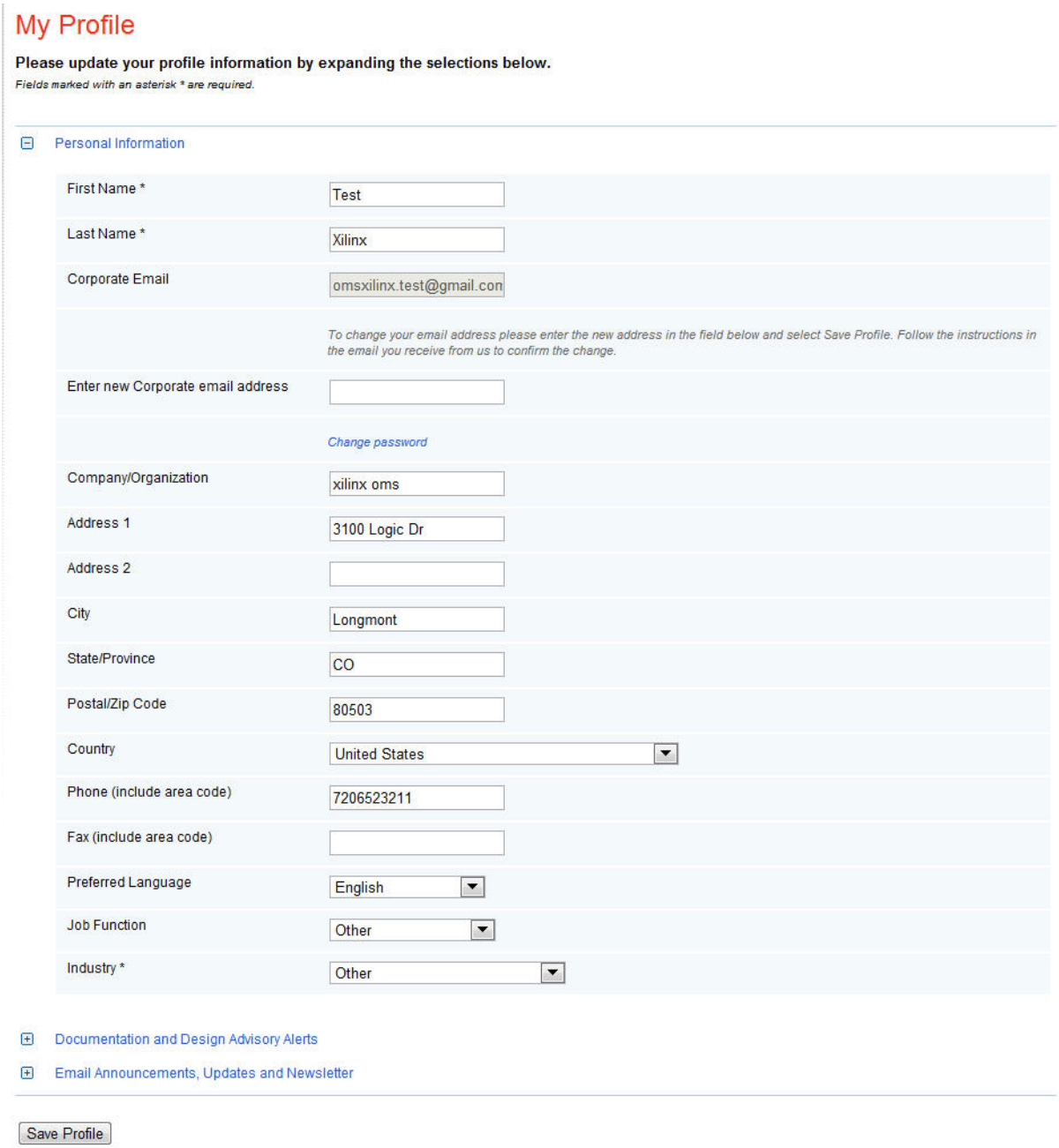


*Figure 5-4:* **Enter New Corporate email Address**

4. Enter your new corporate email address in the **Enter new Corporate email address** box.
5. Click **Save Profile** button for changes to take effect.

# Product Licensing Accounts

When you purchase a design tool edition or IP product from Xilinx, you are purchasing a license to use and receive updates for that product for one year. The license to use Xilinx deign tools and IP products is managed through the use of product entitlements. A product entitlement is the determination of:

- Which product was purchased
- The number of seats purchased
- The license type (floating or node-locked)
- The product subscription period (product updates are provided throughout the year)

In addition to managing the product entitlements for your purchased design tools and IP, you can also access product entitlements for No Charge or Evaluation products. Full and No Charge licenses have a subscription period of one year. Design tools evaluations are for 30 days, and IP evaluations are for 120 days.

Activating a product entitlement results in one or more license keys being generated by the website. When installed, the license keys enable the use of the design tools and IP that were purchased or are being evaluated. Your product entitlements and resulting license key files are managed in a product licensing account on the Xilinx website.

Product licensing accounts are specific to the individual listed on the Xilinx Software Purchase Order, who is either the end user or administrator of the design tools. All purchases made can be managed in the same product licensing account if a single administrator is named. A company site can have multiple accounts managed by different administrators. The latter is helpful if a site has multiple design teams working on differing projects with different budget pools.

***Note:*** A license key can be generated for a product entitlement that has expired; however, it will only enable product releases up to the subscription end date. Applying a product update made available after the subscription end date of your license results in an error.

## LogiCORE IP License Generation in the Xilinx Design Tools

Any LogiCORE™ IP and design tools entitlements you have purchased appear in your list of entitled products when you log into the Product Licensing Site. Licenses for Evaluation and No Charge IP are available on the site in a separate area. Licenses for all your design tools and IP can now be generated in one pass. They are emailed to you in a single license file. IP core FLEXnet licenses now feature more licensing options, such as single or Triple-Redundant Floating Server support, and more host options for node-locked license keys: Ethernet MAC address, Hard Drive Serial Number or USB Dongle ID.

# User Types and Actions

There are three user types for the Product Licensing Site: customer account administrator, end user, and evaluation user.

## Customer Account Administrator

An example of a typical customer account administrator is a CAD tools manager. Every product licensing account *must* have at least one customer account administrator. A customer account administrator can manage more than one product licensing account.

The responsibilities as the customer account administrator include:

- Generating node-locked or floating licenses for Xilinx design tools and IP products.
- Adding and removing users from the product licensing account.
- Assigning administrative privileges to other users.
- Ordering product DVDs (if desired).

The original customer account administrator is the Ship To contact identified during the product ordering process. That person will receive an email with instructions on how to download and license each purchased product. The customer account administrator must follow the link in the email, to ensure access to the purchased products.

## End User

Adding end users to a product licensing account allows an engineer or design team member the flexibility to manage and generate license keys on their own. The end user may generate license keys for node-locked products entitlements within the account as well as evaluation and "no charge" license keys for design tools and IP products. A customer account administrator can also configure the end user account to allow an end user to generate floating licenses. An end user cannot:

- View or generate floating license keys by default. This privilege may be assigned to them by the customer account administrator.
- View the license keys generated by other users.
- Add or remove other users to or from the product licensing account.

## Evaluation User

Evaluation users can:

- Generate a 30-day free evaluation license key that will enable both ISE and Vivado System Edition
- Generate license keys for evaluation and no charge IP products
- Generate a WebPACK™ tool license that will enable WebPACK features in both ISE and Vivado
- Request a Xilinx Design Tools DVD package with one of the following shipping options:
  - Free Shipping (2-4 Weeks)
  - Standard (2-3 Days)
  - Overnight

***Note:*** A customer who is already licensed for a full version of a Xilinx Design Tools product edition can evaluate other Xilinx Design Tools product editions or IP. These product entitlements are made available in the same product licensing account.

All user types can download products electronically and request a Xilinx Design Tools DVD.

# Creating a License Key File

The Create New Licenses tab on the Product Licensing Site is the starting point for license key file generation. The design tools and IP product entitlements you have purchased or wish to evaluate are shown in the product entitlement table.

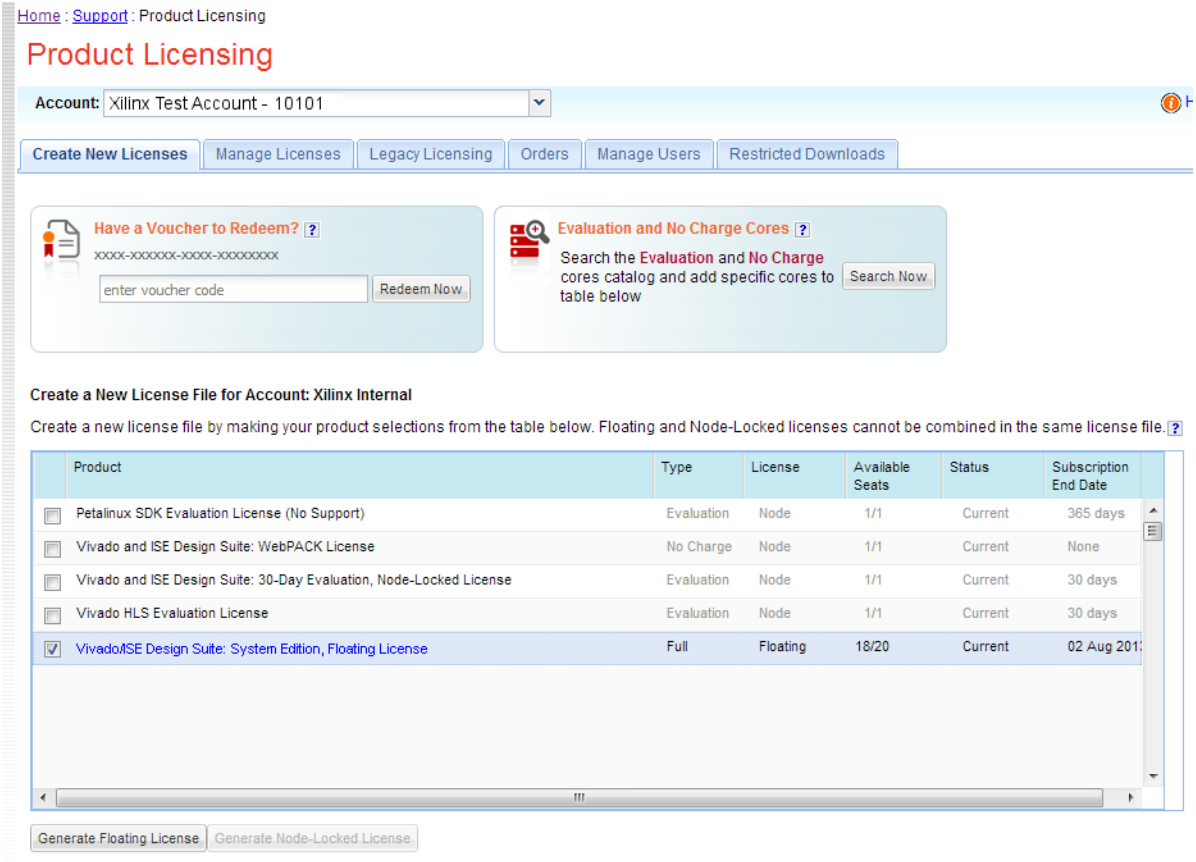


*Figure 5-5:* **Create New License**

## Selecting Products

To begin the license generation process for products you have purchased or want to evaluate:

1. Select a product licensing account from the Account drop-down list.

   ***Note:*** This selection is not available if you are entitled to evaluation or free products only.

2. Enter product voucher codes for design tools or IP product licenses purchased with kits or for tools purchased from the Xilinx online store (optional).
3. Add evaluation or no-charge IP product entitlements to the product entitlement table (optional).
4. Make your product selections from the product entitlement table.

The type of product entitlements available are Full (purchased), No Charge, or Evaluation. Full and No Charge licenses have a subscription period of one year. Design tools evaluation is for 30 days. IP evaluations are for 120 days.

Floating and node-locked licenses cannot be combined in the same license key file.

***Note:*** A floating license resides on a network server and enables applications to check out a license when they are invoked. At any one time, the number of licenses for simultaneous users is restricted to the number of license seats purchased. A node-locked license allows for the use of a single seat of a product entitlement on a specific machine.

For design tools, available seats represents the number of seats available for licensing over the total number of seats purchased. For IP, seats are managed according to the terms of the site wide license agreement.

Products with a status of Current are within their warranty period. Products with a status of Expired have a warranty period end date that has passed. If seats are available, licenses can be generated for either Current or Expired product entitlements.

The Xilinx Design Tools: System Edition evaluation product entitlement provides access to all the capabilities in the Xilinx Design Tools tool set. This product entitlement is automatically included in your product licensing account.

Product vouchers for design tools and IP product licenses may be shipped with a Xilinx or partner development board or design kit. If you have a product voucher card, you may enter the voucher code on the card into the associated text field and click Redeem Now. This places the corresponding design tools or IP product entitlement in the product entitlement table which you can use to generate a license key.

To add Evaluation and No Charge IP to the list of product entitlements, click the **Search Now** button in the Add Evaluation and No Charge IP Cores section of the page. This opens an IP product finder tool.

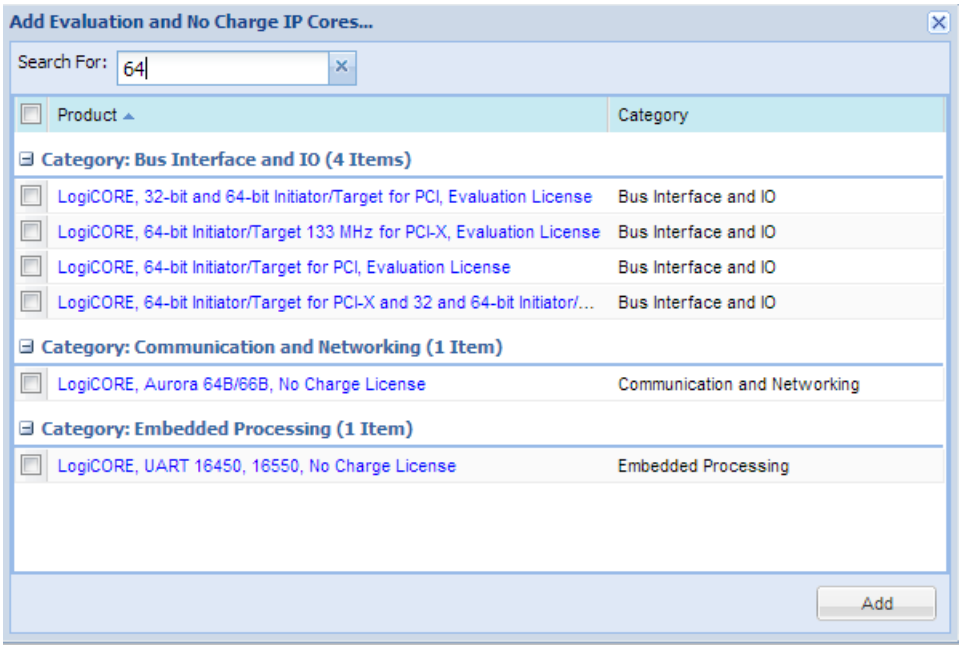


*Figure 5-6:* **IP Product Selector**

***Note:*** IP products are typically sold as site licenses that gives the administrator the ability to generate license keys for floating and node-locked license types. End users see only product entitlements for node-locked products. The customer account administrator, or an End User who has been granted Floating License generation status by the administrator, sees product entitlements for both node-locked and floating products.

## Generating a License

Click the **Generate License** button corresponding to the type of license key file you are generating (floating or node-locked). The license generation form shown below appears.

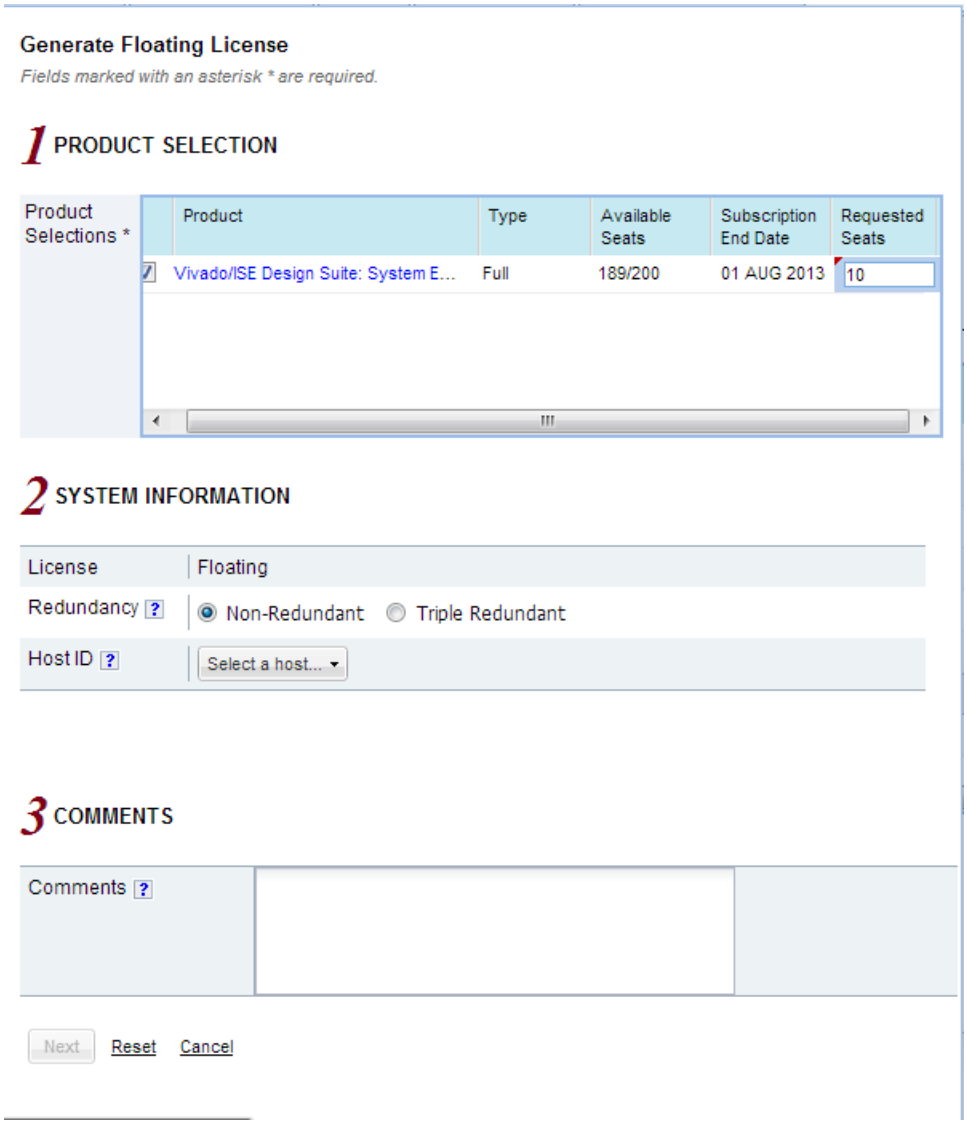


*Figure 5-7:* **Generate Floating License**

To generate floating licenses:

1. Select the number of seats required for each product license.

This is for floating licenses only. All node-locked licenses are for one seat. The number of seats available for a product entitlement is automatically maintained by the system. The Requested Seats field is populated, by default, with the full number of seats remaining on the product entitlement. A product is removed from the product entitlement table if all seats have been activated.

2. Enter system information.

   System information is pre-populated in the option menu if you arrived at the Product Licensing Site from a link within the Xilinx License Configuration Manager (XLCM).

   A redundant server configuration provides a fail over for the license manager software. As long as two of the three servers are running, the license manager can continue to run.

   If you do not have pre-populated system information, or if you want to add a different host, select the **Add a host** option.

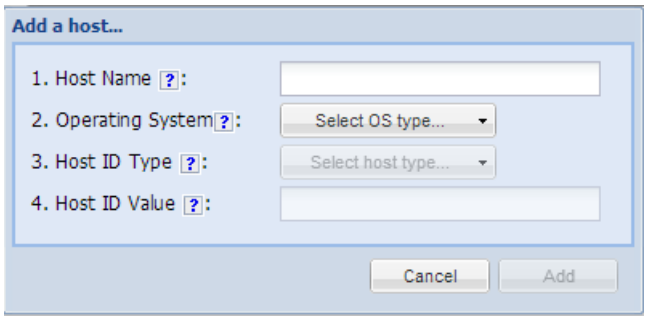


*Figure 5-8:* **Add a Host**

   The host ID value uniquely identifies the machine to which your design tools or IP is licensed. You may choose a host ID type to be a MAC address, a hard drive serial number, a dongle ID, or a Solaris host ID.

   ***Note:*** Not all host ID types are supported for all operating systems. The easiest way to obtain your host ID is to run the XLCM on the machine that will serve as the license host.

3. Add a comment.

   Adding a comment to the license key file makes it easier for an administrator to track the allocation of design tools and IP product entitlements among users.

4. Click **Next**.

   The Review License Request form opens.

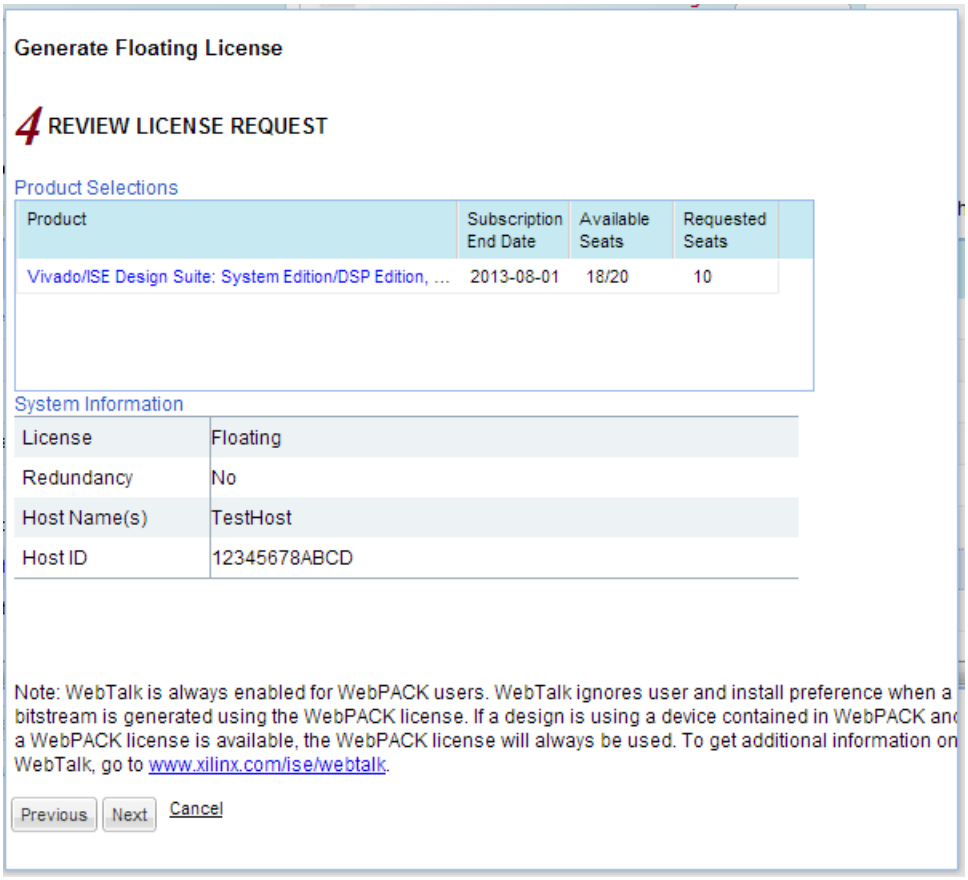


*Figure 5-9:* **Review License Request**

5. Review your selections.
6. If you are satisfied with your selections, click **Next**.

## End User License Agreements

Xilinx Design Tools and No Charge IP product End User License Agreements (EULAs) are agreed to during the product installation process. If you license IP products, you must accept the terms of the associated IP product EULAs before the license file can be generated.

## Third-Party Licenses

A complete copy of the third-party licenses is located at:
`<install_directory>/common/licenses/unified_3rd_party_eula.txt`

## License Generation Confirmation

When you finish generating the licenses, you will receive a confirmation message summarizing your licensing activity.

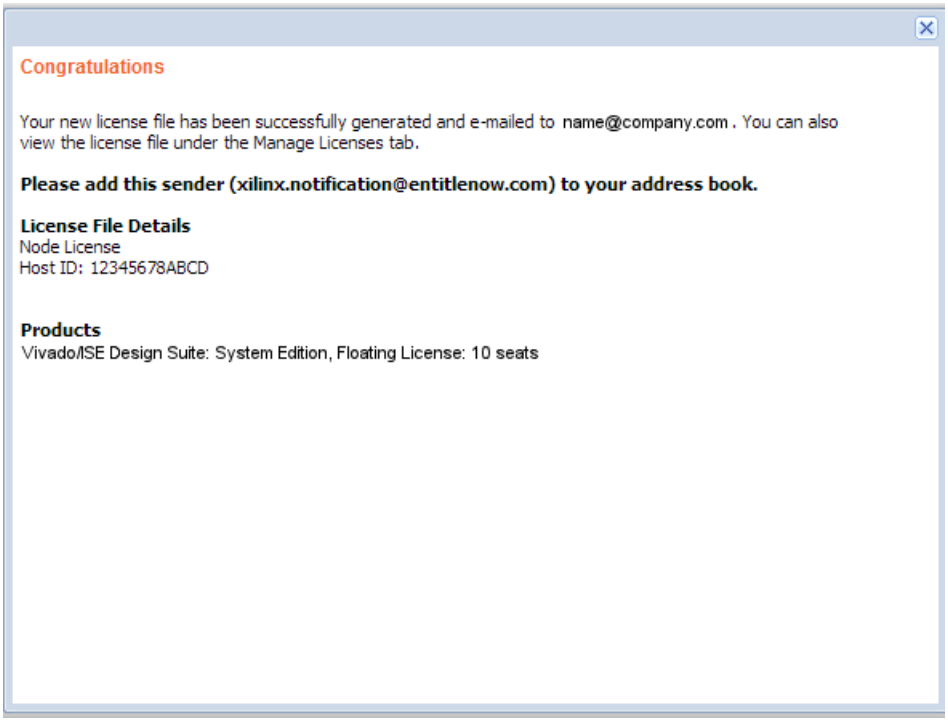


*Figure 5-10:* **License Generation Confirmation**

You will also receive a license generation confirmation email. This message contains the generated license key file as an attachment. Add 'xilinx.notification@entitlenow.com' as a trusted sender in your email address book.

If you do not receive your license by email, you can download it directly from the Xilinx Licensing Site. See the Managing License Key Files section for details

# Managing License Key Files

The Product Licensing Site tracks your license key files. Select the Manage Licenses tab to see all license key files for your product licensing account.

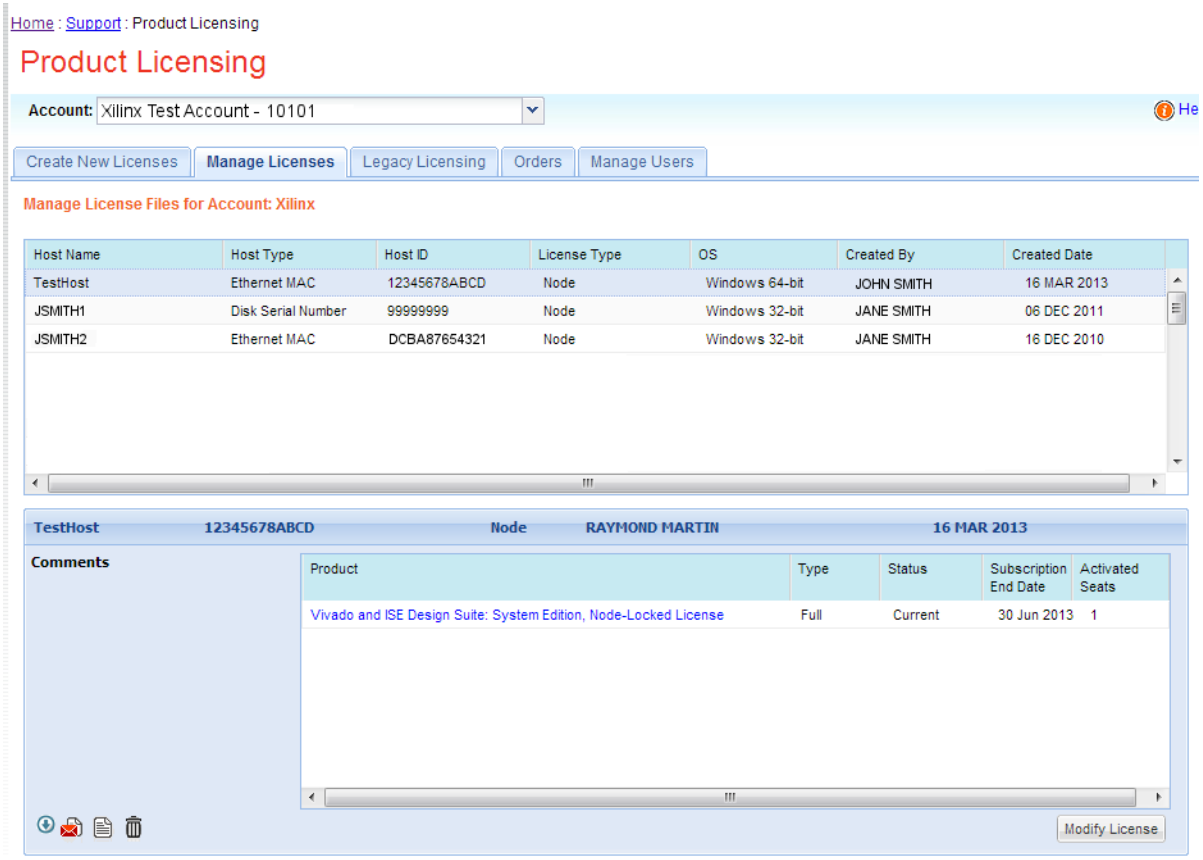


*Figure 5-11:* **Manage Licenses**

Use the Manage Licenses page, to perform the actions described below.

## Exploring and Retrieving Your Existing License Key Files

Information regarding the license key files in your product licensing account are displayed in a split-section view. Click a row in the master view in the top table, to see detailed information about the license key file in the detail view in the bottom table. The detail view table displays:

- A list of product entitlements activated in the key file.
- Comments associated with the key file.

The detail view table gives you the ability to:

- Download - If your license file does not arrive via email you may download the license file here.
- Email - The license file may be emailed to you or another user.
- View - Gives you the ability to view the actual license file.

- Delete - Delete the license file. Once a file is deleted it will then become available on the Create New License page and may be regenerated for another host ID.
- View the end user license agreement (IP only).

## Modifying a License Key File

To modify an existing license key file, select the license key file in the master view. You can modify a license key file as follows:

### Delete an entire license file and place entitlement back into your account

1. From the Manage Licenses Tab (see Figure 5-11), select the license file you wish to delete.
2. Click the **Trash Can** icon located below and to the left of the license file details.
3. Click the **Accept** button to accept the Affidavit of Destruction.

***Note:*** This will delete all license seats in the entire license key file and return the entitlements to your account.

### Rehost or change the license server host for a license key file

1. From the Manage Licenses Tab (see Figure 5-11), select the license file you wish to rehost.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **System Information**.
4. Change or add new Host ID and/or Host Name by using the drop-down list and text entry boxes respectively.
5. Click the **Next** button twice and then click the **Accept** button to accept the Affidavit of Destruction.

### Activate or add additional seats to an existing licensed product entitlement

1. From the Manage Licenses Tab (see Figure 5-11), select the license file to which you wish to add seats.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and add seats up to the total number of seats available in your entitlement.
5. Click **Next** twice. No Affidavit of Destruction is required for adding seats.

### Deactivate or remove seats from an existing licensed product entitlement

1. From the Manage Licenses Tab (see Figure 5-11), select the license file from which you wish to remove seats.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and reduce the number of seats that will be authorized by this license file.
5. Click the **Next** button twice and then click the **Accept** button to accept the Affidavit of Destruction.

### Activate or add additional product entitlements to a license key file

1. From the Manage Licenses Tab (see Figure 5-11), select the license file to which you wish to add features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any new entitlements you wish to add to this license file.
5. Click **Next** twice. No Affidavit of Destruction is required for adding features.

### Deactivate or delete product entitlements from a license key file

1. From the Manage Licenses Tab (see Figure 5-11), select the license file to which you wish to add features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any entitlements you wish to remove from this license file.
5. Click the **Next** button twice and then click the **Accept** button to accept the Affidavit of Destruction.

Modifying a key file uses the same input form as when the license key file was created, except additional product entitlements of the same license type (floating or node-locked) are made available for licensing.

If, during any of the modification steps, you receive a message that you have exceeded your number of rehost attempts, email cs_1@xilinx.com to request additional rehost options.

## Reclaiming Deactivated Product Entitlements

A product entitlement is deactivated when one of the following occurs:

- Rehosting or changing the license server host for a license key file.
- Deactivating or removing seats from an existing licensed product entitlement.
- Deactivating or deleting product entitlements from a license key file.

The license generation facility allows the reallocation of the deactivated seats or product entitlements by making the corresponding seats or product entitlements available for activation in the product entitlements table on the Create License page.

Before the reallocation of entitlement occurs, you must first agree to an Affidavit of Destruction. This legal agreement is required to ensure the deactivated product entitlements are no longer being used.

The number of allocation operations is recorded for each user. Administrators are allowed to reallocate product entitlements five times per major release. End users are allowed to reallocate product entitlements three times per major release.

### What Happens to Your License Key File

For each product entitlement activated, a FLEXnet increment line and corresponding package line is added to the license key file. When a license key file is modified to activate (add) seats for an existing or new product entitlement, additional increment or package lines are added to the license key file.

When a license key file is rehosted or is modified to deactivate (delete) seats or product entitlements, the corresponding increment lines are regenerated or removed from the modified license key file.

## Legacy Licensing

If you wish to obtain a license for Releases 10.1 or earlier, click the **Legacy Licensing** tab.

*Figure 5-12:* **Legacy Licensing**

Then complete the following steps for the respective versions:

### 10.1 and Prior Versions

1. Select the version you desire. You will be prompted to verify your contact information.
2. Fill out the requested form with the required information to receive your registration IDs. Your registration ID will be displayed on the screen and emailed for your records.
3. Go to the Xilinx download center, click the **Archive** link under the **Version** column on the left side of the page to select the product you desire.
4. During the download process you will be prompted to insert your registration ID to complete the download process.

## Understanding Your Tool and IP Orders

The Orders tab will display information regarding the purchasing orders that created the entitlements you see in this account.

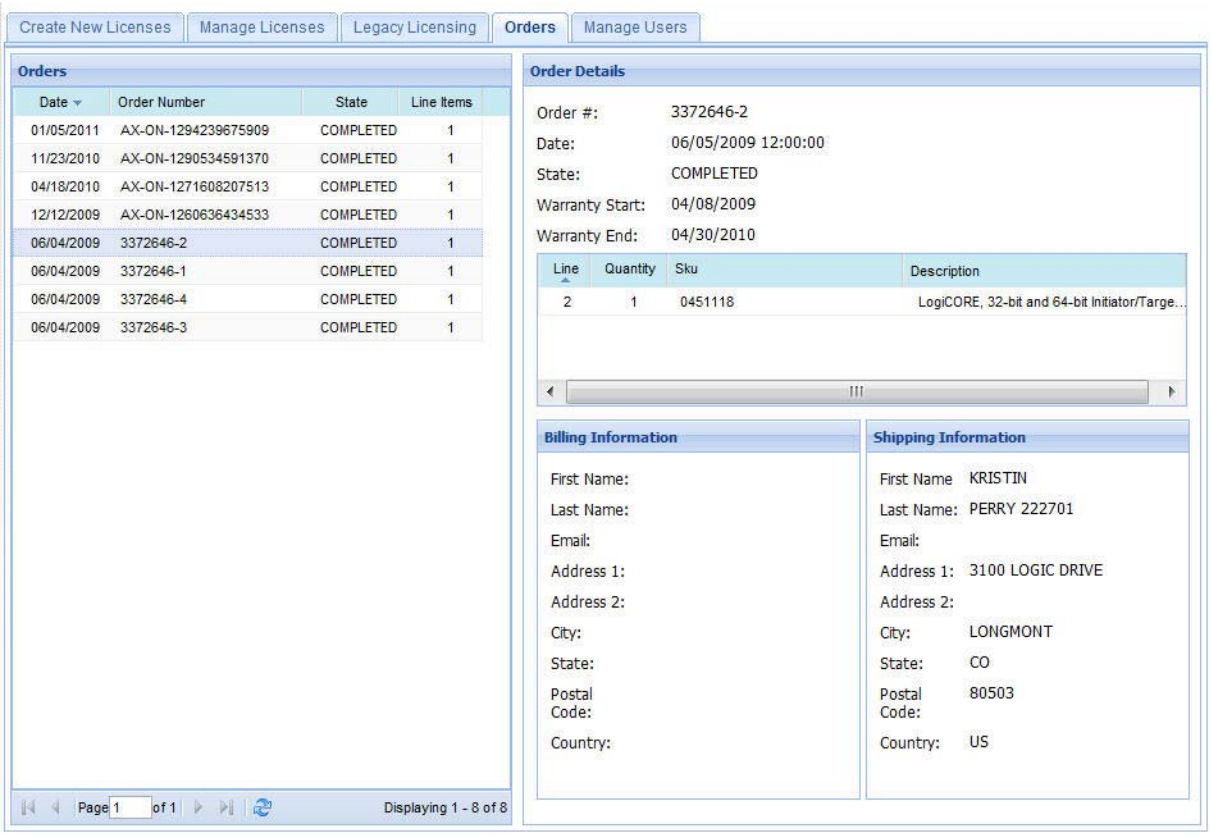


*Figure 5-13:* **Order Information**

- Xilinx order numbers are listed on the left panel of the screen.
- Order details populate on the right panel of the screen when you highlight specific order.
- You may only select one order at a time.
- The order's shipping address information is visible even when product is delivered electronically.

# Managing User Access to Product Licensing Account

The responsibility of administering a product licensing account may be transferred or shared with another user. The ability to add or remove users from a product licensing account is managed under the Manage Users tab.

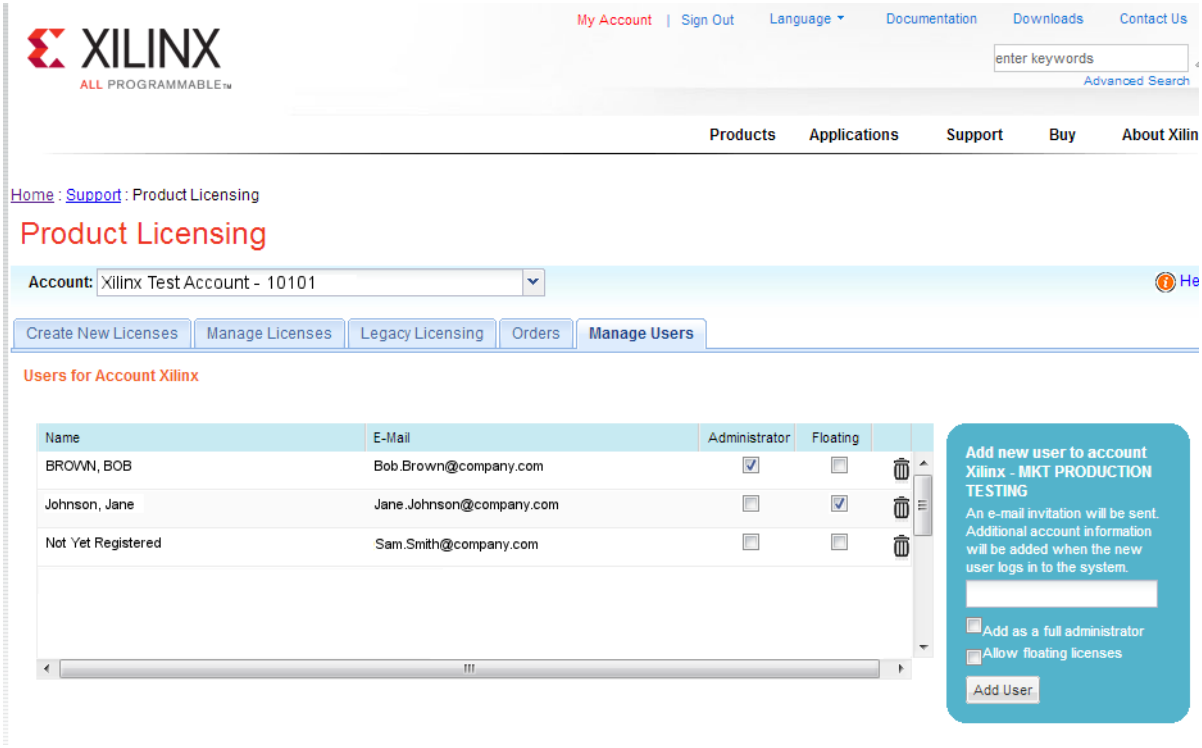


*Figure 5-14:* **Manage Users**

## Adding Users

To add a user to your product licensing account:

- Type in the corporate email address of the new user.
- Check **Add as a full administrator**, to grant the new user customer account administrative privileges. Check **Allow Floating Licenses**, to grant the new user the ability to generate Floating Licenses, but not have full administrative privileges.

***Note:*** The email address you provide must be the same email address the user supplied or supplies when creating their Xilinx account. If not, the user may not be properly recognized when logging in.

If a user has already logged into the Product Licensing Site, their name appears in the user list. If the user has never been to the site, the words Not Yet Registered appears in the space for their name. Once the user has signed in, their name is filled in.

In some instances, a customer account administrator may wish to have design team members administer license key files for their own use. By leaving both Add as full administrator and Allow Floating Licenses check boxes unchecked, the user is granted the following restricted privileges:

- Can generate node-locked license keys only.
- Can view and modify only those license key files they generated for themselves.

- Cannot manage users.

If you check Allow Floating Licenses only, the restriction on node-locked keys is lifted, but the others remain. You cannot check both boxes since it is not allowed. Full administrators already have floating license generation capability.

### Removing Users

To remove administrative or floating license generation privileges from a user, uncheck the **Administrator** or **Floating** check box for that user.

To remove a user from a product licensing account, click the **Trash Can** icon for that user.

## Installing Your License Key File

The following subsections describe installing different types of licenses.

### Node Lock License Installation

After generating a license file, you will receive an e-mail from 'xilinx.notification@entitlenow.com'.

1. Save the license file attached to the e-mail to a temporary directory on your local system.
2. Run the Xilinx License Configuration Manager:
   - For Windows: Select **Start > All Programs > Xilinx Design Tools 14.4 >Accessories > Manage Xilinx Licenses**.
   - For Linux: Type **`xlcm`** in a command-line shell.
3. Click **Copy License** at the top of the Manage Xilinx Licenses tab.
4. Browse to your license file (`Xilinx.lic`) and click **Open**.
5. This copies the license file to the `C:\.Xilinx` (Windows) or `<Home>/.Xilinx` directory of your computer where it will be automatically found by the Xilinx tools.
6. When the Copy License operation is complete, the table on the Manage Xilinx Licenses tab is updated with licensing information from the license file.
7. Click **Close** to exit the Xilinx License Configuration Manager.

## Floating License Installation on Servers

For existing FLEXnet license servers, a common practice is to copy the contents of the license file, mailed from 'xilinx.notification@entitlenow.com', into the existing license file on your FLEXnet server.

***Note:*** Restart the floating license server to enable the Xilinx licenses.

## For New License Servers

1. Download the appropriate Xilinx FLEXnet license utilities for your server's operating system from the Xilinx Download Center at http://www.xilinx.com/download/index.htm.
2. Unzip these utilities into a destination directory. Xilinx recommends you place this directory into your application search path.
3. Once the FLEXnet utilities are installed, run the following commands to start the floating license server:
   - Linux
     - <Server Tool directory>/bin/lin/lmgrd -c <path_to_license>/Xilinx.lic -l <path_to_license>/log1.log
     - <Server Tool directory> bin/lin64/lmgrd -c <path_to_license>/Xilinx.lic -l <path_to_license>/log1.log
   - Windows
     - < Server Tool directory>\bin\nt\lmgrd -c <path_to_license>\Xilinx.lic –l <path_to_license>\log1.log
     - < Server Tool directory>\bin\nt64\lmgrd -c <path_to_license>\Xilinx.lic –l <path_to_license>\log1.log

## Client Machines Pointing to a Floating License

1. Run the **Xilinx License Configuration Manager** (XLCM).
2. Click the **Manage Xilinx Licenses** tab.
3. On the Manage Xilinx Licenses tab, enter the network path to the license server in the port@server format into the XILINXD_LICENSE_FILE field. Click **Set**. The default Xilinx port number is 2100.
4. For Linux operating systems, licensing environment variables cannot be set using the Xilinx License Configuration Manager (XLCM). The environment variable fields are read only, and they are grayed out and there are no Set buttons. The environment variable must be set using the appropriate shell and commands.

# Older Release Notes

## Vivado 2013.1

### What's New

Vivado™ Design Suite 2013.1 introduces two major advances in productivity that will accelerate both time to integration and system-level design. It features the early access of the Vivado IP integrator which is the new Xilinx® intellectual property (IP) centric design environment. It also includes a comprehensive set of libraries to accelerate C/C++ system-level design and high-level synthesis (HLS) in the Vivado HLS tool.

### Device Support

- Zynq™-7000 devices now supported
  - Requires Early Access to Vivado IP integrator
  - Zynq support includes 7Z100 device
- The following devices are production ready
  - Virtex®-7
    - 7VX690T, 7VX1140T, 7VX330T, 7VX415T, 7VX980T
  - Zynq-7000
    - 7Z030 and 7Z045
  - Defense-Grade Kintex™-7Q
    - 7K325T and 7K410T
  - Defense-Grade Virtex-7Q
    - 7V585T and 7VX485T
- The following devices are General ES ready
  - Virtex-7
    - 7VH580T and 7VH870T

# New Vivado Installer

Vivado Design Suite is now available separately from ISE® Design Suite. Both Vivado Design Suite and ISE Design Suite now have their own independent download and installation files.

# Vivado System Edition Products

## Vivado High-Level Synthesis

The Vivado HLS tool has enhanced libraries with support for industry standard floating point math.h operations and real-time video processing functions. Users now have immediate access to video processing functions integrated into an OpenCV environment for embedded vision running on the dual-core ARM® processing system.

- C libraries are enhanced with a new Video library providing support for 31 video and OpenCV Input/Output (I/O) interface functions
  - OpenCV I/O functions: `cvMat2hlsMat`, `IplImage2hlsMat`, `CvMat2hlsMat`, `hlsMat2cvMat`, `hlsMat2IplImage`, `hlsMat2CvMat`
  - Interfaces: `hls::AXIvideo2Mat`, `hls::Mat2AXIvideo`
  - Video functions: `hls::Filter2D`, `hls::Erode`, `hls::Dilate`, `hls::Min`, `hls::Max`, `hls::MinS`, `hls::MaxS`, `hls::Mul`, `hls::Zero`, `hls::Avg`, `hls::AbsDiff`, `hls::CmpS`, `hls::Cmp`, `hls::And`, `hls::Not`, `hls::AddS`, `hls::AddWeighted`, `hls::Mean`, `hls::SubRS`, `hls::SubS`, `hls::Sum`, `hls::Reduce`, `hls::Scale`
- Integration of designs into a software controlled environment is greatly eased with the auto-generation of standalone and Linux software driver files for packaged IP
  - Supported for IP packaged for the Vivado IP catalog and the Embedded Development Kit (EDK) (pcore) environment
- Support is provided for designs packaged for the Vivado IP catalog allowing them to be used in IP integrator
- A new design analysis perspective allows designs to be quickly and intuitively analyzed
  - Both performance and resource metrics can be reviewed in an inter-active graphical environment
  - Cross-linked windows on register-transfer level (RTL) structure and scheduled operations can be cross-referenced with the C source and HDL output allowing hot-spots to be identified and optimized
- The synthesis report has been enhanced to be more intuitive and provide more design level details for latency and initiation interval
- Designs packaged as IP for System Generator for DSP will simulate faster

    - A cycle accurate C model is now provided as part of the IP package and automatically used for simulation in System Generator for DSP
- Packaging IP now generates a project file which can be directly opened in the Vivado Design Suite
- Assertions on variable ranges in the C sourced code are now supported for C synthesis, enabling more optimal hardware to be created
- AXI4 Master, Lite and Stream interfaces are now supported on SystemC designs
- Arrays in the top-level function argument list can now be synthesized with an `ap_bus` I/O protocol allowing them to be implemented as an AXI4 Master interface

### System Generator for DSP

- Support is now provided for the auto-migration of versioned IP, allowing existing designs to be quickly updated to the latest release
- Faster compile and netlist generation times are realized by the auto-propagation of device and interface parameters
- Faster simulation times are optionally available for IP created by the Vivado HLS tool
    - The simulation can use the RTL model or optionally use a faster cycle-accurate C model of the Vivado HLS IP

## Vivado Design Edition Tools

### Interactive Design Environment

- Support for bottom-up synthesis
- Basic support for module analysis flow
- Enhanced run "hook" scripts
    - Allows customization in run flows
- Find infrastructure now issues Tcl commands
    - Improves search – and learning how to use Tcl
- Schematic Editor combines vector instances
    - Simplifies schematics for busses
- Graphical User Interface (GUI) object references update to be consistent with Tcl objects
- Vivado device editor
    - Ability to start from either destination or source in manual routing mode

- Design Rule Checks (DRC)
  - New RTL and netlist linting checks
- Bitstream Generation
  - Ability to set bitstream and other device properties in all netlist views
  - Automatically sets default settings when added
  - Constraints can be saved to target Xilinx Design Constraints (XDC)
- Language Templates
  - SystemVerilog for Design constructs added
- Enhanced BlockRAM inference templates

### Power

- Lower dynamic power consumption out-of-the-box with no performance impact
  - Power optimization enabled in `opt_design` lower Block RAM dynamic power by ~40% and Core dynamic power by ~7.5%
  - Power opt design will provide incremental power saving with additional BRAM and sequential logic optimizations

### Vivado IP Integrator

To accelerate the creation of highly integrated, complex designs in All Programmable FPGA devices, Xilinx introduces the early access release of the Vivado IP integrator. Vivado's IP integrator builds on the foundation of Vivado's extensible IP catalog and standards based approach to packaging IP to deliver intelligent correct-by-construction assembly of designs co-optimized with Xilinx All Programmable solutions. The Vivado IP integrator environment is a licensed early access feature in the 2013.1 release. Contact your field applications engineer to obtain a license.

### Vivado Logic Simulation

- New driver reporting capability added to Vivado simulator which enables users to trace current driving values for a signal type HDL object
- Aldec Active-HDL support enabled in `compile_simlib`

### Xilinx Intellectual Property Simulation

Behavioral simulation of Xilinx IP is now supported in the following simulators:

- Full support
  - Mentor-Graphics: ModelSim and Questa Advanced Simulator

    - Xilinx: Vivado Simulator
- Limited support
    - Aldec: Active-HDL, Riveria-Pro
    - Cadence: Incisive Enterprise Simulator
    - Synopsys: VCS and VCS MX

***Note:*** The phrase "Limited support" means Xilinx has encrypted our IP with the IEEE P1735 V1 public keys for the listed vendors, but testing has been limited to ensuring the listed simulators can decrypt the IP. Testing for "limited support" vendors has not verified that all Xilinx IP cores will fully function in each simulator. The phrase "Full support" means listed simulators have been tested both for decryption and simulation functionality of Xilinx IP cores.

## Vivado HDL Synthesis

- Reduced LUT utilization (by 11%) by default with the ability to leverage both outputs of the 7 series LUT (controllable via a new **`-no_lc`** option)
- **Synthesis Settings** in the user interface now includes a runtime optimized strategy preset
- New **`-directive`** option to replace **`-effort_level`** for shorter runtimes
- New Design Rule Checks (DRC) in elaborated design view
    - Missed RAM templates, clocking, and more
- New resource sharing option for arithmetic operators (**`-resource_sharing`**) to explore advanced area/performance tradeoffs
- Control set optimization option (**`-control_set_opt_threshold`**) to eliminate low `fanout` control signals (clock enables or synchronous set/reset) and possibly obtain higher slice utilization after implementation

## Vivado Implementation

- New **`-directive`** option to replace **`-effort_level`** for shorter runtimes and greater control.
- New and improved implementation strategies offer a variety of implementation approaches.

## Static Timing Analysis

- Generate a report of timing exceptions using report exceptions
- Spread spectrum support
- Simplified source synchronous XDC templates
- Rounding (1ps) user inputs to avoid unexpandable clocks
- Accounting of setup/hold requirements consistent with industry standard tools

- Enabling clock properties at output ports to enable phase support for Simultaneous Switching Noise (SSN)
- Improved check_timing to filter out objects whose connections do not have timing checks

## Vivado I/O Planner

- Added SSN phase support
  - Up to 20% more margin achieved with phase information
- New device constraints view added to enable easy editing of DCI_CASCADE and Intern_Vref constraint
- Enhanced software check for board design
  - Tie off information will be provided based on CFGBVS settings

## Messaging

- Better message quality
- Advanced control of messages in Vivado Integrated Design Environment (IDE)
  - Suppression - Hide specific messages, all messages with same ID or a particular string
  - Severity adjustment - Upgrade or downgrade severity of messages as needed

## Vivado Debug

- Faster debug and programming
  - Flexibility and performance for programming cable via Target Communication Framework (TCF)
- Easier to use interface
  - Easily identify and probe debug nets in enhanced net-centric Debug Window
  - Compare simultaneous ILA waveforms
  - Cascade multiple ILA cores and trigger on external test equipment
  - Manual ICON instantiation no longer required – automatically infers
  - Cross-Trigger between Processing System (PS) and Programmable Logic (PL) for Zynq-7000 devices

## Integrated Vivado Serial I/O Analyzer

- Supports IBERT 7 series GTX, GTH, GTP in IP Catalog

## Device Programming Capabilities

- Connect to JTAG cable and query the device chain
- Directly program a Xilinx 7 series FPGA device with a BIT file
- Check the various status registers of Xilinx 7 series FPGA devices

***Note:*** For all other capabilities offered by Xilinx ISE Lab Tools and Xilinx ISE Design Suite, you will need to install the standalone version of the Xilinx ISE Lab Tools

# Important Information

## Migrating Vivado Designs to Vivado Design Suite 2013.1

*Table 6-1:* **Specifics for Migrating Vivado Designs to Vivado Design Suite 2013.1**

| Change in 2013.1 | Impact on Designs | Resolution |
|---|---|---|
| ISE Design Suite and Vivado Design Suite are now installed individually. Unlike the previous combined installer, the new Vivado installer does not include the iMPACT and ChipScope™ Pro Analyzer tools. | The installation of the ISE and Vivado Design Suites must now be managed and accessed individually. There should be no impact on most existing designs.<br>The exceptions will be designs using the legacy ChipScope debug cores (ICONv1.06a, ILA v1.05a, VIO v1.05a, ChipScope AXI Monitor) including the following Vivado IP cores and Vivado IP example designs:<br>Vivado IP cores:<br>• Memory Interface Generator (MIG) 7 Series<br>• Soft Error Mitigation (SEM) IP core<br>Vivado IP example designs:<br>• Common Packet Radio Interface (CPRI™) IP core<br>• JESD2024 IP core | The ISE Design Suite or the ISE Lab Tools 14.5 must be installed and accessible in order to use ChipScope. |
| To address usability and intuitive hierarchy, connectivity IP in Vivado Design Suite is delivered as a core block with encrypted HDL and GT instance. | As the IP is updated to the 2013.1 version, interface port mismatches may appear.<br>IPs affected:<br>• QSGMII<br>• JESD204<br>• 10G PCS/PMA<br>• 10G EMAC<br>• RXAUI<br>• XAUI | Top-level design changes are required and interface ports must be changed to match the latest port names and widths.<br>For more information see:<br>• Answer Record 55077 |
| To aid clock and reset sharing among multiple IP instantiations, Xilinx IP has been redesigned to allow sharing of common clock and resets among multiple IP instances. | As the IP is updated to the 2013.1 version, interface port mismatches may appear.<br>IP affected:<br>• RXAUI in 2013.1 | The top-level design changes may be required and interface ports must be changed to match the latest port names and widths.<br>For more information see:<br>• Answer Record 55078 |

*Table 6-1:* **Specifics for Migrating Vivado Designs to Vivado Design Suite 2013.1**

| Change in 2013.1 | Impact on Designs | Resolution |
|---|---|---|
| To aid IP debugging, Xilinx IP has been redesigned to bring transceiver debug ports to the top level. | As the IP is updated to the 2013.1 version, interface port mismatches may appear.<br>IP affected:<br>• RXAUI in 2013.1 | The top-level design interface ports must be changed to match the latest port names and widths. See Answer Record 55079 |
| To drive consistency across Xilinx IP, mixed case signal names have been changed to use all lower case for all VHDL and Verilog-based Xilinx cores. | As the IP is updated to the 2013.1 version, interface port name mismatches may appear. Below are a few examples of IPs that will be affected by this change. However, this mismatch may occur with any Xilinx IP in the 2013.1 version.<br>Sampling of IPs affected:<br>• Aurora 8B/10B<br>• Aurora 64B/66B<br>• AXI Perf. Monitor<br>• Clocking Wizard<br>• SelectIO™ Wizard<br>• XADC Wizard<br>• PCIe® Gen2/Gen3 | The top-level design interface ports must be changed to match the latest port names.<br>For more information see:<br>• Aurora 8B/10B: Answer Record 55006<br>• Aurora 64B/66B: Answer Record 55005<br>• AXI Memory Mapped to PCIe: Answer Record 55086<br>• Select IO Wizard: Answer Record 55001<br>• XADC Wizard: Answer Record 54997<br>• 7 Series PCIe: Answer Record 55084<br>• Virtex-7 PCIe Gen3: Answer Record 55085 |
| Xilinx IP in Vivado Design Suite will now have different version numbers than their ISE Design Suite counterparts. All Xilinx IP in Vivado Design Suite has moved to a new version for 2013.1. | All Xilinx IP in Vivado Design Suite has moved to a new version for 2013.1. Customers using older versions of IP may choose to remain with the older version or upgrade to a new version of IP. | Upgrading to new IP version requires changes to IP instantiations in design. |
| To ensure the correct operation of the **Save Constraints** command, strict checking is now applied to XDC files to look for unsupported Tcl commands. | As a result of this change, XDC files that worked in 2012.4 and earlier releases may return a critical warning message when the XDC file is loaded. | The Vivado Design Suite now offers the ability to add "un-managed" Tcl files as design sources in constraints sets. For more information refer to Vivado XDC Changes, page 72, or to Answer Record 54842. |
| Vivado Synthesis and Implementation -effort directives have been replaced. | The corresponding replacement directives will be mapped when runs are launched. | Rerun with the latest directives and strategies. |
| XST is no longer recommended for new Vivado designs, and is hidden by default. XST strategies are no longer available in the Synthesis Settings dialogue box, but are still available through Tcl commands. | None. Designs with existing XST strategies assigned will continue to run. Xilinx IP in the Vivado Design Suite is created and validated using Vivado synthesis. Some IP with constraints may issue errors or warnings. | Select a Vivado synthesis strategy instead of XST. |

## Vivado XDC Changes

XDC constraint files are actively managed in the project by the Vivado Design Suite, which writes constraints to the XDC files to capture user design changes from operations like floorplanning, physical placement, and timing constraints edited in the Vivado IDE. When you select the **File > Save Constraints** or **File > Save Constraints As...** command, the Vivado tool saves constraints to the XDC file – replacing the original constraint for modified constraints, or adding it to the end of the target constraints file for new constraints. The commands that are supported in XDC files have always been a subset of all the Vivado commands and the Tcl built-ins. XDC files do not support string list manipulation commands, procedures, or elaborate looping and conditionals in XDC files because the Vivado tool is operating on a fully-expanded "in-memory" view of these constraints applied to the design, and the tool would not be able to robustly manage and save constraints using these constructs. The list of commands which are allowed in standard XDC files is documented in Answer Record 54842: http://www.xilinx.com/support/answers/54842.htm.

Starting in 2013.1, the Vivado Design Suite performs additional checks looking in the XDC files for unsupported Tcl commands. When unsupported Tcl commands are found, the Vivado tool returns a critical warning such as:

```
"CRITICAL WARNING: [Designutils 20-1307] Command 'lappend', 'lindex', 'lsort', or
'concat' is not supported in the xdc constraint file ...".
```

However, in 2013.1, to let you use some of the advanced features of Tcl, such as list manipulation and looping, as design constraints in your project, the Vivado Design Suite provides a new feature called an "un-managed" Tcl source file. This feature lets you specify a Tcl command file as a source for design constraints in a constraint set. In addition, the script-based project-less flow has always allowed sourcing Tcl command files as general Tcl scripts at different design stages, for example after opening a post-synthesis linked design. Un-managed Tcl allows elaborate Tcl scripts to apply design constraints, but does not support the **File > Save Constraints** command to write design changes back to the source files. In this case the Tcl source file is un-managed.

## Vivado High-Level Synthesis

- The term *throughput* has been changed to *Initiation Interval* or *Interval* throughout the documentation
  - This has been done to avoid confusion with design throughput which is expressed in terms of clock cycle per second
- Floating-point designs verified by ModelSim in the RTL co-simulation flow must use libraries
  - The libraries must be compiled by the users for the particular version of ModelSim being used

  ***Note:*** Details on how to perform this are provided in the documentation

- There is no longer a requirement to differentiate SystemC design and C/C++ designs, the **-type** option to the **add_files** command has been removed

## Vivado IP Versioning Changes

- The version format and strategy will be unified across all Xilinx IP
  - The format will be Major.Minor (Revision)
    - Major - major interface change and behavior changes
    - Minor – small behavior or interface changes (one or two ports change)
    - Revision – no behavior changes
  - All IP references will be based on the Major.Minor fields only
- Only the latest version of a given IP can be generated from the IP catalog
  - Older versions will no longer be available
  - Existing output products from older versions, which already exist on disk can always be re-used
  - Modifications or generation of a removed IP will require the IP to be upgraded first

## Updates to Existing IP

- Aurora 64B/66B (v8_0)
  - GTH support & hardware (HW) validation
  - Vivado only Core (Legacy Free)
  - Lower case to ports
  - Native Vivado simulator/MTI support
- Aurora 8B/10B (v9_0)
  - GTP/GTH support & HW validation
  - Vivado only Core (Legacy Free)
  - Lower case to ports
  - Native Vivado simulator/MTI support
- PCI Express® Gen3/Gen2
  - Updated GT wrappers
  - Inter-processor interrupt (
  - IPI) Level 0 support
  - Added Root Port support

- Added support for Zynq 7030 and 7045 devices
- 10G Ethernet MAC
  - New hierarchy structure
  - Separate XDC files for core and example design
- XAUI
  - New hierarchy structure
  - Separate XDC files for core and example design
  - Updated GTP and GTH transceiver files
- RXAUI
  - New hierarchy structure and clocking and reset modules
  - Separate XDC files for core and example design
  - Updated GTP transceiver files
- 10G Ethernet PCS/PMA (10GBASE-R/10GBASE-KR)
  - New hierarchy structure and clocking and reset modules
  - Separate XDC files for core and example design
  - Updated GTX and GTH transceiver files
  - Tri-Mode Ethernet MAC
  - Kintex-7 production
- 1000BASE-X/SGMII
  - Updated GTP and GTH transceiver files
- QSGMII
  - Updated GTP transceiver files
- GMII to RGMII
  - Updated auto-negotiation logic
- AXI Ethernet
  - IP Integrator support for 7 series and Zynq-7000
- SPI-4.2
  - Virtex-7 production
- PCI32 and PCI64
  - Kintex-7 production
- For a detailed list of Xilinx IP Cores, see the *IP Release Notes Guide* (XTP025) [Ref 1]

# Known Issues

Vivado™ Design Suite Tools Known Issues can be found at Answer Record 5512

XILINX

*Appendix A*

# Additional Resources

## Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx® Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

## Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

## Xilinx Documentation Navigator

You can view Xilinx tool and hardware documentation in the Xilinx Documentation Navigator or on the Xilinx website. The Documentation Navigator is integrated with the Vivado™ Design Suite and it provides a catalog of Xilinx documentation and videos.

For more information about the Documentation Navigator, see the *Vivado Design Suite User Guide: Getting Started* (UG910).

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To view the Xilinx design tools license details and EULA, see http://www.xilinx.com/cgi-bin/docs/rdoc?v=2013.2;d=end-user-license-agreement.pdf.

# References

1. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
2. *IP Release Notes Guide* (XTP025)
3. *USB Cable Installation Guide* (UG344)
4. *Platform Cable USB II Data Sheet* (DS593)
5. *Parallel Cable IV Data Sheet* (DS097)
6. Xilinx Download Center (http://www.xilinx.com/support/download/index.htm)
7. Xilinx Design Tools WebTalk page (http://www.origin.xilinx.com/ise/webtalk/)
8. *Vivado Design Suite Video Tutorials* (http://www.xilinx.com/training/vivado/index.htm)
9. *Vivado Design Suite Documentation* (www.xilinx.com/support/documentation/dt_vivado2013-1.htm)