XA Zynq®-7000 All Programmable SoC

XILINX.

	Device Name	Z-7010		Z-7020		Z-7030
	Part Number	XA7Z010		XA7Z020		XA7Z030
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™				
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor				
	Maximum Frequency	667 MHz				
	L1 Cache	32 KB Instruction, 32 KB Data per processor				
	L2 Cache	512 KB				
	On-Chip Memory	256 KB				
	External Memory Support (1)	DDR3, DDR3L, DDR2, LPDDR2				
	External Static Memory Support (1)	2x Quad-SPI, NAND, NOR				
	DMA Channels	8 (4 dedicated to Programmable Logic)				
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	Peripherals w/ built-in DMA(1)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO				
	Security(2)	AES and SHA 256b Decryption and Authentication for Secure Boot				
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts				
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA		Artix®-7 FPGA		Kintex®-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates(3))	28K Logic Cells (~430K)		85K Logic Cells (~1.3M)		125K Logic Cells (~1.9M)
	Look-Up Tables (LUTs)	17,600		53,200		78,600
	Flip-Flops	35,200		106,400		157,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)		560 KB (140)		1,060 KB (265)
	Programmable DSP Slices (18x25 MACCs)	80		220		400
	Peak DSP Performance (Symmetric FIR)	74 GMACs		204 GMACs		593 GMACs
	PCI Express® (Root Complex and End Point)	–		–		Gen2 x4
	Analog Mixed Signal (AMS) / XADC(1)	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs				
	Security(2)	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration				
Speed Grades	XA I-Grade (–40°C to 100°C)	-1				
	XA Q-Grade (–40°C to 125°C)	-1				
Packages	Package Type(4)	**CLG225(1)**	**CLG400**	**CLG400**	**CLG484**	**FBG484 / FBV484**
	Size (mm)	13x13	17x17	17x17	19x19	23x23
	Pitch (mm)	0.8	0.8	0.8	0.8	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os)(5)	32	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	125	200	100
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	–	–	–	–	63
	Serial Transceivers	–	–	–	–	4
	Maximum Transceiver Speed (Speed Grade Dependent)	NA	NA	NA	NA	6.6 Gb/s

XMP088 (v1.3)

Notes:
1. Z-7010 in CLG225 has restrictions on PS peripherals, Memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
2. Security block is shared by the Processing System and the Programmable Logic.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
4. Devices in the same package are pin-to-pin compatible.
5. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.
6. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.