SECURITY MONITOR IP CORE

SECURITY MONITOR IP

Industry-Leading Programmable Logic Device Security Protecting IP and Mission Critical Data

Defense contractors and government agencies must address secure, complex specifications to deliver solutions with Information Assurance (IA) and Anti-Tamper (AT) support. In commercial markets, solution providers put high priority on safeguarding their business-critical on-device intellectual property.

An exportable[1] security solution, the Xilinx® Security Monitor (SecMon) IP, meets security needs for both defense and commercial projects. The fully autonomous soft core continuously monitors for signs of post-configuration tampering and can carry out penalties that render designs inaccessible. The 8th generation[2] technology is proven and mature.

Xilinx Solution Highlights

- Protection level helping customers meet the stringent design requirements of secure Aerospace and Defense products as instructed by DoD 5200.39
- Commercially viable and exportable solution to safeguard on-device IP
- Mature, proven technology now in its 8th generation[2]
- Autonomous and self-contained; does not require off-chip control or support (e.g., no need to load external bitstream during zeroization)
- Extensive monitoring functions: integrity of configuration memory, environmental conditions, JTAG status and more
- Partial Reconfiguration Support / Monitoring
- User-customizable penalties and automatic tamper responses to attempted attacks or “hackers”
- Easy design integration (fully place-and-routed design file delivered in the innovative Qualified Bitstream Flow for all available device families through Kintex® & Virtex® UltraScale® devices – source code for Zynq® UltraScale+™ SoC devices)

Post-Configuration Security

The SecMon IP core operates completely independent within an FPGA/SoC design to augment existing silicon security features with post-configuration Anti-Tamper protection. The power draw (60mW, worst case) and resource impact (approximately 1% to 8% on the largest to smallest supported FPGA/SoC) are minimal.

1 Xilinx SecMon IP has been approved by the U.S. Department of State for export (January, 2012).
2 Available for Virtex-5, Spartan®-6, Virtex-6 and 7-Series, Kintex and Virtex UltraScale, and Zynq UltraScale+ MPSoC and RFSoC & Zynq SoC families today. Contact your local Xilinx FAE for details.

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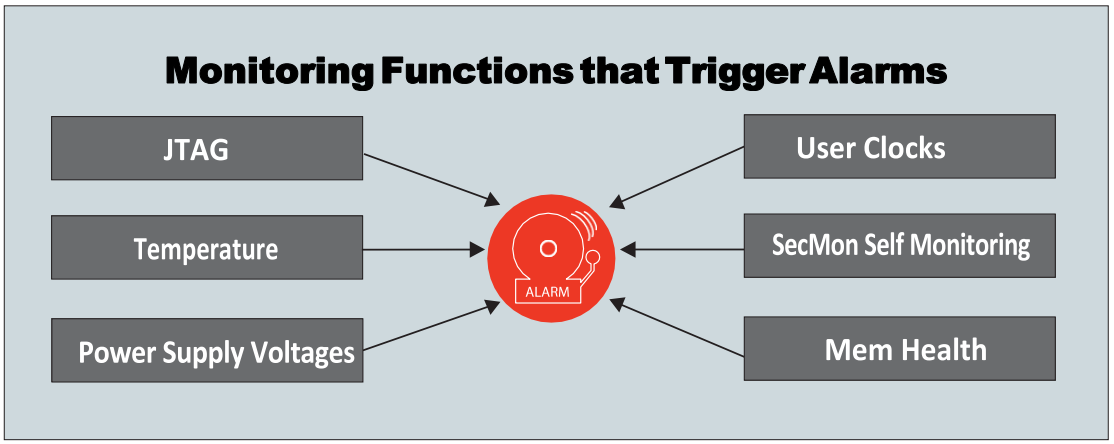

Autonomous Monitoring

- Configuration Memory Integrity
- JTAG Activity
- Temperature and Voltage
- User Clocks
- Partial reconfiguration
- Self-monitoring
- Security Critical Register Monitoring
- Processor System Memory Health in Zynq UltraScale+ SoC devices

Configurable Penalties

- Zeroization of FPGA Configuration Memory
- Zeroization of PS Memories and Secure Lockdown in Zynq UltraScale+ SoC
- Zeroization of AES Bitstream Key
- Global 3-State
- Global Set/Reset

System Extensibility

- Penalties can be asserted due to off-chip events at the system level
- Alarm limits (e.g. temperature and voltage) are user-configurable; Programmable alarm responses with delays for accommodating related "housecleaning" events
- Custom tamper conditions (monitor system loops, voltage, etc., via analog input pins)
- UltraScale-based SecMon IP allows multiple SecMon IP cores to be connected together to act as a single functional anti-tamper unit. This provides a solution for both board level (device-to-device) and stacked silicon interconnect (SSI) devices with multiple instances of the SecMon IP.

Revolutionary Delivery Innovations

Delivered as a fully place-and-routed design file for all available device families through Kintex and Virtex UltraScale, the SecMon IP allows developers to import Anti-Tamper capabilities into designs with much shorter customer verification and certification times. Xilinx also offers an industry-first automated Bitstream comparison capability for customers that require maximum verification of the integrated security solution. The Xilinx Qualified Bitstream Flow speeds time to market and can save customers thousands of hours of engineering design and verification effort while upholding strict quality standards.

Delivered as both software and HDL source code, Zynq UltraScale+ SoC Security Monitor is easily integrated using the standard Xilinx tool flows while expanding the provided protection to include the entire Processor System and Programmable Logic. A full documentation suite, including integration instructions, user guide, test plan, and test software, speeds time to market.

Take the NEXT STEP

For more information about Xilinx SecMon IP supported devices and availability, please contact your Xilinx sales representative or a local Xilinx office.

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