LogiCORE IP Slice (v1.0)

PB042 (v1.0) April 6, 2016 **Product Brief**

Introduction

The Slice IP core is used to rip bits off a bus net. Often there is a need to rip some bits off a wide bus net. This IP core can be instantiated to accomplish this purpose.

Additional Information

See the product page.

Features

- Configurable input bus width
- Configurable number of bits to be ripped off of the input bus

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™, UltraScale™, Zynq® -7000, Artix®-7, Virtex® -7, Kintex®-7
Supported User Interfaces	N/A
Provided with Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	N/A
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Figure 1 illustrates the Slice in a system.

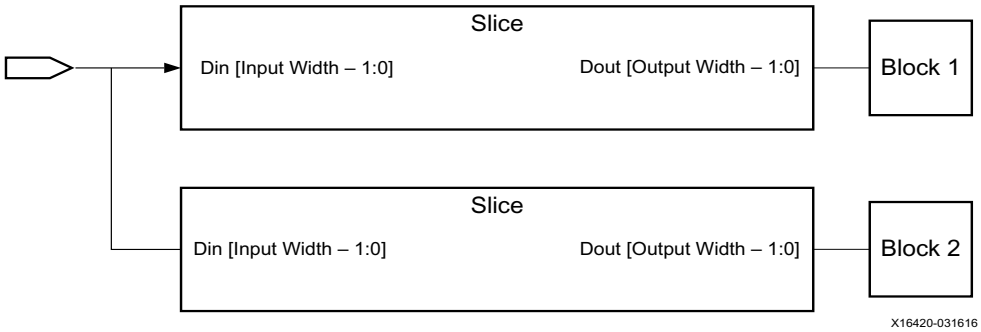

Figure 1: **Slice in a System**

Block Diagram

Figure 2: **Block Diagram**

Using Slice in a Block Design

In a block design you instantiate the Slice IP core by right clicking in the block design canvas and selecting **Add IP** from the context menu.

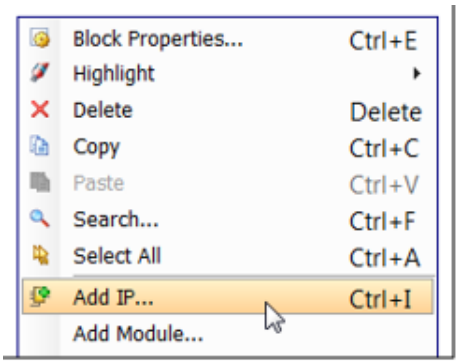

Figure 3: **Adding the Slice Block in the Block Design Canvas**

In the **Search** field of the IP catalog, type **Slice** and double-click the selection to instantiate it.

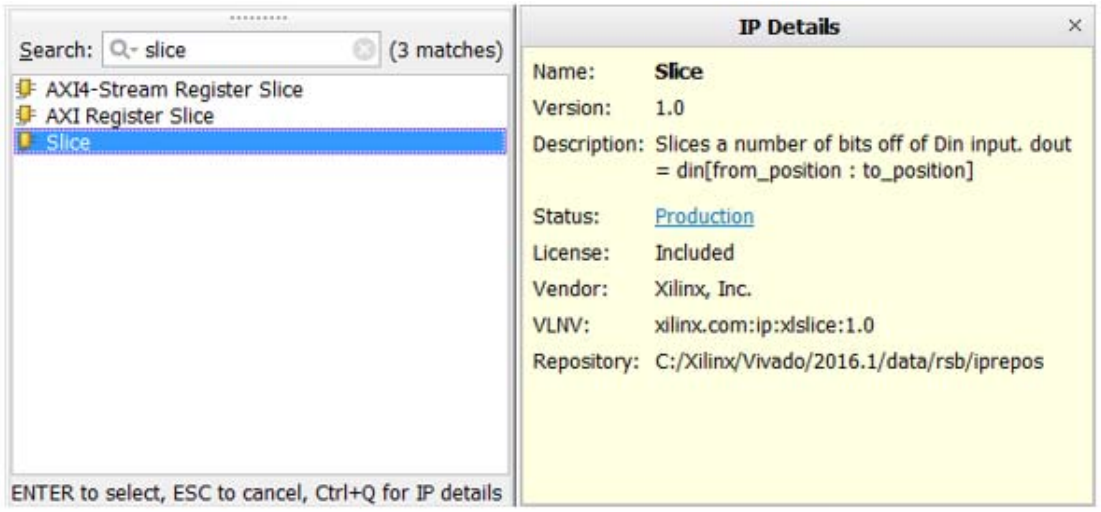

Figure 4: **Search the Slice IP in the IP Catalog and Instantiate**

This instantiates the Slice IP in the design as shown in Figure 5.

Figure 5: **Slice IP Before Customization**

Double-click the Slice block to open the Re-customize IP dialog box.

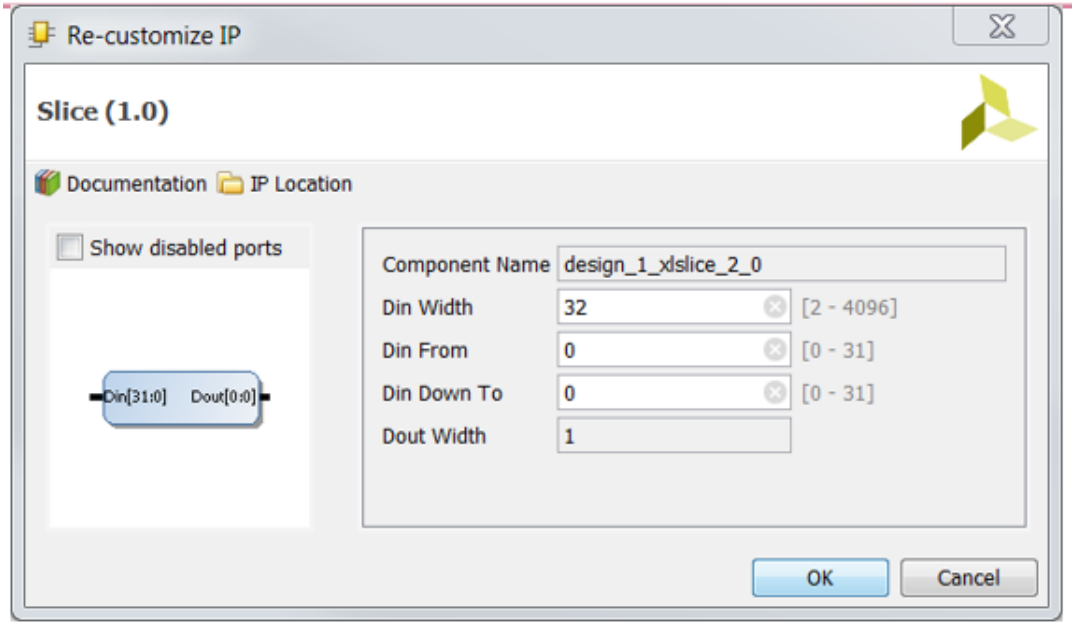

Figure 6: **Re-customize IP Dialog Box**

In Figure 6, set the **Din Width** parameter to the bit width of the input bus from where bits will be ripped off. Set the **Din From** parameter to the highest bit to be ripped and the **Din Down To** parameter to the lowest bit to be ripped. As an example, if you need to rip 12-bits from a 32-bit input bus and those bits are 11 through 0, you would set the **Din Width** to 32, **Din From** to 11 and **Din Down To** to 0. If only single-bit widths are needed to be ripped, set the **Din From** and **Din Down To** both to the same value. For example, if the fifth bit needs to be ripped, set **Din From** to 5 and **Din Down To** to 5 as well.

I/O Signals

The I/O signals are listed and described in Table 1.

Table 1: **I/O Signals**

Port Name	Description
Din[Input Width – 1: 0]	This is the input bus.
Dout [Output Width – 1: 0]	This is the vectored output bus or a single bit output which is based on the number of bits to be ripped.

Design Parameters

The parameters are listed and described in Table 2.

Table 2: **Design Parameters**

Parameter	Description	Type
Din Width	Bit width of the input bus.	Integer
Din From	Highest bit to be ripped.	Integer
Din Down To	Lowest bit to be ripped.	Integer
Dout Width	This value is auto-calculated based on the number of bits to be ripped and represents the output bus width of the output port Dout.	Integer

Design Implementation

Design Tools

Note: This IP can only be used in the Vivado® IP integrator. It is not designed to be used in an RTL-only design flow within the Vivado Design Suite.

HDL file is provided during generation in the Vivado IP integrator.

Target Technology

The target technologies are UltraScale+™, UltraScale™, Zynq®-7000, and 7 series devices.

Device Utilization and Performance Benchmarks

Using this block in the block design will not incur any resource usage of the FPGA.

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

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Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/06/2016	1.0	Initial Xilinx release.

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