LogiCORE IP Concat (v2.1)

PB041 (v2.1) April 6, 2016 **Product Brief**

Introduction

The Concat IP core is used for concatenating bus signals of varying widths.

Additional Information

See the product page.

Features

- Configurable number of ports
- Configurable bit width of each port

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™, UltraScale™, Zynq® -7000, Artix®-7, Virtex® -7, Kintex®-7
Supported User Interfaces	N/A
Provided with Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	N/A
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

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Overview

The Concat IP core provides a mechanism to combine bus signals of varying width into a single bus.

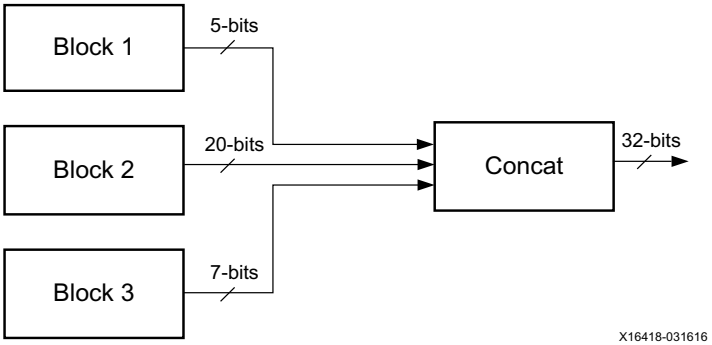

Figure 1: **Concat IP in a System**

Block Diagram

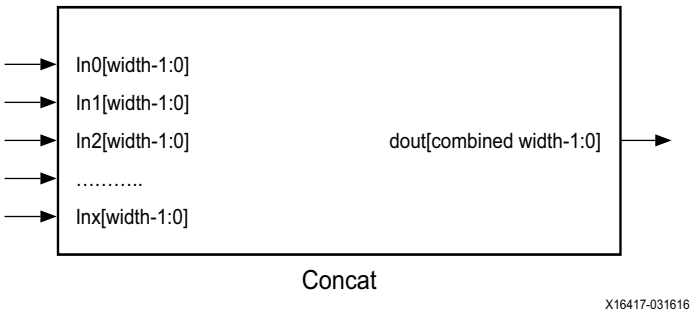

Figure 2: **Block Diagram**

Using Concat in a Block Design

In a block design you instantiate the Concat IP core by right clicking in the block design canvas and selecting **Add IP** from the context menu.

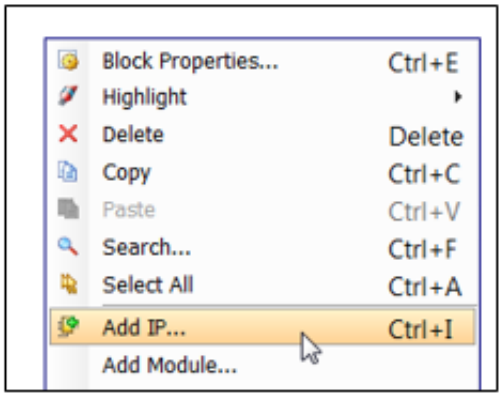

Figure 3: **Adding the Concat Block in the Block Design Canvas**

In the Search field of the IP Catalog, type **Concat** and double-click the Concat IP core to instantiate it.

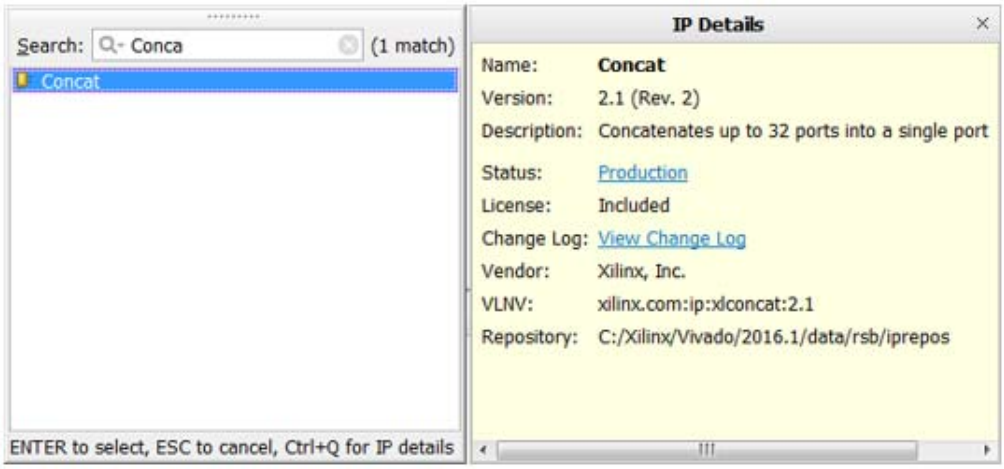

Figure 4: **Search the Concat IP Core in the IP Catalog and instantiate**

This instantiates the Concat IP core in the design as shown in Figure 5.

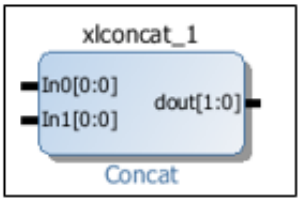

Figure 5: **Concat IP Before Customization**

Double-click the Concat block to open the Re-Customize IP dialog box.

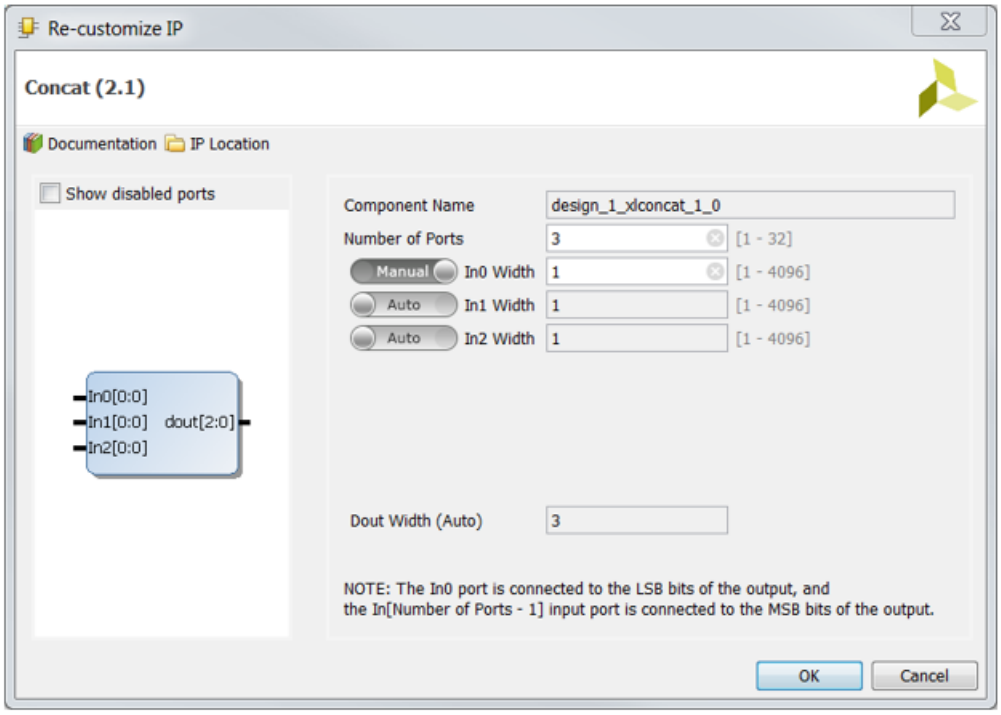

Figure 6: **Re-customize IP Dialog Box**

In Figure 6, set the **Number of Ports** parameter to the number of input ports desired. To set the bit width of an input port, toggle the button to the left of the **Inx Width** field to **Manual** which makes the **Inx Width** field editable. Enter the bit width in the field. The output bit width is the combined bit widths of all the input ports and is shown in the **Dout Width** field.

I/O Signals

The I/O signals are listed and described in Table 1.

Table 1: **I/O Signals**

Port Name	Description
Inx[width-1:0]	Input bus with variable width. The number of input ports depends on the Number of Ports parameter. The “width” can be set to the desired number of bits.
dout[combined width – 1 : 0]	dout is the output port whose bit width equals the combined bit widths of all the input ports.

Design Parameters

The parameters are listed and described in Table 2.

Table 2: **Design Parameters**

Parameter	Description	Type
Number of Ports	Number of Input ports desired.	Integer

Design Implementation

Design Tools

Note: This IP can only be used in Vivado® IP integrator. It is not designed to be used in an RTL-only design flow within the Vivado Design Suite.

HDL file is provided during generation in the Vivado IP integrator.

Target Technology

The target technologies are UltraScale+™, UltraScale™, Zynq®-7000, and 7 series devices.

Device Utilization and Performance Benchmarks

Using this block in the block design will not incur any resource usage of the FPGA.

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

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Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/06/2016	2.1	Initial Xilinx Release.

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