UHD SDI Audio v2.0

LogiCORE IP Product Guide

Vivado Design Suite

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Introduction

The Xilinx® UHD SDI Audio core is configurable as an audio embedder or an audio extractor. When configured as an audio embedder, the core can embed of up to 32 channels of AES3 audio data over an AXI4-Stream audio interface onto an SDI stream. Similarly, when configured as an audio extractor, the core can extract up to 32 channels of audio data from the incoming SDI stream and output them in AES3 format on an AXI4-Stream audio interface. In both the configurations, the core supports multiple audio sample rates (32 kHz, 44.1 kHz, and 48 kHz).

It is designed in accordance with SMPTE ST 272 for SD-SDI, SMPTE ST 299-1 for HD-SDI and SMPTE ST 299-1 and 2 for 3G/6G/12G-SDI. This IP includes standard bus interfaces to the AMBA® AXI4-Lite and AXI4-Stream interfaces, allowing for easier integration of the IP with other Audio Interface IPs for further processing of audio data.

Features

- Supports up to 32 channels of audio.
- 20/24-bit audio at multiple sample rates (32 kHz, 44.1 kHz and 48 kHz).
- Synchronous and asynchronous audio support.
- Supports 192-bit AES3 channel status extraction.
- Reports the presence and status of audio groups on the incoming SDI stream.
- AXI4-Stream interface to carry audio samples in AES3 format.
- AXI4-Lite and port based interface for configuration of the core.

IP Facts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Versal® ACAP, UltraScale+™Families, Zynq® UltraScale+™ MPSoC, Kintex UltraScale, Virtex® UltraScale™, 7 series,[2] Zynq®-7000 SoC
Supported User Interfaces	AXI4-Stream, AXI4-Lite, and Native SDI
Resources	Performance and Resource Use web page
Provided with Core	
Design Files	Register Transfer Lever (RTL)
Example Design	Verilog
Test Bench	Not Provided
Constraints File	XDC
Simulation Model	Not Provided
Supported S/W Driver[2]	Standalone and Linux
Tested Design Flows[3]	
Design Entry	Vivado Design Suite
Simulation	For supported simulators, see the Xilinx® Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Release Notes and Known Issues	Master Answer Record: 70290.
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. Artix®-7 device is not supported.
3. Standalone driver details can be found in the Vitis™ directory (<install_directory>/vitis/<release>/data/embeddedsw/doc/xilinx_drivers.htm). Linux OS and driver support information is available from the Xilinx Wiki page.
4. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

XILINX

Chapter 2

Overview

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. All Versal® ACAP design process Design Hubs and the Design Flow Assistant materials can be found on the Xilinx.com website. This document covers the following design processes:

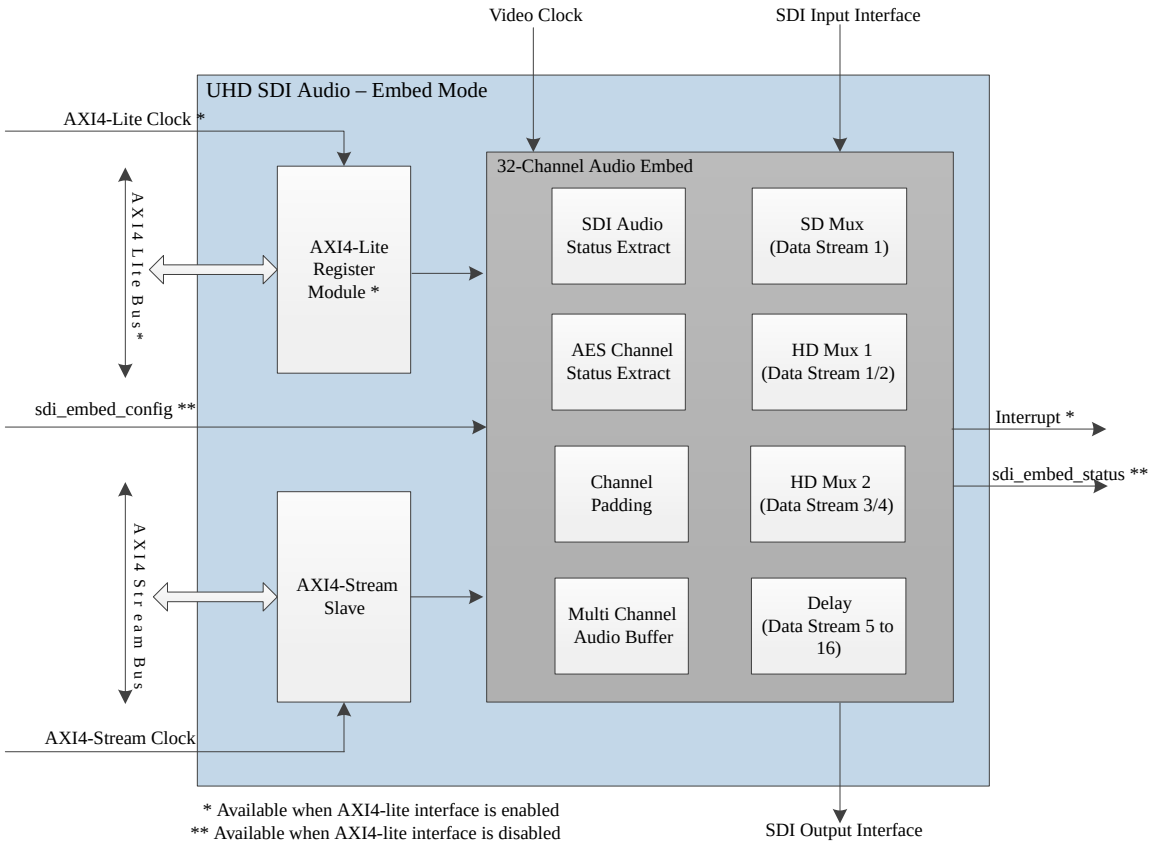
- **Hardware, IP, and Platform Development:** Creating the PL IP blocks for the hardware platform, creating PL kernels, functional simulation, and evaluating the Vivado® timing, resource use, and power closure. Also involves developing the hardware platform for system integration. Topics in this document that apply to this design process include:
  - Port Descriptions
  - Register Space
  - Clocking
  - Resets
  - Customizing and Generating the Core
  - Chapter 6: Example Design

Core Overview

The Xilinx® UHD-SDI Audio (Embed) receives audio data on AXI4-Stream interface, video data on SDI input interface and transmits audio embedded video data back to the SDI Transmitter on SDI output interface.

The following figure shows the top level block diagram of UHD-SDI Audio (Embed) in 32-channel configuration.

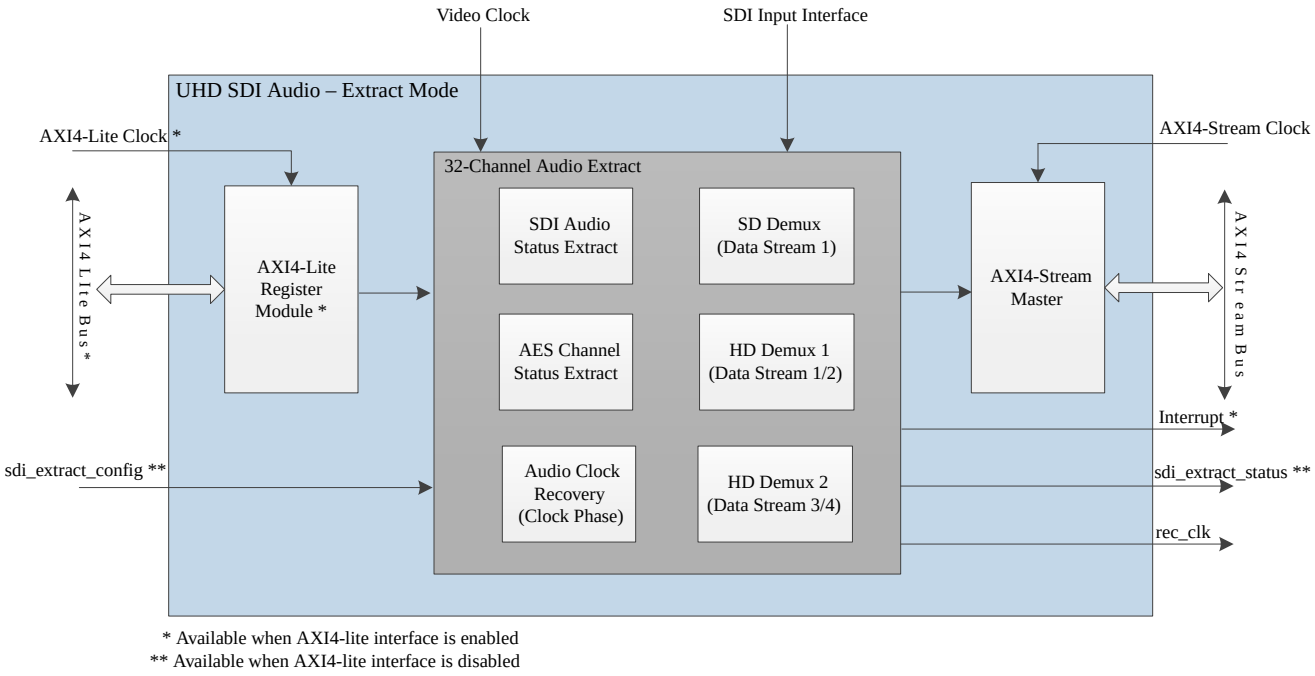
Figure 1: **Block Diagram of UHD-SDI Audio (Embed)**



The UHD-SDI Audio (Extract) receives audio embedded video data on SDI input interface and transmits audio data out on AXI4-Stream interface.

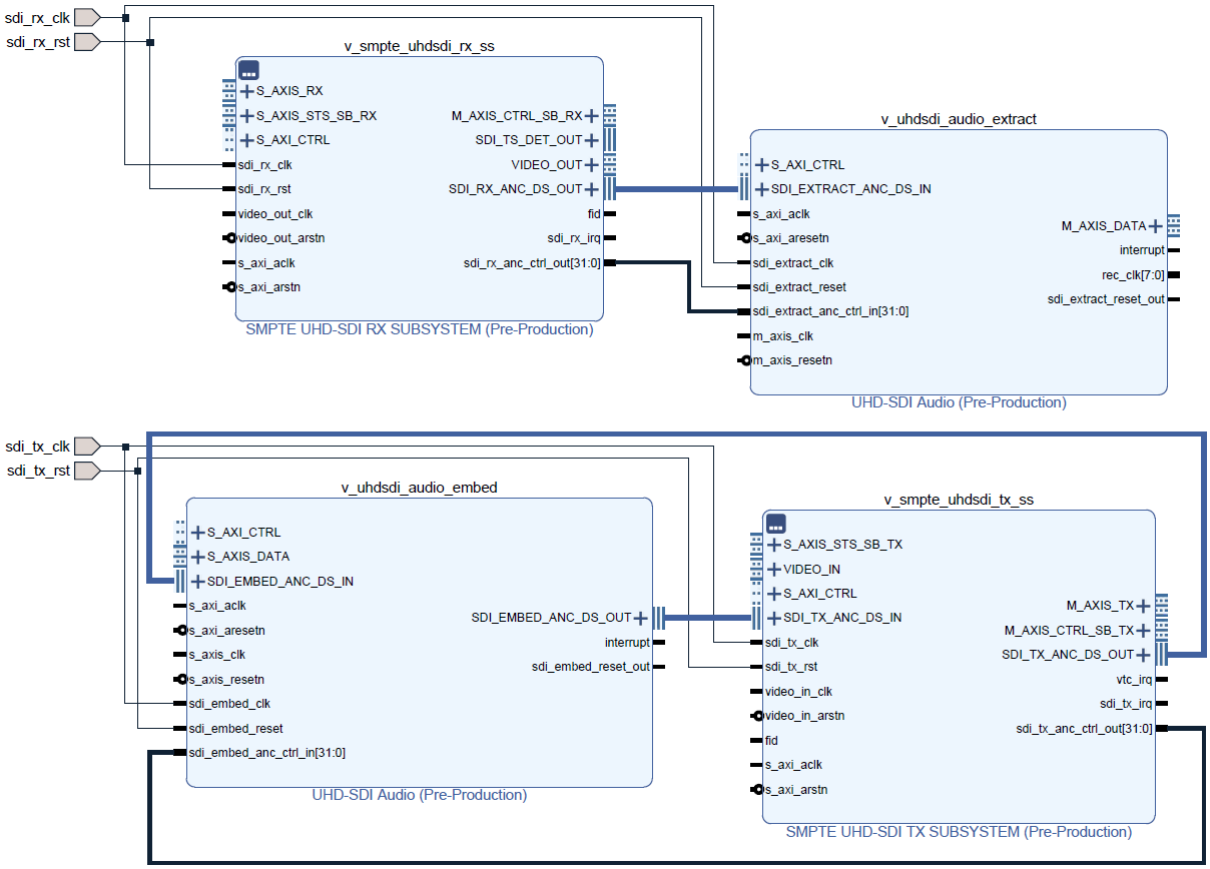
The following figure shows the top level block diagram of UHD-SDI Audio (Extract) in 32-channel configuration.

Figure 2: **Block Diagram of UHD-SDI Audio (Extract)**



The following figure highlights the interface between the Xilinx UHD-SDI TX Subsystem, UHD-SDI RX Subsystem and UHD-SDI Audio (Embed & Extract).

Figure 3: **Block Diagram of UHD-SDI TX/RX Subsystem with UHD-SDI Audio (Embed & Extract)**



Applications

- SDI Audio Embedding
- SDI Audio Extraction

Unsupported Features

- Audio sample rate of 96 KHz is not supported.
- The 16-way data stream interleaving (12G_SDI_16DS) is not supported when UHD-SDI Audio IP core is used with Xilinx® UHD SDI TX/RX subsystem.
- Except for SD-SDI mode, UHD-SDI Audio IP core does not accept or support Luma and CbCr data coming (multiplexed) on same data stream.
- In UHD-SDI Audio (Embed), audio frame number in control packet is always tied to 0 irrespective of synchronous or asynchronous audio.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

The UHD-SDI Audio IP core consists of the following sub-blocks in Embed mode:

- AXI4-Lite Slave (optional)
- AXI4-Stream Slave
- Audio Multiplexers
- Channel Padding (optional)
- SDI Audio Status Extract (optional)
- AES Channel Status Extract (optional)

The UHD-SDI Audio IP core consists of the following sub-blocks in Extract mode:

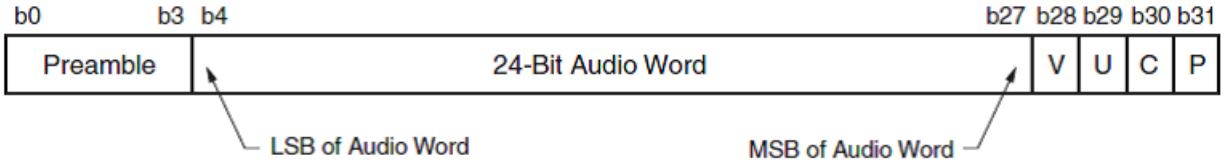
- AXI4-Lite Slave (optional)
- AXI4-Stream Master
- Audio De-Multiplexers
- Clock Phase Logic (optional)
- SDI Audio Status Extract (optional)
- AES Channel Status Extract (optional)

Sub blocks marked as optional has significant impact on the resource utilization of the IP. Based on the use case, optional blocks can be enabled or disabled during core generation.

AES3 Data Format

This section focuses on the standard two-channel PCM audio described in the AES3 specification.The basic data structure of AES3 is called a sub-frame. Each 32-bit sub-frame contains a single audio sample for one audio channel along with a few other bits of information as shown in the following figure. A sub-frame begins with a 4-bit preamble. The audio word can be either 24 bits or 20 bits. Following the audio word are the valid (V), user data (U), channel status (C), and parity (P) bits.

Figure 4: **AES3 Subframe Format with 24-Bit Audio Sample**



The preamble provides the start of the audio block (0x1) and audio channel information (0x2 - Channel 1 of pair and 0x3 - Channel 2 of pair). Bits[27:4] carry the audio data MSB bit at the 27th position and the LSB position is based on the audio sample length. Bit[28] provides the audio validity information. Bit[29] carries the user data information, and Bit[30] carries the channel status bit. Bit[31] is the even parity over 32 bits except for the preamble bits.

Two consecutive subframes, one for each of the two audio channels, form a complete frame. Frames are grouped together in blocks of 192 frames. This grouping of frames into blocks serves to define the beginning and ending points for the sequence of channel status and user data bits.

AXI4-Stream Audio Interface

The AXI4-Stream Audio Interface carries audio samples in AES3 format. The data width over the AXI4-Stream Audio Interface is fixed at 32 bits to carry one sub-frame as shown in the Figure 4: AES3 Subframe Format with 24-Bit Audio Sample. The TID indicates the channel number of the audio data (TID is 0 for channel 1 and TID is 31 for channel 32).

UHD-SDI Audio (Embed) uses TID to identify the group to which incoming audio need to be embedded. Similarly, UHD-SDI Audio (Extract) uses TID to convey the group from which audio is extracted. For example, to embed audio onto group 2, send the audio samples with TID 4, 5, 6, and 7 to the UHD-SDI Audio (Embed). Similarily, the audio extracted from group 4 is sent out with TID 12, 13, 14, and 15 by UHD-SDI Audio (Extract). The following table highlights the mapping of AXI4-Stream TID to audio groups and channels in a 32-channel system.

Table 1: **Mapping of AXI4-Stream TID in 32-Channel System**

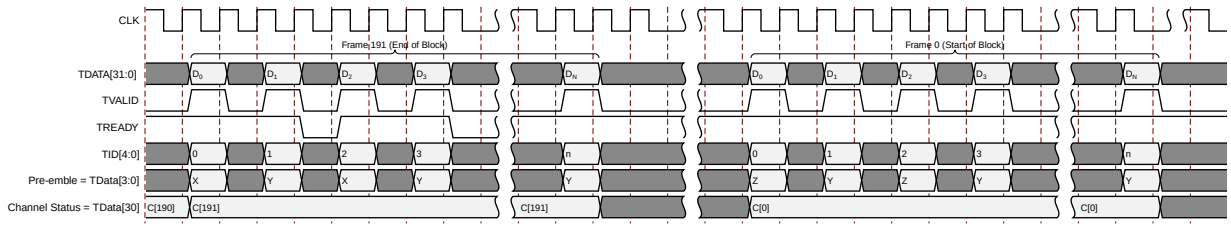
AXI4-Stream TID	Channel Number	SDI Audio Group	Channel Number in Group
0	1	1	1
1	2	1	2
2	3	1	3
3	4	1	4
4	5	2	1
5	6	2	2
6	7	2	3

Table 1: **Mapping of AXI4-Stream TID in 32-Channel System** *(cont'd)*

AXI4-Stream TID	Channel Number	SDI Audio Group	Channel Number in Group
7	8	2	4
8	9	3	1
9	10	3	2
10	11	3	3
11	12	3	4
12	13	4	1
13	14	4	2
14	15	4	3
15	16	4	4
16	17	5	1
17	18	5	2
18	19	5	3
19	20	5	4
20	21	6	1
21	22	6	2
22	23	6	3
23	24	6	4
24	25	7	1
25	26	7	2
26	27	7	3
27	28	7	4
28	29	8	1
29	30	8	2
30	31	8	3
31	32	8	4

The following figure highlights the frame structure and the block transition in multi-channel AXI4-Stream Audio Interface.

Figure 5: **Multi-Channel AXI4-Stream Audio Interface**



AXI4-Lite Slave

The AXI4-Lite Slave provides the read/write control logic to the core register set. The registers are accessible by the external AXI4-Lite master. The data width of the AXI4-Lite interface is fixed at 32 bits. The register set can be reset to default values by writing 0x1 to the soft reset register (offset - 0x04).

When AXI4-Lite interface is disabled, UHD-SDI Audio IP core accepts the configuration through `sdi_embed_config`/`sdi_extract_config` and conveys the status through `sdi_embed_status`/`sdi_extract_status` signals.

AXI4-Stream Slave

The audio interface to an UHD-SDI Audio (Embed) is a 32-bit AXI4-Stream slave bus. AXI4-Stream Slave generates the handshaking signal `s_axis_tready` after receiving the streaming data (`s_axis_tdata`), data valid signal (`s_axis_tvalid`), and channel number identification (`s_axis_tid`).

***Note*:** The UHD-SDI Audio (Embed) strictly expects audio samples to be distributed as per sample rate on the AXI4-Stream Interface. One audio sample per each channel in one period of audio clock (48 KHz, 44.1 KHz, 32 KHz).

Channel Padding Logic

Channel padding logic should be enabled when AXI4-Stream master interfacing with UHD-SDI Audio (Embed) is a non-multiple of four source. (Example 5.1 system generates 6 samples which is non-multiple of four. Similarly AES3/SPDIF generates two samples which is non multiple of four.)

Embedding of audio in SDI is performed on group granularity (each group consist of four channels of audio). When enabled, Channel padding logic converts the non-multiple of four channel AXI4-S transactions (2, 6, 10, 14, etc.) to multiple of four channel transactions (4, 8, 12, 16, etc.) by padding the remaining two channels with mute data.

Audio Multiplexer

In SD-SDI mode, as per SMPTE ST 272, up to 16 channels of audio are inserted on data stream 1. In HD-SD mode, as per SMPTE ST 299-1, up to 16 channels of audio are inserted onto data streams 1 and 2. In 3G, 6G and 12G SDI modes, as per SMPTE 299-1 and SMPTE ST 299-2, up to 32 channels of audio are inserted onto data streams 1, 2, 3 and 4. Audio control packets are inserted on data stream 1 and 3 (Y Video In) and audio data packets are inserted on data stream 2 and 4 (CBCR Video In). Remaining data streams from SDI Transmitter are delayed to match the latency of the audio insertion. Audio embedded and latency matched data streams are sent back to the SDI Transmitter for further processing.

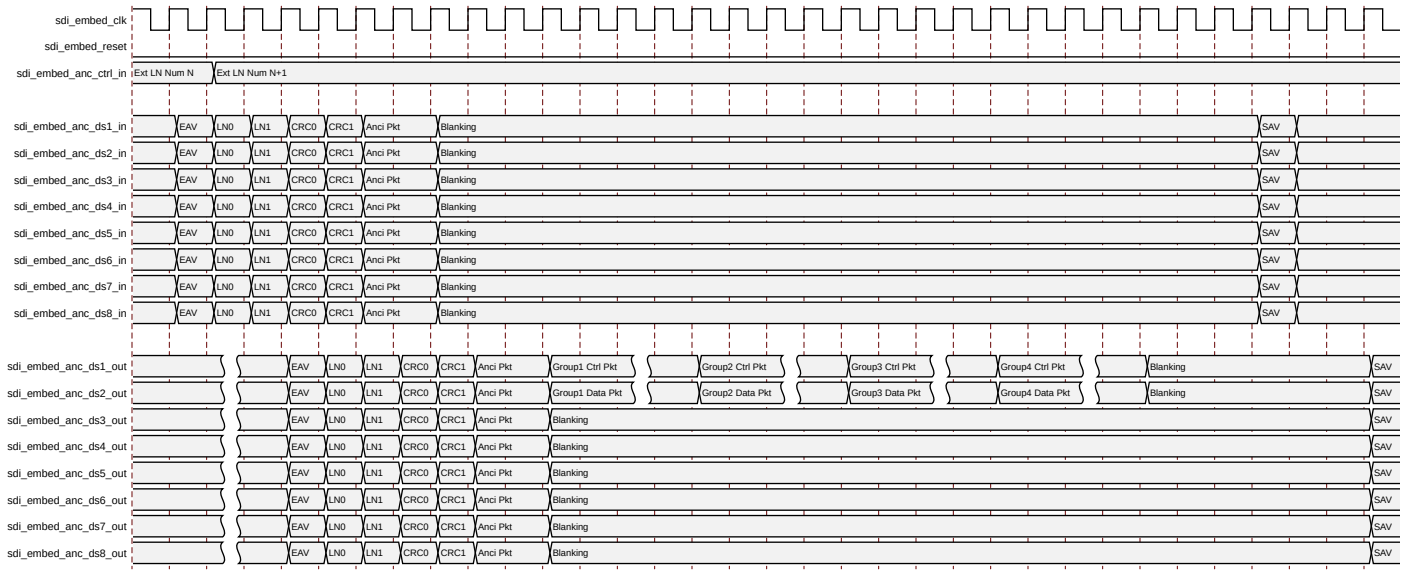
The figure below highlights the maximum number of audio channels that can be embedded in each SDI mode as per the SDI specification. Audio multiplexers working on data stream 1, 2, 3, and 4 embeds a maximum of 32 audio channels.

Figure 6: **Embedding Multiple Audio Groups**

Maximum Number of Audio Channels in each SDI Mode (as per spec)									
SDI Mode	DS1/2	DS3/4	DS5/6	DS7/8	DS9/10	DS11/12	DS13/14	DS15/16	Total
SD	16	Data Stream N/A							16
HD	16	Data Stream N/A							16
3G-A	32	Data Stream N/A							32
3G-B	16	16	Data Stream N/A						32
6G-M1	32	32	Data Stream N/A						64
6G-M2	16	16	16	16	Data Stream N/A				64
12G-8DS	32	32	32	32	Data Stream N/A				128
12G-16DS	16	16	16	16	16	16	16	16	128
Note : Due to the limitation in the blanking region, only half of the channels are supported in the following video formats (4096x2160p29.97/30/59.94/60 and 2048x1080p29.97/30/59.94/60)									

The following figure highlights the SDI Interface to the UHD-SDI Audio (Embed) in 12G SDI mode with 8 data streams. UHD-SDI Audio (Embed) bypass the non-audio ancillary packets before inserting the audio packets into the blanking region.

Figure 7: **SDI Interface Diagram of UHD-SDI Audio (Embed)**



SDI Audio Status Extract

This module checks for the presence of audio control packets on the incoming SDI stream. When a control packet is detected for a particular group, this module marks the group as active and decodes active channel, sample rate, and asx information into the status registers.

After all the control packets are received, an interrupt `aud_stat_update` is asserted to indicate that data in active group (0x40), active channel (0x60), sample rate (0x70) and asx (0x80) status registers are valid.

Several other interrupts are provided to indicate the change in active groups, active channels, sample rate and asx information from its previous value.

Note: The audio status update (`aud_stat_update`) interrupt is asserted once for each frame. If the control packets are not present in the complete frame, this interrupt is asserted with `active_group` (0x40) set to 0x0.

Audio De-Multiplexer

In SD-SDI mode, as per SMPTE ST 272, up to 16 channels of audio is extracted from data stream 1 (Y Video In). In HD-SD mode, as per SMPTE ST 299-1, up to 16 channels of audio is extracted from data stream 1 and 2. In 3G, 6G and 12G SDI modes, as per SMPTE ST 299-1 and SMPTE ST 299-2, up to 32 channels of audio are extracted from data streams 1, 2, 3, and 4. Audio control packets are extracted from data stream 1 and 3 (Y Video In) and audio data packets are extracted from data stream 2 and 4 (CBCR Video In).

Clock Phase Logic

When clock phase logic is enabled, extracted audio samples along with the correspoding clock phase information are stored in the internal buffers. Audio samples are output on AXI4-Stream interfacewhen the clock phase matches with the current line and sample position. This ensures that Audio samples are evenly distributed (as per sample rate) on the AXI4-Stream interface.

When clock phase logic is disabled, audio samples are output on AXI4-Stream interface as and when they are extracted.

Note: Some equipment may not produce the correct clock phase in which case UHD-SDI Audio (Extract) cannot match the decoded clock phase with the line and sample number. UHD-SDI Audio (Extract) has the logic to handle this case by flushing the samples whose clock phase cannot be matched.

AXI4-Stream Master

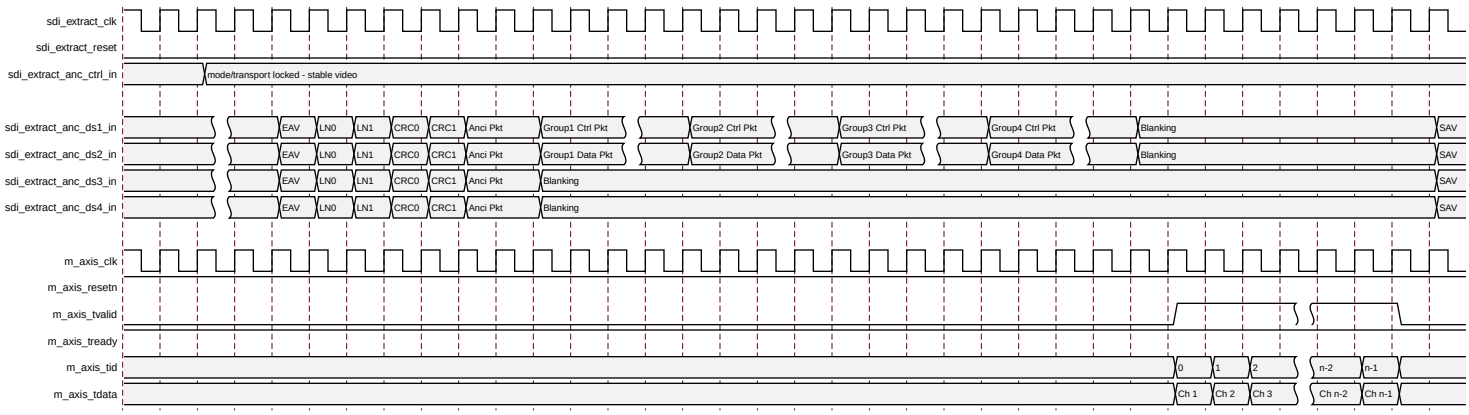
The audio interface to an UHD-SDI Audio (Extract) is a 32-bit AXI4-Stream master bus. The AXI4-Stream Master transfers the 32-bit data read from the receive sample FIFO onto the AXI4-Stream interface. The corresponding data valid signal (m_axis_tvalid) is set and the channel identifier signal (m_axis_tid) is driven with the corresponding channel number.

When GUI option **Enable Per Group AXIS** is turned on, UHD-SDI Audio (Extract) outputs audio data on multiple AXI4-Stream master interfaces. Each AXI4-Stream interface carrying audio data of one audio group.

Note: UHD-SDI Audio (Extract) does not wait for all the audio samples to be decoded before sending them out on AXI4-S interface. For example, if the incoming stream has 16 channels of audio (embedded as audio groups G1, G1, G1, G2, G2, G2, G3, G3, G3, G4, G4, G4), UHD-SDI Audio (Extract) does not wait for all the 16 channels to be decoded before initiating the AXI4-S transaction. It outputs the samples as they are decoded (G1, G1, G1, G2, G2, G2, G3, G3, G3, G4, G4, G4). Systems that expect all the samples to come in order (G1, G2, G3, G4, etc) should handle it outside of this IP.

The following figure highlights the interface diagram of the UHD-SDI Audio (Extract).

Figure 8: **Interface Diagram of UHD-SDI Audio (Extract)**



AES Channel Status Extract

Extraction of channel status bits into channel status registers is configurable. When enabled, channel status registers hold the 192-bit channel status information. User can select the channel pair from which channel status should be extracted.

After one complete audio block is received, an interrupt `aes_cs_update` is asserted to indicate that data in channel status registers (0x48 to 0x5C) are valid.

Another interrupt is provided to indicate the change in channel status information from its previous value.

Standards

The UHD-SDI Audio IP core is designed in accordance with the SMPTE ST 272 for SD-SDI, SMPTE ST 299-1 for HD-SDI and SMPTE ST 299-1 & 2 for 3G/6G/12G-SDI.

Performance

For full details about performance and resource use, visit the Performance and Resource Use web page.

Maximum Frequencies

Maximum frequency of AXI4-Stream interface clock (`s_axis_clk` and `m_axis_clk`) is 300 MHz.

Maximum frequency of AXI4-Lite interface clock (`s_axi_aclk`) is 200 MHz.

Maximum frequency of SDI interface clock (`sdi_embed_clk` and `sdi_extract_clk`) is 297 MHz in 12G-SDI mode, 148.5 MHz in 6G/3G/SD-SDI modes and 74.25 MHz in HD-SDI mode.

Resource Use

For full details about performance and resource use, visit the Performance and Resource Use web page.

Port Descriptions

The UHD-SDI Audio IP core I/O signals are listed and described in this section.

UHD-SDI Audio (Embed) Input/Output (I/O) Signals

The UHD-SDI Audio (Embed) Input/Output (I/O) signals are listed and described in the following sections.

Configuration Interface [AXI4-Lite Interface Enabled]

Table 2: **UHD-SDI Audio (Embed) I/O Signal Description**

Port Name	Width	I/O	Description
s_axi_aclk	1	Input	AXI4-Lite clock
s_axi_aresetn	1	Input	AXI4-Lite reset, Active-Low
s_axi_awaddr	32	Input	AXI4-Lite Write address
s_axi_awprot	3	Input	Write protection
s_axi_awvalid	1	Input	Write address valid
s_axi_awready	1	Output	Write address ready
s_axi_wdata	32	Input	Write data bus
s_axi_wstrb	4	Input	Write strobes
s_axi_wvalid	1	Input	Write valid
s_axi_wready	1	Output	Write ready

Table 2: **UHD-SDI Audio (Embed) I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
s_axi_bresp	2	Output	Write response
s_axi_bvalid	1	Output	Write response valid
s_axi_bready	1	Input	Response ready
s_axi_araddr	32	Input	Read address
s_axi_arprot	3	Input	Read protection
s_axi_arvalid	1	Input	Read address valid
s_axi_arready	1	Output	Read address ready
s_axi_rdata	32	Output	Read data bus
s_axi_rresp	2	Output	Read response
s_axi_rvalid	1	Output	Read valid
s_axi_rready	1	Input	Read ready

Configuration Interface [AXI4-Lite Interface Disabled]

Table 3: **UHD-SDI Audio (Embed) I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_config	128	Input	See UHD-SDI Audio (Embed) Register Space for detailed information on the fields mentioned below: [0] - module_en [1] - core_reset [5:2] - t_family [9:6] - t_rate [10] - t_scan [11] - ext_line_en [14:12] - smpl_rate [15] - smpl_size [16] - asx [20:17] - aes_chan_pair [31:21] - reserved [63:32] - valid_chan [95:64] - mute_chan [127:96] - reserved
sdi_embed_status	388	Output	See UHD-SDI Audio (Embed) Register Space for detailed information on the fields mentioned below: [3:0] -gui_max_aud_chan [5:4] -gui_uhdsdi_std [6] - gui_aud_function [7] - gui_axilite [8] - gui_sdi_aud_stat [9] - gui_aes_chan_stat [10] - gui_chan_pad [19:11]- reserved [20] - aud_stat_update [21] - act_group_change [22] - act_chan_change [23] - smpl_rate_change [24] - asx_change [25] - aes_cs_update [26] - aes_cs_change [31:27]- reserved [63:32] - core_version [255:64] - chan_stat [299:256] - reserved [307:300] - act_group_stat [339:308] - act_chan_stat [371:340] - smpl_rate_stat [387:372] - asx_stat

AXI4-Stream Slave Interface [Audio Input]

Table 4: **UHD-SDI Audio (Embed) I/O Signal Description**

Port Name	Width	I/O	Description
s_axis_clk	1	Input	AXI4-Stream clock
s_axis_resetn	1	Input	AXI4-Stream reset, Active-Low
s_axis_tvalid	1	Input	AXI4-Stream Valid
s_axis_tready	1	Output	AXI4-Stream Ready
s_axis_tdata	32	Input	AXI4-Stream Data
s_axis_tid	log base 2 (Maximum Audio Channels)	Input	AXI4-Stream Identifier s_axis_tid width is: • 1 when Maximum Audio Channels is 2 • 2 when Maximum Audio Channels is 4 • 3 when Maximum Audio Channels is 6 or 8 • 4 when Maximum Audio Channels is 10, 12, 14 or 16 • 5 when Maximum Audio Channels is 32

Reset Output Interface

Table 5: **UHD-SDI Audio (Embed) I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_reset_out	1	Output	This signal, when set to 1, indicates that UHD-SDI Audio (Embed) is under reset.

SDI Input Interface

Table 6: **UHD-SDI Audio (Embed) I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_clk	1	Input	This is the video clock
sdi_embed_reset	1	Input	Video reset, Active-High

Table 6: **UHD-SDI Audio (Embed) I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
sdi_embed_anc_ctrl_in	32	Input	Ancillary control information from the Xilinx® UHD SDI Transmitter Subsystem. You mmust populate these signals manually when UHD-SDI TX Subsystem is not used. [0] - Clock enable in SD-SDI mode [1] - Clock enable in non-SD mode [12:2] - External line number. In general, externally provided line numbers must be used in cases where valid line numbers have not yet been embedded in the input video stream. [13] - SDI Transmitter Reset. This signals indicates that UHD-SDI TX Subsystem is under reset. When UHD-SDI TX Subsystem is not used, connect this to `tx_fabric_rst_out` from drp control engine. [16:14] - SDI mode • 0 - HD • 1 - SD • 2 - 3G • 4 - 6G • 5 - 12G [19:17] - Data stream interleaving pattern. • 0 - SD, HD, and 3G level A • 1 - 3G level B • 2 - 8 stream interleave in 6G and 12G modes • 3 - 4 stream interleave in 6G mode • 4 - 16 stream interleave in 12G mode [31:20] - Reserved
sdi_embed_anc_ds1_in	10	Input	Data stream 1. In SD mode this is interleaved Y/C. In HD and 3GA modes, this is the Y channel. In 3GB mode, this is the link A Y channel. In 6G and 12G modes, this is ds1.
sdi_embed_anc_ds2_in	10	Input	Data stream 2. Not used in SD mode. In HD and 3GA modes, this is the C channel. In 3GB mode, this is the link A C channel. In 6G and 12G modes, this is ds2.
sdi_embed_anc_ds3_in	10	Input	Data stream 3. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B Y channel. In 6G and 12G modes this is ds3.
sdi_embed_anc_ds4_in	10	Input	Data stream 4. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B C channel. In 6G and 12G modes this is ds4.
sdi_embed_anc_ds5_in through sdi_embed_anc_ds16_in	10	Input	Additional data stream ports. The number of ports that are active depend on the number of data streams interleaved on the SDI signal. These ports are never active in SD, HD, or 3G modes.

SDI Output Interface

Table 7: **UHD-SDI Audio (Embed) I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_anc_ds1_out	10	Output	Data stream 1. In SD mode this is interleaved Y/C. In HD and 3GA modes, this is the Y channel. In 3GB mode, this is the link A Y channel. In 6G and 12G modes, this is ds1.
sdi_embed_anc_ds2_out	10	Output	Data stream 2. Not used in SD mode. In HD and 3GA modes, this is the C channel. In 3GB mode, this is the link A C channel. In 6G and 12G modes, this is ds2.
sdi_embed_anc_ds3_out	10	Output	Data stream 3. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B Y channel. In 6G and 12G modes, this is ds3.
sdi_embed_anc_ds4_out	10	Output	Data stream 4. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B C channel. In 6G and 12G modes, this is ds4.
sdi_embed_anc_ds5_out through sdi_embed_anc_ds16_out	10	Output	Additional data stream ports. The number of ports that are active depend on the number of data streams interleaved on the SDI signal. These ports are never active in SD, HD, or 3G modes.

Interrupt Interface [AXI4-Lite Interface Enabled]

Table 8: **UHD-SDI Audio (Embed) I/O Signal Description**

Port Name	Width	I/O	Description
interrupt	1	Output	Interrupt

UHD-SDI Audio (Extract) Input/Output (I/O) Signals

The UHD-SDI Audio (Extract) Input/Output (I/O) signals are listed and described in the following sections.

Configuration Interface [AXI4-Lite Interface Enabled]

Table 9: **UHD-SDI Audio (Extract) I/O Signal Description**

Port Name	Width	I/O	Description
s_axi_aclk	1	Input	AXI4-Lite clock
s_axi_aresetn	1	Input	AXI4-Lite reset, Active-Low
s_axi_awaddr	32	Input	Write address
s_axi_awprot	3	Input	Write protection
s_axi_awvalid	1	Input	Write address valid
s_axi_awready	1	Output	Write address ready
s_axi_wdata	32	Input	Write data bus

Table 9: **UHD-SDI Audio (Extract) I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
s_axi_wstrb	4	Input	Write strobes
s_axi_wvalid	1	Input	Write valid
s_axi_wready	1	Output	Write ready
s_axi_bresp	2	Output	Write response
s_axi_bvalid	1	Output	Write response valid
s_axi_bready	1	Input	Response ready
s_axi_araddr	32	Input	Read address
s_axi_arprot	3	Input	Read protection
s_axi_arvalid	1	Input	Read address valid
s_axi_arready	1	Output	Read address ready
s_axi_rdata	32	Output	Read data bus
s_axi_rresp	2	Output	Read response
s_axi_rvalid	1	Output	Read valid
s_axi_rready	1	Input	Read ready

Configuration Interface [AXI4-Lite Interface Disabled]

Table 10: **UHD-SDI Audio (Extract) I/O Signal Description**

Port Name	Width	I/O	Description
sdi_extract_config	128	Input	See UHD-SDI Audio (Extract) Register Space for detailed information on the fields mentioned below [0] - module_en [1] - core_reset [16:2] - reserved [20:17] - aes_chan_pair [27:21] - reserved [28] - ignore_clk_phase [31:29] - reserved [63:32] - valid_chan [95:64] - mute_chan [127-96] - reserved

Table 10: **UHD-SDI Audio (Extract) I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
sdi_extract_status	388	Output	See UHD-SDI Audio (Extract) Register Space for detailed information on the fields mentioned below. [3:0] - gui_max_aud_chan [5:4] - gui_uhdsdi_std [6] - gui_aud_function [7] - gui_axilite [8] - gui_sdi_aud_stat [9] - gui_aes_chan_stat [10] - gui_clk_phase [11] - gui_per_group_axis [15:12] - reserved [16] - parity_err [17] - chksum_err [18] - rs_fifo_overflow [19] - vid_prop_change [20] - aud_stat_update [21] - act_group_change [22] - act_chan_change [23] - smpl_rate_change [24] - asx_change [25] - aes_cs_update [26] - aes_cs_change [31:27] - reserved [63:32] - core_version [255:64] - chan_stat [263:256] - rs_fifo_overflow_stat [299:264] - reserved [307:300] - act_group_stat [339:308] - act_chan_stat [371:340] - smpl_rate_stat [387:372] - asx_stat

SDI Input Interface

Table 11: **UHD-SDI Audio (Extract) I/O Signal Description**

Port Name	Width	I/O	Description
sdi_extract_clk	1	Input	This is the video clock
sdi_extract_reset	1	Input	Video reset, Active-High

Table 11: **UHD-SDI Audio (Extract) I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
sdi_extract_anc_ctrl_in	32	Input	Ancillary control information from the Xilinx UHD SDI Receiver Subsystem. You must populate these signals manually when UHD-SDI RX Subsystem is not used. [0] - `rx_ce`. This signal is the video clock enable from the receiver [3:1] - `rx_mode`. This signal indicates the current SDI mode of the receiver • 000 = HD • 001 = SD • 010 = 3G • 100 = 6G • 101 = 12G 1000/1000 • 110 = 12G 1000/1001 [7:4] - `rx_t_family`. This signal indicate the video format family • 0000 - SMPTE ST 274 1920 x 1080 • 0001 SMPTE ST 296 1280 x 720 • 0010 SMPTE 2048-2 2048 x 1080 • 0011 SMPTE 295 1920 x 1080 • 1000 NTSC 720 x 486 • 1001 PAL 720 x 576 • 1111 Unknown [8] - `rx_mode_locked`. When the receiver locks to the correct SDI mode, the `rx_mode_locked` goes High. [9] `rx_t_locked`. This signal is 1 when the transport detection function in the receiver has identified the transport format of the SDI signal

Table 11: **UHD-SDI Audio (Extract) I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
sdi_extract_anc_ctrl_in (cont'd)	32	Input	[13:10] `rx_t_rate`. This signal indicates the frame rate of the transport. • 0000 - None • 0010 - 23.98 Hz • 0011 - 24 Hz • 0100 - 47.95 • Hz 0101 - 25 Hz • 0110 - 29.97 Hz • 0111 - 30 Hz • 1000 - 48 Hz • 1001 - 50 Hz • 1010 - 59.94 Hz • 1011 - 60 Hz • Others - Reserved [14] `rx_t_scan`. This signal indicates whether the transport is interlaced (Low) or progressive (High). [15] - `rx_rst_int_sys`. This signals indicates that UHD-SDI RX Subsystem is under reset. When UHD-SDI RX Subsystem is not used, connect this to `rx_fabric_rst_out` from drp control engine.. [16] `rx_level_b_3g`. In 3G-SDI mode, this output is asserted High when the input signal is level B and Low when it is level A. [19:17] `rx_act_streams`. This signal indicates the number of data streams that are active for the current video format being received. • 000 - 1 active stream • 001 - 2 active streams • 010 - 4 active streams • 011 - 8 active streams • 100 - 16 active streams [31:20] reserved
sdi_extract_anc_ds1_in	10	Input	Data stream 1. In SD mode this is interleaved Y/C. In HD and 3GA modes, this is the Y channel. In 3GB mode, this is the link A Y channel. In 6G and 12G modes, this is ds1.
sdi_extract_anc_ds2_in	10	Input	Data stream 2. Not used in SD mode. In HD and 3GA modes, this is the C channel. In 3GB mode, this is the link A C channel. In 6G and 12G modes, this is ds2.
sdi_extract_anc_ds3_in	10	Input	Data stream 3. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B Y channel. In 6G and 12G modes this is ds3.
sdi_extract_anc_ds4_in	10	Input	Data stream 4. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B C channel. In 6G and 12G modes this is ds4.

AXI4-Stream Master Interface [Audio Output]

***Note*:** When GUI option **Enable Per Group AXIS** is enabled, multiple AXI4-Stream interfaces with group number as the post fix is available in place of the interface shown below (example m_axis_*_grp1, m_axis_*_grp2, etc.)

Table 12: **UHD-SDI Audio (Extract) I/O Signal Description**

Port Name	Width	I/O	Description
m_axis_clk	1	Input	AXI4-Stream clock
m_axis_resetn	1	Input	AXI4-Stream reset, Active-low
m_axis_tvalid	1	Output	AXI4-Stream Valid Out
m_axis_tready	1	Input	AXI4-Stream Ready
m_axis_tdata	32	Output	AXI4-Stream Data
m_axis_tid	log base 2 (Maximum Audio Channels)	Output	AXI4-Stream Identifier m_axis_tid width is set to: • 1 when Maximum Audio Channels is 2 • 2 when Maximum Audio Channels is 4 • 3 when Maximum Audio Channels is 6 or 8 • 4 when Maximum Audio Channels is 10, 12, 14 or 16 • 5 when Maximum Audio Channels is 32

Reset Output Interface

Table 13: **UHD-SDI Audio (Extract) I/O Signal Description**

Port Name	Width	I/O	Description
sdi_extract_reset_out	1	Output	This signal, when set to 1, indicates that Audio Extractor is under reset. Downstream IP's can use this signal as reset.

Interrupt Interface [AXI4-Lite Interface Enabled]

Table 14: **SDI Audio Extractor I/O Signal Description**

Port Name	Width	I/O	Description
interrupt	1	Output	Interrupt

Recovered Clock Interface

Table 15: **UHD-SDI Audio (Extract) Signal Description**

Port Name	Width	I/O	Description
rec_clk	Ceil (Maximum Audio Channels/4)	Output	Clock recovered using clock phase data for non-SD SDI modes. This signal is only valid when clock phase logic is enabled. • Bit 0 - Clock recovered from Group 1 • Bit 1 - Clock recovered from Group 2 through • Bit 7 - Clock recovered from Group 8

Register Space

UHD-SDI Audio (Embed) Register Space

The following table specifies the offset address, register name, and accessibility of each firmware addressable registers within the UHD-SDI Audio (Embed). User access to each register is from an offset to the base address.

***Note*:** AES Channel Status Registers (0x48 to 0x5C) are only valid when GUI option **Extract AES Channel Status** is enabled.

***Note*:** SDI Audio Status Registers (0x40, 0x60, 0x70, and 0x80) are only valid when GUI option **Extract SDI Audio Status** is enabled.

Table 16: **Register Address Space - UHD-SDI Audio (Embed)**

Offset	Name	Description
0x00	Module Control	Register to enable the embedding of audio on to SDI stream.
0x04	Soft Reset Register	Register to issue soft reset to the core.
0x08	Core Version Register	Status register conveying the core version
0x0C	Interrupt Enable Register	Register to enable different interrupts
0x10	Interrupt Status Register	Status register conveying the status of different interrupts
0x14	Video Control Register	Register to indicate video properties
0x18	Audio Control Register	Register to indicate audio properties
0x20	Channel Valid Register	Register to indicate valid channels
0x30	Channel Mute Register	Register to indicate mute channels

Table 16: **Register Address Space - UHD-SDI Audio (Embed)** *(cont'd)*

Offset	Name	Description
0x40	Active Group Status Register	Status register conveying the audio groups that are detected on the incoming SDI stream
0x48	Channel Status Register 1	Status register conveying the bits [31:0] of AES channel status
0x4C	Channel Status Register 2	Status register conveying the bits [63:32] of AES channel status
0x50	Channel Status Register 3	Status register conveying the bits [95:64] of AES channel status
0x54	Channel Status Register 4	Status register conveying the bits [127:96] of AES channel status
0x58	Channel Status Register 5	Status register conveying the bits [159:128] of AES channel status
0x5C	Channel Status Register 6	Status register conveying the bits [191:160] of AES channel status
0x60	Active Channel Status Register	Status register conveying the active channel information decoded from audio control packet
0x70	Sample Rate Status Register	Status register conveying the sample rate information decoded from audio control packet
0x80	Asynchronous Channel Pair Status Registers	Status register conveying the async channel pair (ASX) information decoded from audio control packet
0xFC	GUI Parameters Status register	Status register conveying the values of the GUI parameters selected during core generation
Others	Reserved	Reserved

Module Control Register (0x00)

Table 17: **Module Control Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:1	reserved	N/A	0	Reserved
0	module_en	R/W	0	This bit when set to 1, enables the embedding of audio onto SDI stream.

Soft Reset Register (0x04)

Table 18: **Soft Reset Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:2	Reserved	N/A	0	Reserved
1	core_reset	R/W	0	This bit when set to 1, resets the data path of the core.

Table 18: **Soft Reset Register - UHD-SDI Audio (Embed)** *(cont'd)*

Bit	Field Name	Access Type	Default Value	Description
0	config_reset	RW1C	0	This bit when set to 1, resets the configuration registers.

Core Version Register (0x08)

Table 19: **Core Version Register (0x08) - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:24	major_version	RO	2	Core major version
23:16	minor_version	RO	0	Core minor version
15:12	revision	RO	0	Core revision
11:8	patch	RO	0	Core patch details
7:0	internal_revision	RO	0	Core internal revision

Interrupt Enable Register (0x0C)

Table 20: **Interrupt Enable Register (0x0C) - UHD-SDI Audio (Embed)**

Bit	Access Type	Field Name	Default Value	Description
31:18	N/A	reserved	0	Reserved
17	R/W	aes_cs_change	0	This bit when set to 1, generates an interrupt when AES channel status value decoded is different from its previous value
16	R/W	aes_cs_update	0	This bit when set to 1, generates an interrupt when AES channel status value is updated to the registers (0x48 to 0x5C)
15:13	N/A	reserved	0	Reserved
12	R/W	asx_change	0	This bit when set to 1, generates an interrupt when ASX value decoded is different from its previous value
11	R/W	smpl_rate_change	0	This bit when set to 1, generates an interrupt when sample rate value decoded is different from its previous value
10	R/W	act_chan_chang	0	This bit when set to 1, generates an interrupt when active channel value decoded is different from its previous value
9	R/W	act_group_change	0	This bit when set to 1, generates an interrupt when active group value decoded is different from its previous value
8	R/W	aud_stat_update	0	This bit when set to 1, generates an interrupt when active group (0x40), active channel (0x60), sample rate (0x70) and asx (0x80) registers are updated
7:0	N/A	reserved	0	Reserved

Interrupt Status Register (0x10)

Table 21: **Interrupt Status Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:18	Reserved	N/A	0	Reserved
17	aes_cs_change	RW1C	0	This bit when read as 1, indicates that AES channel status value decoded is different from its previous value
16	aes_cs_update	RW1C	0	This bit when read as 1, indicates that AES channel status registers (0x48 to 0x5C) are updated
15:13	Reserved	N/A	0	Reserved
12	asx_change	RW1C	0	This bit when read as 1, indicates that ASX value decoded is different from its previous value
11	smpl_rate_change	RW1C	0	This bit when read as 1, indicates that sample rate value decoded is different from its previous value
10	act_chan_change	RW1C	0	This bit when read as 1, indicates that active channel value decoded is different from its previous value
9	act_group_change	RW1C	0	This bit when read as 1, indicates that active group value decoded is different from its previous value
8	aud_stat_update	RW1C	0	This bit when read as 1, indicates that active group (0x40), active channel (0x60), sample rate (0x70) and asx (0x80) registers are updated
7:0	Reserved	N/A	0	Reserved

Video Control Register (0x14)

Table 22: **Video Control Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:17	reserved	N/A	0	Reserved
16	ext_line_en	R/W	0	This bit selects the source of video line number • 0 - Use line numbers decoded from video stream • 1 - Use line numbers decoded from ancillary control bus “sdi_embed_anc_ctrl_in”
15:9	reserved	N/A	0	Reserved
8	t_scan	R/W	0	Transport Scan • 0 – Interlaced or PSF • 1 – Progressive ***Note*:** Dual Link 3G-B is the special case where 1080p60 image is split in to 2 x 1080i60 images. In this case transport scan should be mentioned as Interlaced.

Table 22: **Video Control Register - UHD-SDI Audio (Embed)** *(cont'd)*

Bit	Field Name	Access Type	Default Value	Description
7:4	t_rate	R/W	0	Transport Rate • 2 - 23.98 Hz • 3 - 24 Hz • 4 - 47.95 Hz • 5 - 25 Hz • 6 - 29.97 Hz • 7 - 30 Hz • 8 - 48 Hz • 9 - 50 Hz • 10 - 59.94 Hz • 11 - 60 Hz For example, 24 Hz should be configured for 1080p24, 1080pSF24 and 1080i48 resolutions.
3:0	t_family	R/W	0	Transport Family • 0 - 1920 x 1080 • 1 - 1280 x 720 • 2 - 2048 x 1080 • 8 - 720 x 486 (NTSC) • 9 - 720 x 576 (PAL) ***Note*:** 1920x1080 and 2048x1080 are the resolutions of sub images for 3840x2160 and 4096x2160 resolutions.

Audio Control Register (0x18)

Table 23: **Audio Control Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:20	reserved	N/A	0	Reserved

Table 23: **Audio Control Register - UHD-SDI Audio (Embed)** *(cont'd)*

Bit	Field Name	Access Type	Default Value	Description
19:16	aes_chan_pair	R/W	0	This signal selects the channel pair from which 192-bit AES channel status need to be extracted. • 0 – Channel Pair 1 (Channel 1 & 2) • 1 – Channel Pair 2 (Channel 3 & 4) through • 15 – Channel Pair 16 (Channel 31 & 32)
15:5	reserved	N/A	0	Reserved
4	asx	R/W	0	This signal indicates the asynchronous data flag (ASX) • 0 – Synchronous Audio • 1 – Asynchronous Audio
3	smpl_size	R/W	0	This signal indicates the audio sample size (for SD-SDI mode only) • 0 – 20 bit Audio • 1 – 24 bit Audio
2:0	smpl_rate	R/W	0	This signal indicates the audio sample rate • 0 – 48 KHz • 1 – 44.1 KHz • 2 – 32 KHz

Channel Valid Register (0x20)

Table 24: **Channel Valid Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	valid_chan	R/W	0xFFFFFFFF	When set to 1, each bit enables the embedding of that channel onto SDI. When set to 0, that particular channel is blocked from going onto SDI. For example, if the incoming audio on AXI4-S interface is for 16 channels and you want to embed only Group 2, then this register should be configured as 0x0000_00F0.. • Bit [0] – Channel 1 • Bit [1] – Channel 2 through • Bit [31] – Channel 32

Channel Mute Register (0x30)

Table 25: **Channel Mute Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Vaule	Description
31:0	mute_chan	R/W	0	Each bit when set to 1, replaces the audio data with mute data while embedding on to SDI. • Bit [0] – Channel 1 Mute • Bit [1] – Channel 2 Mute through • Bit [31] – Channel 32 Mute

Active Group Status Register (0x40)

Table 26: **Active Group Status Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:8	Reserved	N/A	0	Reserved
7:0	act_group_stat	RO	0	Each bit when read as 1, indicates that audio control packet for that group is detected on the incoming SDI stream. • Bit [0] – Group 1 (Channel 1 to 4) • Bit [1] – Group 2 (Channel 5 to 8) through • Bit [7] – Group 8 (Channel 28 to 32)

Channel Status Register 1 (0x48)

Table 27: **Channel Status Register 1 - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_stat_1	RO	0	Bits [31:0] of AES Channel Status

Channel Status Register 2 (0x4C)

Table 28: **Channel Status Register 2 - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_stat_2	RO	0	Bits [63:32] of AES Channel Status

Channel Status Register 3 (0x50)

Table 29: **Channel Status Register 3 - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_stat_3	RO	0	Bits [95:64] of AES Channel Status

Channel Status Register 4 (0x54)

Table 30: **Channel Status Register 4 - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_stat_4	RO	0	Bits [127:96] of AES Channel Status

Channel Status Register 5 (0x58)

Table 31: **Channel Status Register 5 - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_stat_5	RO	0	Bits [159:128] of AES Channel Status

Channel Status Register 6 (0x5C)

Table 32: **Channel Status Register 6 - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_stat_6	RO	0	Bits [191:160] of AES Channel Status

Active Channel Status Register (0x60)

Table 33: **Active Channel Status Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	act_chan_stat	RO	0	Active channel information decoded from audio control packet • Bit [0] – Channel 1 • Bit [1] – Channel 2 through • Bit [31] – Channel 32

Sample Rate Status Register (0x70)

Table 34: **Sample Rate Status Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:0	smpl_rate_stat	RO	0	Sample rate information decoded from audio control packet (0 – 48 KHz, 1 – 44.1 KHz, 2 – 32 KHz, 3 – Reserved) • Bit [1:0] – Channel 1 & 2 • Bit [3:2] – Channel 3 & 4 through • Bit [31:30] - Channel 31 & 32

Async Channel Pair Status Register (0x80)

Table 35: **Async Channel Pair Status Register - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
15:0	asx_stat	RO	0	ASX information decoded from audio control packet (0 - Synchronous audio & 1 - Asynchronous audio) • Bit [0] – Channel 1 & 2 Asx • Bit [1] – Channel 3 & 4 Asx through • Bit [15] - Channel 31 & 32 Asx
31:16	Reserved	RO	0	Reserved

GUI Parameters (0xFC)

Table 36: **GUI Parameters - UHD-SDI Audio (Embed)**

Bit	Field Name	Access Type	Default Value	Description
31:11	reserved	N/A	0	Reserved
10	gui_chan_pad	RO	1	Core is configured with channel padding • 0 - Disabled • 1 – Enabled
9	gui_aes_chan_stat	RO	1	Core is configured with AES channel status extraction • 0 - Disabled • 1 – Enabled
8	gui_sdi_aud_stat	RO	1	Core is configured with SDI audio status extraction • 0 - Disabled • 1 – Enabled
7	gui_axilite	RO	1	Core is configured with AXI4-Lite • 0 - Disabled • 1 – Enabled
6	gui_aud_function	RO	0	Core is configured with audio function set to • 0 - Embed • 1 – Extract
5:4	gui_uhdsdi_std	RO	2	Core is configured with UHD SDI mode set to • 0 - 3G_SDI • 1 - 6G_SDI • 2 - 12G_SDI_8DS • 3 - 12G_SDI_16DS

Table 36: **GUI Parameters - UHD-SDI Audio (Embed)** *(cont'd)*

Bit	Field Name	Access Type	Default Value	Description
3:0	gui_max_aud_chan	RO	7	Core is configured with maximum audio channels set to • 0 – 2 Channels • 1 – 4 Channels • 2 – 6 Channels • 3 – 8 Channels • 4 – 10 Channels • 5 – 12 Channels • 6 – 14 Channels • 7 – 16 Channels • 8 – 32 Channels

UHD-SDI Audio (Extract) Register Space

This section specifies the offset address, register name, and accessibility of each firmware addressable registers within the UHD-SDI Audio (Extract). User access to each register is from an offset to the base address.

***Note*:** AES Channel Status Registers (0x48 to 0x5C) are only valid when GUI option **Extract AES Channel Status** is enabled.

***Note*:** SDI Audio Status Registers (0x40, 0x60, 0x70, and 0x80) are only valid when GUI option **Extract SDI Audio Status** is enabled.

Table 37: **Register Address Space - UHD-SDI Audio (Extract)**

Offset	Name	Description
0x00	Module Control Register	Register to enable the extraction of audio from SDI stream
0x04	Soft Reset Register	Register to issue soft reset to the core
0x08	Core Version Register	Status register conveying the core version
0x0C	Interrupt Enable Register	Register to enable different interrupts
0x10	Interrupt Status Register	Status register conveying the status of different interrupts
0x18	Audio Control Register	Register to indicate audio properties
0x20	Channel Valid Register	Register to indicate valid channels
0x30	Channel Mute Register	Register to indicate mute channels
0x40	Active Group Status Register	Status register conveying the audio groups that are detected on the incoming SDI stream
0x44	RX Sample FIFO Overflow Status Register	Status register conveying the group for which RX sample FIFO is overflowing

Table 37: **Register Address Space - UHD-SDI Audio (Extract)** *(cont'd)*

Offset	Name	Description
0x48	Channel Status Register 1	Status register conveying the bits [31:0] of AES channel status
0x4C	Channel Status Register 2	Status register conveying the bits [63:32] of AES channel status
0x50	Channel Status Register 3	Status register conveying the bits [95:64] of AES channel status
0x54	Channel Status Register 4	Status register conveying the bits [127:96] of AES channel status
0x58	Channel Status Register 5	Status register conveying the bits [159:128] of AES channel status
0x5C	Channel Status Register 6	Status register conveying the bits [191:160] of AES channel status
0x60	Active Channel Status Register	Status register conveying the active channel information decoded from audio control packet
0x70	Sample Rate Status Register	Status register conveying the sample rate information decoded from audio control packet
0x80	Asynchronous Channel Pair Status Registers	Status register conveying the async channel pair (ASX) information decoded from audio control packet
0xFC	GUI Parameters Status Register	Status register conveying the values of the GUI parameters selected during core generation
Others	Reserved	Reserved

Module Control Register (0x00)

Table 38: **Module Control Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:1	Reserved	Not applicable	0	Reserved
0	module_en	R/W	0	This bit when set to 1, enables the extraction of audio from SDI stream

Soft Reset Register (0x04)

Table 39: **Soft Reset Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:2	Reserved	N/A	0	Reserved
1	core_reset	R/W	0	This bit when set to 1, resets the data path of the core
0	config_reset	RW1C	0	This bit when set to 1, resets the configuration registers.

Core Version Register (0x08)

Table 40: **Core Version Register (0x08) - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:24	major_version	RO	2	Core major version
23:16	minor_version	RO	0	Core minor version
15:12	revision	RO	0	Core revision
11:8	patch	RO	0	Core patch details
7:0	internal_revision	RO	0	Core internal revision

Interrupt Enable Register (0x0C)

Table 41: **Interrupt Enable Register (0x0C) - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:18	N/A	reserved	0	Reserved
17	R/W	aes_cs_change	0	This bit when set to 1, generates an interrupt when AES channel status value decoded is different from its previous value
16	R/W	aes_cs_update	0	This bit when set to 1, generates an interrupt when AES channel status value is updated to the registers (0x48 to 0x5C)
15:13	N/A	reserved	0	Reserved
12	R/W	asx_change	0	This bit when set to 1, generates an interrupt when ASX value decoded is different from its previous value
11	R/W	smpl_rate_change	0	This bit when set to 1, generates an interrupt when sample rate value decoded is different from its previous value
10	R/W	act_chan_chang	0	This bit when set to 1, generates an interrupt when active channel value decoded is different from its previous value
9	R/W	act_group_change	0	This bit when set to 1, generates an interrupt when active group value decoded is different from its previous value
8	R/W	aud_stat_update	0	This bit when set to 1, generates an interrupt when active group (0x40), active channel (0x60), sample rate (0x70) and asx (0x80) registers are updated
7:0	N/A	reserved	0	Reserved

Interrupt Status Register (0x10)

Table 42: **Interrupt Status Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:18	Reserved	N/A	0	Reserved

Table 42: **Interrupt Status Register - UHD-SDI Audio (Extract)** *(cont'd)*

Bit	Field Name	Access Type	Default Value	Description
17	aes_cs_change	RW1C	0	This bit when read as 1, indicates that AES channel status value decoded is different from its previous value
16	aes_cs_update	RW1C	0	This bit when read as 1, indicates that AES channel status registers (0x48 to 0x5C) are updated
15:13	Reserved	RW1C	0	Reserved
12	asx_change	RW1C	0	This bit when read as 1, indicates that ASX value decoded is different from its previous value
11	smpl_rate_change	RW1C	0	This bit when read as 1, indicates that sample rate value decoded is different from its previous value
10	act_chan_change	RW1C	0	This bit when read as 1, indicates that active channel value decoded is different from its previous value
9	act_group_change	RW1C	0	This bit when read as 1, indicates that active group value decoded is different from its previous value
8	aud_stat_update	RW1C	0	This bit when read as 1, indicates that active group (0x40), active channel (0x60), sample rate (0x70) and asx (0x80) registers are updated
7:4	Reserved	N/A	0	Reserved
3	vid_prop_change	R/W	0	This bit when read as 1, indicates that change in incoming video properties is detected
2	rs_fifo_overflow	R/W	0	This bit when read as 1, indicates that receive sample FIFO is overflowing
1	checksum_error	R/W	0	This bit when read as 1, indicates that checksum error is detected
0	parity_error	R/W	0	This bit when read as 1, indicates that parity error is detected

Audio Control Register (0x18)

Table 43: **Audio Control Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:30	reserved	N/A	0	Reserved
29	Ignore_clk_phase	R/W	0	This bit when set to 1, ignores the clock phase information while outputting data
28:20	reserved	N/A	0	Reserved
19:16	aes_chan_pair	R/W	0	This signal selects the channel pair from which 192-bit AES channel status need to be extracted • 0 – Channel Pair 1 (Channel 1 & 2) • 1 – Channel Pair 2 (Channel 3 & 4) through • 15 – Channel Pair 16 (Channel 31 & 32)
15:0	reserved	N/A	0	Reserved

Channel Valid Register (0x20)

Table 44: **Channel Valid Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	valid_chan	R/W	0xFFFFFFFF	When set to 1, each bit enables the transmission of that audio channel on AXI4-S interface. Setting this to 0 blocks the audio channel from coming on AXI4-S interface. For example, if the incoming SDI stream is having 16-channels of audio and you want to extract only Group 2, this register should be set to 0x0000_00F0. • Bit [0] - Channel 1 Valid • Bit [1] - Channel 2 Valid through • Bit [31] - Channel 32 Valid

Channel Mute Register (0x30)

Table 45: **Channel Mute Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	mute_chan	R/W	0	Each bit when set to 1, replaces the audio data with mute data while sending it on AXI4-S.. • Bit [0] - Channel 1 Mute • Bit [1] - Channel 2 Mute through • Bit [31] - Channel 32 Mute

Active Group Status Register (0x40)

Table 46: **Active Group Status Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:8	Reserved	N/A	0	Reserved

Table 46: **Active Group Status Register - UHD-SDI Audio (Extract)** *(cont'd)*

Bit	Field Name	Access Type	Default Value	Description
7:0	act_group_stat	RO	0	Each bit when read as 1, indicates that audio control packet for that group is detected on the incoming SDI stream • Bit [0] – Group 1 (Channel 1 to 4) • Bit [1] – Group 2 (Channel 5 to 8) through • Bit [7] – Group 8 (Channel 28 to 32)

RX Sample FIFO Overflow Status Register (0x44)

Table 47: **RX Sample FIFO Overflow Status Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
[31:8]	Reserved	N/A	0	Reserved
[7:0]	rs_fifo_overflow_stat	RO	0x0	Each bit when read as 1, indicates that RX Sample FIFO for that group is overflowing. • Bit [0] – Group 1 (Channel 1 to 4) • Bit [1] – Group 2 (Channel 5 to 8) through • Bit [7] – Group 8 (Channel 28 to 32)

Channel Status Register 1 (0x48)

Table 48: **Channel Status Register 1 - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_status_1	RO	0	Bits [31:0] of AES Channel Status

Channel Status Register 2 (0x4C)

Table 49: **Channel Status Register 2 - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_status_2	RO	0	Bits [63:32] of AES Channel Status

Channel Status Register 3 (0x50)

Table 50: **Channel Status Register 3 - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_status3	RO	0	Bits [95:64] of AES Channel Status

Channel Status Register 4 (0x54)

Table 51: **Channel Status Register 4 - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_status_4	RO	0	Bits [127:96] of AES Channel Status

Channel Status Register 5 (0x58)

Table 52: **Channel Status Register 5 - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_status_5	R	0	Bits [159:128] of AES Channel Status

Channel Status Register 6 (0x5C)

Table 53: **Channel Status Register 6 - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	chan_status_6	RO	0	Bits [191:160] of AES Channel Status

Active Channel Status Register (0x60)

Table 54: **Active Channel Status Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	act_chan_stat	RO	0	Active channel information decoded from audio control packet. • Bit [0] – Channel 1 • Bit [1] – Channel 2 through • Bit [31] – Channel 32

Sample Rate Status Register (0x70)

Table 55: **Sample Rate Status Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:0	smpl_rate_stat	RO	0	Sample rate information decoded from audio control packet (0 – 48 KHz, 1 – 44.1 KHz, 2 – 32 KHz, 3 – Reserved) • Bit [1:0] – Channel 1 & 2 • Bit [3:2] – Channel 3 & 4 through • Bit [31:30] - Channel 31 & 32

Async Channel Pair Status Register (0x80)

Table 56: **Async Channel Pair Status Register - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
15:0	asx_stat	RO	0	ASX information decoded from audio control packet (0 - Synchronous audio & 1 - Asynchronous audio) • Bit [0] – Channel 1 & 2 Asx • Bit [1] – Channel 3 & 4 Asx through • Bit [15] - Channel 31 & 32 Asx
31:16	Reserved	RO	0	Reserved

GUI Parameters (0xFC)

Table 57: **GUI Parameters - UHD-SDI Audio (Extract)**

Bit	Field Name	Access Type	Default Value	Description
31:12	reserved	N/A	0	Reserved
11	gui_per_group_axis	RO	0	Core is configured with per group AXI4-S • 0 - Disabled • 1 – Enabled
10	gui_clk_phase	RO	1	Core is configured with clock phase logic • 0 - Disabled • 1 – Enabled
9	gui_aes_chan_stat	RO	1	Core is configured with AES channel status extraction • 0 - Disabled • 1 – Enabled
8	gui_sdi_aud_stat	RO	1	Core is configured with SDI audio status extraction • 0 - Disabled • 1 – Enabled
7	gui_axilite	RO	1	Core is configured with AXI4-Lite • 0 - Disabled • 1 – Enabled
6	gui_aud_function	RO	1	Core is configured with audio function set to • 0 - Embed • 1 – Extract
5:4	gui_uhdsdi_std	RO	2	Core is configured with UHD SDI mode set to • 0 - 3G_SDI • 1 - 6G_SDI • 2 - 12G_SDI_8DS • 3 - 12G_SDI_16DS

Table 57: **GUI Parameters - UHD-SDI Audio (Extract)** *(cont'd)*

Bit	Field Name	Access Type	Default Value	Description
3:0	gui_max_audio_chan	RO	7	Core is configured with maximum audio channels set to • 0 – 2 Channels • 1 – 4 Channels • 2 – 6 Channels • 3 – 8 Channels • 4 – 10 Channels • 5 – 12 Channels • 6 – 14 Channels • 7 – 16 Channels • 8 – 32 Channels

Designing with the Core

Clocking

The list of clocks in UHD-SDI Audio (Embed).

- **s_axi_aclk:** This is the processor domain clock. AXI4-Lite interface works on this clock.
- **s_axis_clk:** This is the AXI4-Stream interface clock. This should be greater than 512 times the audio sampling rate.
- **sdi_embed_clk:** This is the video domain clock. It is 74.25 MHz or 74.175 MHz during HD SDI, 148.5 MHz or 148.35 MHz during SD/3G/6G SDI and 297 MHz during 12G SDI mode. This is the same clock connected to `sdi_tx_clk` of the Xilinx® UHD-SDI TX Subsystem.

The list of clocks in UHD-SDI Audio (Extract).

- **s_axi_aclk:** This is the processor domain clock. AXI4-Lite interface works on this clock.
- **m_axis_clk:** This is the AXI4-Stream interface clock. This should be greater than 512 times the audio sampling rate.
- **sdi_extract_clk :** This is the video domain clock. It is 74.25 MHz or 74.175 MHz during HD SDI, 148.5 MHz or 148.35 MHz during SD/3G/6G SDI and 297 MHz during 12G SDI mode. This is the same clock connected to `sdi_rx_clk` of the Xilinx UHD-SDI RX Subsystem.

Resets

The UHD-SDI Audio (Embed) uses the following resets.

- **`s_axi_aresetn`:** This is an Active-Low AXI4-Lite interface reset. This reset brings the core registers set and the interrupts to the default state.
- **`s_axis_resetn`:** This is an Active-Low AXI4-Stream interface reset. This resets the entire logic working on `s_axis_clk`
- **`sdi_embed_reset`:** This is an Active-High video domain reset. This resets the entire core except for the core register set and the interrupts.

- **Soft Reset:** Two soft resets are provided apart from the reset ports mentioned above (Offset - 0x04).
  - The `config_reset` resets the core register set and the interrupts (equivalent to s_axi_aresetn)
  - The `core_reset` resets the entire core except for the core register set and the interrupts (equivalent to the `sdi_embed_reset`).

Note: When switching between video resolutions, there is a strict requirement to keep UHD-SDI Audio (Embed) under reset. It is recommended to follow the below sequence of steps.

1. Assert `core_reset` or de-assert `module_en`.
2. Change video resolution to be sent on SDI TX.
3. Modify the configuration in SDI Embed (if any).
4. De-assert `core_reset` or assert `module_en`.

The UHD-SDI Audio (Extract) uses the following resets.

- **`s_axi_aresetn`:** This is Active-Low AXI4-Lite interface reset. This reset brings the core registers set and the interrupts to the default state.
- **`m_axis_resetn`:** This is an Active-Low AXI4-Stream interface reset. This resets the entire logic working on `m_axis_clk`.
- **`sdi_extract_reset`:** This is an Active-High video domain reset. This resets the entire core except for the core register set and the interrupts.
- **Soft Reset:** Two soft resets are provided apart from the reset ports mentioned above (Offset - 0x04).
  - The `config_reset` signal resets the core register set and the interrupts (equivalent to `s_axi_aresetn`).
  - The `core_reset` signal resets the entire core except for the core register set and the interrupts (equivalent to the `sdi_extract_reset`).

Programming Sequence

The following programming sequence to enable embedding of audio onto the SDI stream:

1. Configure the video resolution in SDI TX.
2. After the video from SDI TX is stable, configure UHD-SDI Audio (Embed).
   - 0x14 - 0x0001_01B0 (Enable external line number and configure the video resolution. In this case it is 1920x1080p60)

- 0x18 - 0x0000_0008 (48 KHz audio with 24-bit precision)
- 0x20 - 0xFFFF_FFFF (Enable embedding of all the channels)
- 0x04 - 0x0000_0000 (Bring the system out of reset)
- 0x00 - 0x0000_0001 (Module enable to start embedding of audio data onto SDI)

3. If you want to change the video resolution, reset or disable the UHD-SDI Audio (Embed).
   - 0x04 - 0x0000_0002 (Keep the system in reset)
   - 0x00 - 0x0000_0000 (Module disable)
4. Repeat from step 1.

The following programming sequence to enable extraction of audio from the SDI stream.

1. Read the status of the incoming audio (Optional).
   - 0x0C – 0x0000_0100 (Enable audio status update interrupt).
   - As part of the ISR, check for the presence of audio data on the incoming SDI stream (read - 0x40).
   - If the audio data is present, read the sample rate and active channel information.
   - Disable the interrupt after reading all the information (if not disabled, audio status update interrupt comes once for each frame).
   - Enable other interrupts to detect change in any of the information you are interested in (sample rate change, active channel change, active group change, etc.).
2. Configure the UHD-SDI Audio (Extract).
   - 0x20 - 0xFFFF_FFFF (Enable extraction of all the channels).
   - 0x04 - 0x0000_0000 (Bring the system out of reset).
   - 0x00 - 0x0000_0001 (Module enable to start extraction of audio data from SDI).

Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis, and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the **Customize IP** command from the toolbar or right-click menu.

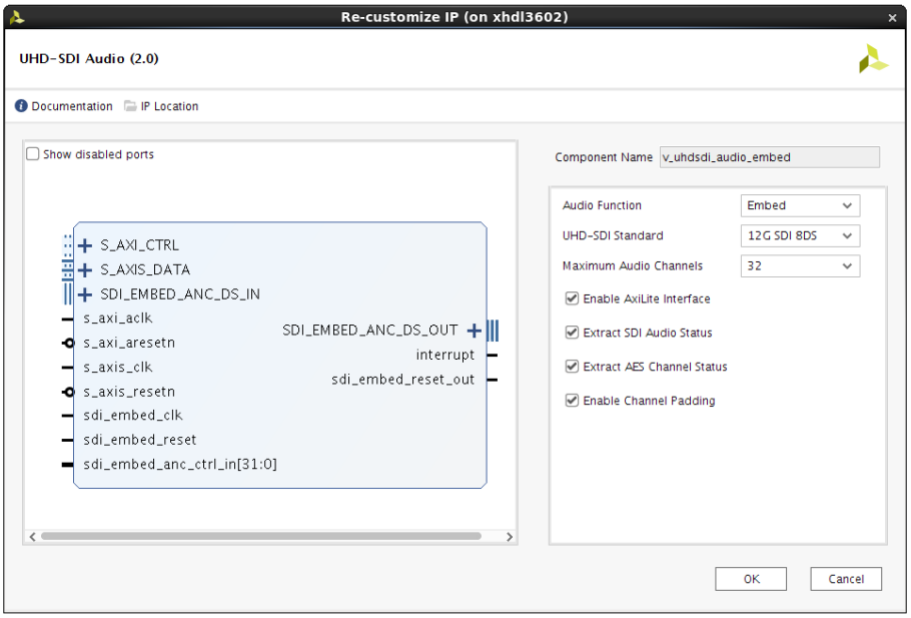
For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Configuration for Audio Embed Function

The following figure shows the Customize IP dialog box with information about customizing parameters for the UHD-SDI Audio (Embed).

Figure 9: **Re-customize IP**



- **Component Name:** Enter a name for the core instance. The Component Name is the base name of the output files generated for this core. This example uses the name v_uhdsdi_audio_embed.
- **Audio Function:** Specifies the Audio Function. Available options:
  - Embed
  - Extract
- **UHD-SDI Standard:**

  Specifies the maximum line rate that should be supported. For 7 series speed grade 3, UltraScale and UltraScale+ devices, the available options are:

  - 3G SDI
  - 6G SDI
  - 12G SDI 8DS
  - 12G SDI 16DS

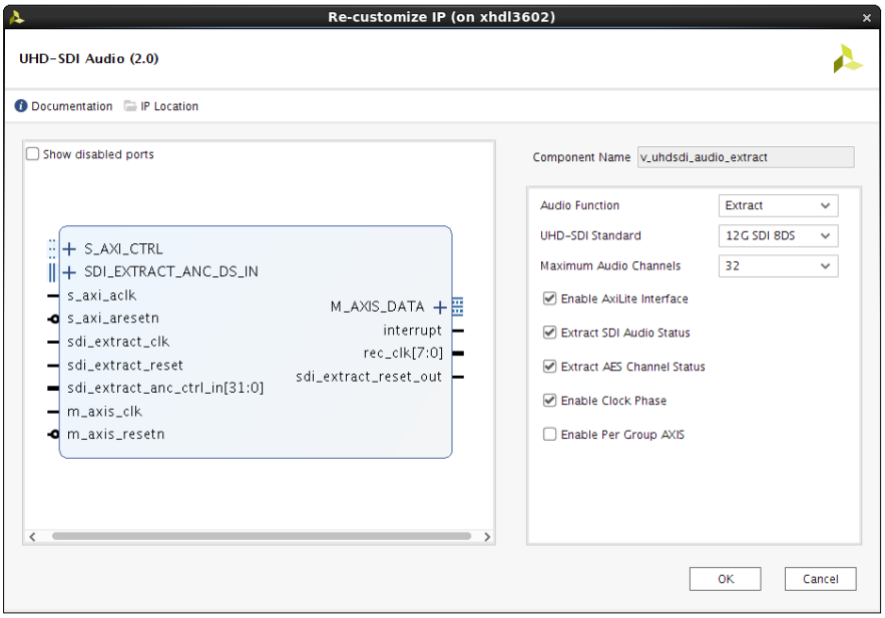
  For 7 series speed grade 1 and 2 devices, the available options are:

  - 3G SDI
  - 6G SDI
- **Maximum Audio Channels:** Specifies the maximum number of audio channels that should be supported by the UHD-SDI Audio (Embed) IP core. Available options:
  - 2 (Audio can only be embedded onto group 1)
  - 4 (Audio can only be embedded onto group 1)
  - 6 (Audio can only be embedded onto group 1 & 2)
  - 8 (Audio can only be embedded onto group 1 & 2)
  - 10 (Audio can only be embedded onto group 1, 2 & 3)
  - 12 (Audio can only be embedded onto group 1, 2 & 3)
  - 14 (Audio can only be embedded onto group 1, 2, 3 & 4)
  - 16 (Audio can only be embedded onto group 1, 2, 3 & 4)
  - 32 (Audio can only be embedded onto group 1, 2, 3, 4, 5, 6, 7 & 8)
- **Enable AXI4-Lite Interface:** when enabled, the AXI4-Lite interface is used for configuration. If it is not enabled, port based interface is chosen.
- **Extract SDI Audio Status:** when enabled, UHD-SDI Audio (Embed) IP core reports the status of audio data present on the incoming SDI stream.
- **Extract AES Channel Status:** when enabled, UHD-SDI Audio (Embed) IP core extracts 192 bit AES channel status.
- **Enable Channel Padding:** when enabled, UHD-SDI Audio (Embed) IP core converts non-multiple of four channel AXI4-S transactions (2, 6, 10, etc.) to multiples of 4 channels (4, 8, 12, etc.) by stuffing the remaining two channels with mute data.

Configuration for Audio Extract Function

The following figure shows the Customize IP dialog box with information about customizing parameters for the UHD-SDI Audio (Extract).

Figure 10: **Re-customize IP**



- **Component Name:** Enter a name for the core instance. The Component Name is the base name of the output files generated for this core. This example uses the name v_uhdsdi_audio_embed.
- **Audio Function:** Specifies the Audio Function. Available options:
  - Embed
  - Extract
- **UHD-SDI Standard:** Specifies the maximum line rate that should be supported. For 7 series speed grade 3, UltraScale and UltraScale+ devices, the available options are:
  - 3G SDI
  - 6G SDI
  - 12G SDI 8DS
  - 12G SDI 16DS

  For 7 series speed grade 1 and 2 devices, the available options are:
  - 3G SDI
  - 6G SDI
- **Maximum Audio Channels:** Specifies the maximum number of audio channels that should be supported by the UHD-SDI Audio (Extract) IP core. Available options:
  - 2 (Audio can only be extracted from group 1)

- 4 (Audio can only be extracted from group 1)
- 6 (Audio can only be extracted from group 1 & 2)
- 8 (Audio can only be extracted from group 1 & 2)
- 10 (Audio can only be extracted from group 1, 2 & 3)
- 12 (Audio can only be extracted from group 1, 2 & 3)
- 14 (Audio can only be extracted from group 1, 2, 3 & 4)
- 16 (Audio can only be extracted from group 1, 2, 3 & 4)
- 32 (Audio can only be extracted from group 1, 2, 3, 4, 5, 6, 7 & 8)

- **Enable AXI4-Lite Interface:** When enabled, the AXI4-Lite interface is used for configuration. If it is not enabled, port based interface is chosen.
- **Extract SDI Audio Status:** When enabled, UHD-SDI Audio (Extract) IP core reports the status of the audio data present on the incoming SDI stream.
- **Extract AES Channel Status:** When enabled, UHD-SDI Audio (Extract) IP core extracts 192 bit AES channel status.
- **Enable Clock Phase:** When enabled, UHD-SDI Audio (Extractor) IP core uses clock phase data to output the audio sample on AXI4-S interface.
- **Enable Per Group AXIS:** When enabled, UHD-SDI Audio (Extract) IP core outputs audio data on multiple AXI4-S interfaces. Each AXI4-S interface carries data for one audio group.

User Parameters

The following table shows the relationship between the fields in the Vivado® IDE and the user parameters (which can be viewed in the Tcl Console).

Table 58: **User Parameters**

Vivado IDE Parameter/Value[1]	User Parameter/Value	Default Value
Audio Function	C_AUDIO_FUNCTION	Embed
UHD-SDI Standard	C_LINE_RATE	12G SDI 8DS
Maximum Audio Channels	C_MAX_AUDIO_CHANNELS	16
Enable AxiLite Interface	C_INCLUDE_AXILITE	True
Extract SDI Audio Status	C_SDI_AUD_STAT_EXT	True
Extract AES Channel Status	C_AES_CHAN_STAT_EXT	True
Enable Channel Padding	C_ENABLE_CHANNEL_PADDING	True
Enable Clock Phase	C_ENABLE_CLOCK_PHASE	True

Table 58: **User Parameters** *(cont'd)*

Vivado IDE Parameter/Value[1]	User Parameter/Value	Default Value
Enable Per Group AXIS	C_ENABLE_PER_GROUP_AXIS	False

Notes:

1. Parameter values are listed in the table where the Vivado IDE parameter value differs from the user parameter value. Such values are shown in this table as indented below the associated parameter.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Constraining the Core

Required Constraints

The period of the sdi_embed_clk and sdi_extract_clk must be constrained depending on the maximum line rate to be supported. Also, the period of the AXI4-Stream and AXI4-Lite clocks must be constrained based on the system design.

Device, Package, and Speed Grade Selections

For 7 series devices, -3 speed grade parts are required to support 12G-SDI. Not all packages support 12G-SDI line rates. The MGTAVCC voltage rail must be set to 1.05V if 12G-SDI operation is required. This voltage level also supports the other SDI lines rates. If the maximum line rate is 6G-SDI or slower, then -1 speed grade devices are sufficient and the MGTAVCC voltage rail can be set to the normal value of 1.00V.

UltraScale/UltraScale+ GTH/GTY transceivers support operation at all SDI rates up to and including 12G-SDI in -1 speed grade devices.

Clock Frequencies

The source of the sdi_embed_clk is usually the serial transceiver's TXOUTCLK. The source of the sdi_extract_clk is usually the serial transceiver's RXOUTCLK. The exact constraints to be used on these clocks depends on the hierarchical structure of the design, but they would be similar to the constraints shown below with an application specific path to the TXOUTCLK and RXOUTCLK pins of the serial transceiver.

Applications that support 12G-SDI operation must constrain the frequency of the UHD-SDI Audio IP core's sdi_embed_clk and sdi_extract_clk to 297 MHz.

create_clock -period 3.367 -name tx0_outclk -waveform {0.000 1.683} [get_pins SDI/GTX/gtxe2_i/TXOUTCLK]

create_clock -period 3.367 -name rx0_outclk -waveform {0.000 1.683} [get_pins SDI/GTX/gtxe2_i/RXOUTCLK]

When the maximum line rate is 6G-SDI or slower, the maximum clock frequency of sdi_embed_clk and sdi_extract_clk is 148.5 MHz and the constraints below would be appropriate:

create_clock -period 6.734 -name tx0_outclk -waveform {0.000 3.367} [get_pins SDI/GTX/gtxe2_i/TXOUTCLK]

create_clock -period 6.734 -name rx0_outclk -waveform {0.000 3.367} [get_pins SDI/GTX/gtxe2_i/RXOUTCLK]

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Example Design

Example design support is not available for the UHD-SDI Audio IP core. However, example design is available for SMPTE UHD-SDI RX Subsystem. As part of the example design for SMPTE UHD-SDI RX Subsystem demonstration, the UHD-SDI Audio IP core is used to embed and extract audio data. For more details on the options and features available, refer to the Example Design section of the *SMPTE UHD-SDI RX Subsystem Product Guide* (PG290).

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Chapter 7

Verification, Compliance, and Interoperability

The UHD-SDI Audio IP core has been verified using simulation and hardware testing. A highly parameterized transaction-based simulation test suite was used to verify the core.

The tests include:

- Different SDI modes and video resolutions
- Different audio sample rates
- Register read and write access

Hardware Testing

The UHD-SDI Audio IP core has been tested with standard off-the-shelf SDI test equipment. The following table lists different video resolutions on which 48 KHz audio is validated.

Video Resolution	SDI Mode	SDI Source and Sink	Audio Channels
720x576i50	SD-HDI	Omnitek/Phabrix SXE	16
720x486i59.94	SD-HDI	Omnitek/Phabrix SXE	16
1920x1080i47.95	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080i48	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080i50	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080i59.94	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080i60	HD-SDI	Omnitek/Phabrix Qx	16
2048x1080i47.95	HD-SDI	Omnitek/Phabrix Qx	16
2048x1080i48	HD-SDI	Omnitek/Phabrix Qx	16
2048x1080i50	HD-SDI	Omnitek/Phabrix Qx	16
2048x1080i59.94	HD-SDI	Omnitek/Phabrix Qx	8
2048x1080i60	HD-SDI	Omnitek/Phabrix Qx	8
1280x720p25	HD-SDI	Omnitek/Phabrix Qx	16
1280x720p29.97	HD-SDI	Omnitek/Phabrix Qx	16
1280x720p30	HD-SDI	Omnitek/Phabrix Qx	16

Video Resolution	SDI Mode	SDI Source and Sink	Audio Channels
1280x720p50	HD-SDI	Omnitek/Phabrix Qx	16
1280x720p59.94	HD-SDI	Omnitek/Phabrix Qx	16
1280x720p60	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080p23.98	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080p24	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080p25	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080p29.97	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080p30	HD-SDI	Omnitek/Phabrix Qx	16
1920x1080sF23.98	HD-SDI	Omnitek	16
1920x1080sF24	HD-SDI	Omnitek	16
1920x1080sF25	HD-SDI	Omnitek	16
1920x1080sF29.97	HD-SDI	Omnitek	16
1920x1080sF30	HD-SDI	Omnitek	16
2048x1080p23.98	HD-SDI	Omnitek/Phabrix Qx	16
2048x1080p24	HD-SDI	Omnitek/Phabrix Qx	16
2048x1080p25	HD-SDI	Omnitek/Phabrix Qx	16
2048x1080p29.97	HD-SDI	Omnitek/Phabrix Qx	8
2048x1080p30	HD-SDI	Omnitek/Phabrix Qx	8
2048x1080sF23.98	HD-SDI	Omnitek	16
2048x1080sF24	HD-SDI	Omnitek	16
2048x1080sF25	HD-SDI	Omnitek	16
2048x1080sF29.97	HD-SDI	Omnitek	8
2048x1080sF30	HD-SDI	Omnitek	8
1920x1080p47.95	3G-A	Phabrix Qx	32
1920x1080p48	3G-A	Phabrix Qx	32
1920x1080p50	3G-A	Phabrix Qx	32
1920x1080p59.94	3G-A	Phabrix Qx	32
1920x1080p60	3G-A	Phabrix Qx	32
2048x1080p47.95	3G-A	Phabrix Qx	32
2048x1080p48	3G-A	Phabrix Qx	32
2048x1080p50	3G-A	Phabrix Qx	32
2048x1080p59.94	3G-A	Phabrix Qx	16
2048x1080p60	3G-A	Phabrix Qx	16
1920x1080p47.95	3G-B DL	Omnitek	16
1920x1080p48	3G-B DL	Omnitek	16
1920x1080p50	3G-B DL	Omnitek	16
1920x1080p59.94	3G-B DL	Omnitek	16
1920x1080p60	3G-B DL	Omnitek	16
2048x1080p47.95	3G-B DL	Omnitek	16
2048x1080p48	3G-B DL	Omnitek	16

Video Resolution	SDI Mode	SDI Source and Sink	Audio Channels
2048x1080p50	3G-B DL	Omnitek	16
2048x1080p59.94	3G-B DL	Omnitek	8
2048x1080p60	3G-B DL	Omnitek	8
3840x2160p23.98	6G-SDI	Omnitek/Phabrix Qx	32
3840x2160p24	6G-SDI	Omnitek/Phabrix Qx	32
3840x2160p25	6G-SDI	Omnitek/Phabrix Qx	32
3840x2160p29.97	6G-SDI	Omnitek/Phabrix Qx	32
3840x2160p30	6G-SDI	Omnitek/Phabrix Qx	32
4096x2160p23.98	6G-SDI	Omnitek/Phabrix Qx	32
4096x2160p24	6G-SDI	Omnitek/Phabrix Qx	32
4096x2160p25	6G-SDI	Omnitek/Phabrix Qx	32
4096x2160p29.97	6G-SDI	Omnitek/Phabrix Qx	16
4096x2160p30	6G-SDI	Omnitek/Phabrix Qx	16
3840x2160p47.95	12G-SDI	Phabrix Qx	16
3840x2160p48	12G-SDI	Phabrix Qx	16
3840x2160p50	12G-SDI	Phabrix Qx	16
3840x2160p59.94	12G-SDI	Phabrix Qx	16
3840x2160p60	12G-SDI	Phabrix Qx	16
4096x2160p47.95	12G-SDI	Phabrix Qx	16
4096x2160p48	12G-SDI	Phabrix Qx	16
4096x2160p50	12G-SDI	Phabrix Qx	16
4096x2160p59.94	12G-SDI	Phabrix Qx	16
4096x2160p60	12G-SDI	Phabrix Qx	16

***Note*:** Due to the limitation in the test equipment, only 16-Channel is validated in 12G-SDI mode but the IP supports 32 channels in 12G-SDI mode.

Appendix A

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools.

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT! *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support. The Xilinx Community Forums are also available where members can learn, participate, share, and ask questions about Xilinx solutions.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the UHD SDI Audio Core

AR 70290.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Debug Tools

There are many tools available to address design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx® devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Hardware Debugging

General Checks

Perform the following general checks:

- Ensure that all timing constraints were met during implementation.
- Verify that all clocks are connected with expected frequencies.
- Verify that all resets are connected with expected polarities.

Core Generation

Ensure that core is generated with expected configuration (Audio function, SDI line rate, Maximum audio channels, Axi4-Lite enable, etc) by reading the “GUI Parameters” register (Offset - 0xFC).

AXI4-Stream Slave Interface

Ensure that audio samples are strictly distributed as per the sample rate. One sample per each channel per one audio clock period (48 KHz, 44.1 KHz, 32 KHz).

SDI Transmitter Ancillary Data Control

Perform the following checks.

- The Audio Embedder receives video data streams from SDI Transmitter, embeds audio and transmits the audio embedded video data streams back to the SDI Transmitter core.

- The Xilinx® SDI Transmitter has the provision to use the video data streams or audio embedded video data streams (ancillary data).
- If Audio Embedder is embedding the audio data and the audio data is not visible on the SDI link, ensure that the SDI Transmitter is configured to use the ancillary data path.

Core Status

After all the configuration is done, if the UHD-SDI Audio IP core is not working as expected, ensure that core is out of reset by probing `sdi_embed_reset_out` and `sdi_extract_reset_out` signals..

XILINX

Appendix B

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this product guide:

1. *Vivado Design Suite: AXI Reference Guide* (UG1037)
2. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
3. *Vivado Design Suite User Guide: Designing with IP* (UG896)
4. *Vivado Design Suite User Guide: Getting Started* (UG910)
5. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
6. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
7. *Xilinx® SMPTE UHD-SDI RX Subsystem Product Guide* (PG290)
8. *Xilinx® SMPTE UHD-SDI TX* (PG289)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
12/01/2021 Version 2.0	
IP Facts	Updated.
12/05/2018 Version 2.0	
General updates.	• Update to version v2.0. • Added support for 7-series devices.
Features	Added 32-channel support.
Core Overview	Modified the architecture to reduce resource utilization.
AXI4-Lite Slave	New feature.
Channel Padding Logic	New feature.
Clock Phase Logic	New feature.
04/04/2018 Version 1.0	
Initial Xilinx® release.	N/A

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