SMPTE SD/HD/3G-SDI 3.0

LogiCORE IP Product Guide

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Introduction

The serial digital interface (SDI) family of standards from the Society of Motion Picture and Television Engineers (SMPTE) is widely used in professional broadcast video equipment. The Xilinx LogiCORE™ IP SMPTE SD/HD/3G-SDI core interfaces are used by broadcast studios and video production centers to carry uncompressed digital video along with embedded ancillary data such as multiple audio channels. The SMPTE SD/HD/3G-SDI core implements interfaces for the SDI family of standards.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Kintex® UltraScale™ and Virtex® UltraScale, Zynq®-7000, Artix®-7, Virtex-7, Kintex-7
Resources	See Table 2-2.
Provided with Core	
Documentation	Product Guide
Design Files	Verilog source code
Example Design	Provided Separately (2) See XAPP592 [Ref 8] and XAPP1097 [Ref 15]
Test Bench	Verilog
Constraints File	XDC
Simulation Models	Verilog Structural
Supported Software Drivers	Not Applicable
Tested Design Flows	
Design Entry Tools	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis Tools	Vivado Synthesis
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the Vivado IP Catalog.
2. Example designs are provided in FPGA device-specific application notes
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Features

- Standards compliance:
  - SMPTE ST 259 (SD-SDI)
  - SMPTE ST 292 (HD-SDI)
  - SMPTE ST 372 (Dual Link HD-SDI)
  - SMPTE ST 424 and ST 425-1 (3G-SDI) including levels A, B-DL, and B-DS
  - SMPTE ST 352 (Payload ID)
  - SMPTE RP 165 (SD-SDI EDH)
- Triple-Rate SDI receiver features:
  - A single reference clock frequency supports reception of five different bit rates:
    - 270 Mb/s SD-SDI
    - 1.485 Gb/s HD-SDI
    - 1.485/1.001 Gb/s HD-SDI
    - 2.97 Gb/s 3G-SDI
    - 2.97/1.001 Gb/s 3G-SDI
  - Automatically detects incoming SDI standard and bit rate

  - Automatically detects incoming video transport format
  - Detects and captures ST 352 packets
  - Checks for CRC errors for HD-SDI and 3G-SDI
  - Optionally checks for EDH errors for SD-SDI
- Triple-Rate SDI transmitter features:
  - Only two reference clock frequencies are required to transmit five different bit rates:
    - 270 Mb/s SD-SDI
    - 1.485 Gb/s HD-SDI
    - 1.485/1.001 Gb/s HD-SDI
    - 2.97 Gb/s 3G-SDI
    - 2.97/1.001 Gb/s 3G-SDI
  - Generates and inserts CRC and line numbers for HD-SDI and 3G-SDI
  - Generates and inserts EDH packets for SD-SDI
  - Generates and inserts ST 352 packets for all SDI standards

Overview

SMPTE Interface Standards

The SMPTE SD/HD/3G-SDI core implements three main SMPTE interface standards:

- SD-SDI (SMPTE ST 259): SDTV Digital Signal/Data - Serial Digital Interface
- HD-SDI (SMPTE ST 292-1): 1.5 Gb/s Signal/Data Serial Interface
- 3G-SDI (SMPTE ST 424): 3 Gb/s Signal/Data Serial Interface

In addition, two SMPTE SDI receivers or transmitters can be combined to implement SMPTE ST 372 Dual Link HD-SDI interfaces.

SD-SDI

The SMPTE SD/HD/3G-SDI core is designed to support the 270 Mb/s bit rate (level C) of the SD-SDI standard.

The SMPTE SD/HD/3G-SDI core fully supports the SMPTE RP 165 Error Detection and Handling (EDH) standard for the receive and transmit sections.

HD-SDI

Although this standard is called a 1.5 Gb/s interface, the bit rates supported by HD-SDI are actually 1.485 Gb/s and 1.485/1.001 Gb/s. The SMPTE SD/HD/3G-SDI core fully supports both of these bit rates. The SMPTE SD/HD/3G-SDI core also fully supports generation (TX-side) and checking (RX-side) of CRC values for each video line and the insertion (TX-side) and capture (RX-side) of line number values for each line.

3G-SDI

This standard is called a 3 Gb/s interface, but the actual bit rates are 2.97 Gb/s and 2.97/1.001 Gb/s. The SMPTE SD/HD/3G-SDI core fully supports both of these bit rates. 3G-SDI supports several different mapping levels, described in the SMPTE ST 425-1 standard. These levels are called A, B-DL, and B-DS. The SMPTE SD/HD/3G-SDI core supports all three of

these levels. As with the HD-SDI standard, the SMPTE SD/HD/3G-SDI core supports CRC generation and checking and line number insertion and capture for 3G-SDI.

Payload ID

The SMPTE SD/HD/3G-SDI core implements a SMPTE ST 352 payload ID ancillary data packet insertion capability for the transmitter that works in all SDI modes (SD-SDI, HD-SDI, 3G-SDI, and dual link HD-SDI). The receive side also detects and captures the four data bytes of ST 352 payload ID packets.

Ancillary Data Support

The SMPTE SD/HD/3G-SDI core allows the application to implement ancillary data packet insertion prior to transmission. While the core doesn't provide ancillary data packet insertion capability, except for ST 352 payload ID packets, it has the necessary data paths to allow ancillary data packet insertion to be implemented by the application. On the receive side, all embedded ancillary data is preserved by the SMPTE SD/HD/3G-SDI core's receiver section and is present in the SDI data streams output from the core. Applications can process the received SDI data streams to receive and/or modify the ancillary data as needed.

Complete SMPTE SDI Interface Solution

A complete SMPTE SDI interface is comprised of:

- A multi-rate SDI-compliant transceiver
- The SMPTE SD/HD/3G-SDI core
- Control logic for the transceiver
- Industry standard SDI cable driver (for TX) and SDI cable equalizer (for RX)
- Transceiver reference clock source(s)

Figure 1-1 shows a high-level block diagram of an SDI receive/transmit interface using the SMPTE SD/HD/3G-SDI core. In this figure, a transceiver internal to the Xilinx FPGA is used with the SMPTE SD/HD/3G-SDI core.

The SMPTE SD/HD/3G-SDI core implements one SDI receiver and one SDI transmitter. If only a receiver or only a transmitter is needed by the application, the input ports for the unused half of the core can be tied to ground and the output ports left unconnected. The synthesis tool will optimize the unused portion of the core out of the application.

When both the receiver and transmitter sections of the SMPTE SD/HD/3G-SDI core are used, the receiver and transmitter are completely independent. They can be operating in different SDI modes and bit rates (receiving 3G-SDI at 2.97/1.001 Gb/s while transmitting SD-SDI at 270 Mb/s or HD-SDI at either bit rate, for example).

The SMPTE SD/HD/3G-SDI core always supports all three SDI modes (SD-SDI, HD-SDI, and 3G-SDI). If only a subset of these modes is required by an application, the full SMPTE SD/HD/3G-SDI core is still used.

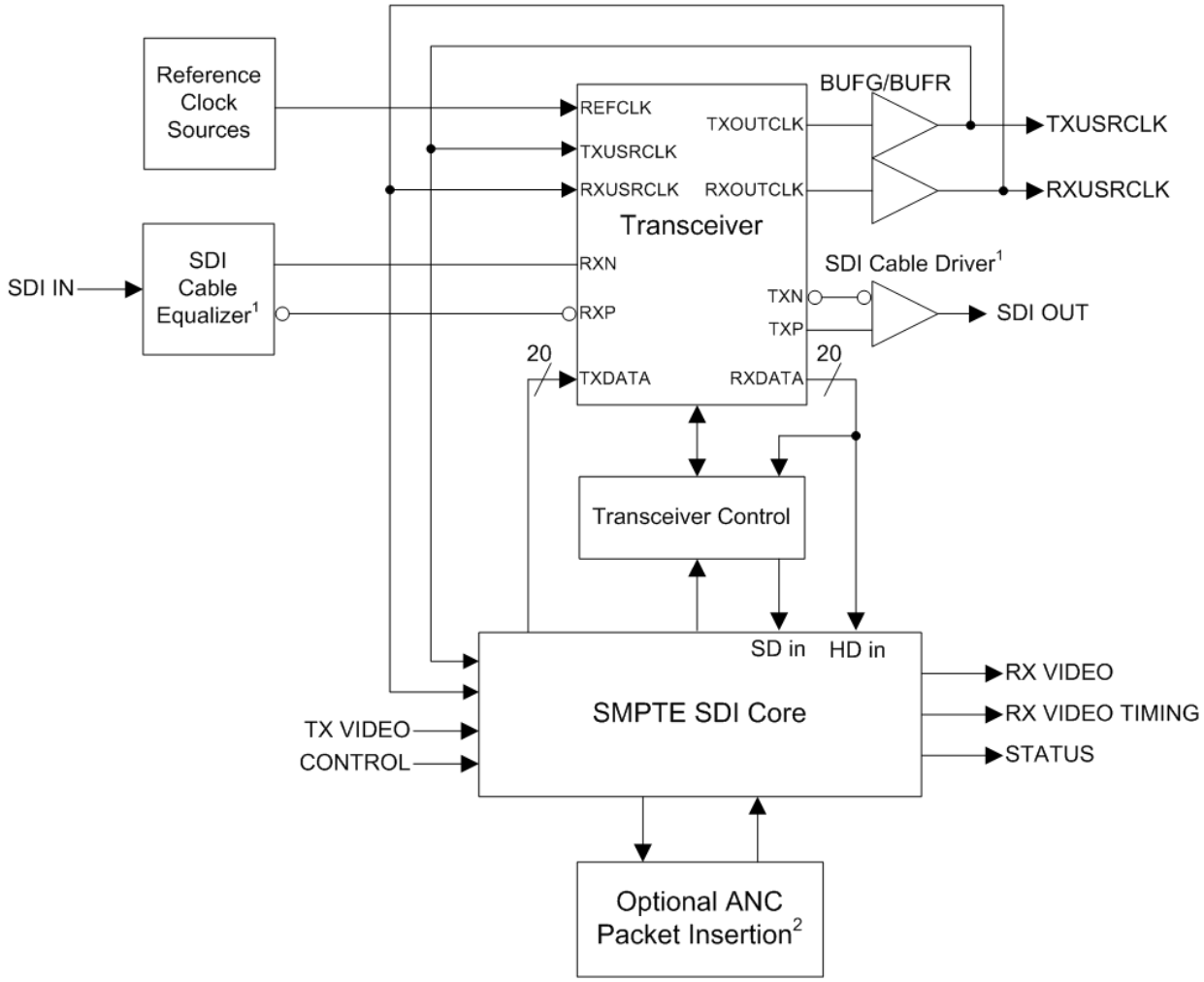

Figure 1-1: **Overview of a Complete SMPTE SDI Interface**

1. SDI cable equalizer and cable driver are external to the FPGA.
2. The optional ANC packet insertion function is not included with the SMPTE SD/HD/3G-SDI core.

Feature Summary

The Xilinx SMPTE SD/HD/3G-SDI IP core implements the data path for SDI receivers and transmitters. A complete SDI interface implementation consists of the SMPTE SD/HD/3G-SDI core, a transceiver (internal to the FPGA or external), and control logic associated with the transceiver. The SMPTE SD/HD/3G-SDI core supports SD-SDI, HD-SDI, and 3G-SDI (level A, level B-DL, and level B-DS) and dual link HD-SDI standards. The SMPTE SD/HD/

3G-SDI core will initially be validated with the GTX transceivers in Kintex-7, Virtex-7 FPGA, and Zynq-7000 devices.

Applications

- Professional broadcast cameras
- Professional digital video recorders
- Professional video processing equipment
- Medical imaging

Licensing

The SMPTE SD/HD/3G-SDI core is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Standards

See SMPTE Interface Standards for standards compliance information.

Supported Video Formats

Table 2-1 shows the video formats that are supported by the LogiCORE IP SMPTE SD/HD/3G-SDI core.

Table 2-1: **Supported Video Formats**

Interface	Video Standard	Sampling Structure / Bit Depth	Frame/Field Rate (Hz)
SD-SDI SMPTE 259-C	PAL	4:2:2 Y'C_B'C_R' 10-bit or 8-bit	50
	NTSC	4:2:2 Y'C_B'C_R' 10-bit or 8-bit	59.94
HD-SDI SMPTE 292	SMPTE 274	4:2:2 Y'C_B'C_R' 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:2:2 Y'C_B'C_R' 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 260	4:2:2 Y'C_B'C_R' 10-bit	1035i: 59.94, 60
	SMPTE 2048-2	4:2:2 Y'C_B'C_R' 10-bit	1080p: 23.98, 24, 25, 29.97, 30

Table 2-1: **Supported Video Formats *(Cont'd)***

Interface	Video Standard	Sampling Structure / Bit Depth	Frame/Field Rate (Hz)
3G-SDI Level A SMPTE 425-A	SMPTE 274	4:2:2 Y'C_B'C_R' 10-bit	1080p: 50, 59.94, 60
		4:4:4 Y'C_B'C_R' or RGB 10-bit 4:4:4:4 Y'C_B'C_R'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:4:4 or 4:4:4:4 Y'C_B'C_R' or RGB 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 428-9	4:4:4 X'Y'Z' 12-bit	1080p: 24 1080PsF: 24
	SMPTE 428-19	4:4:4 X'Y'Z' 12-bit	1080p: 25, 30 1080PsF: 25, 30
	SMPTE 2048-2	4:2:2 Y'C_B'C_R' 10-bit	1080p: 47.95, 48, 50, 59.94, 60
		4:4:4 Y'C_B'C_R' or RGB 10-bit 4:4:4:4 Y'C_B'C_R'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit 4:2:2:4 Y'C_B'C_R'A 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
3G-SDI Level B-DL SMPTE 425 B-DL	SMPTE 372	See Dual Link HD-SDI SMPTE 372.	
3G-SDI Level B-DS SMPTE 425 B-DS	2 X HD-SDI streams	See HD-SDI SMPTE 292.	

Table 2-1: **Supported Video Formats *(Cont'd)***

Interface	Video Standard	Sampling Structure / Bit Depth	Frame/Field Rate (Hz)
Dual Link HD-SDI SMPTE 372	SMPTE 274	4:2:2 Y'C_B'C_R' 10-bit	1080p: 50, 59.94, 60
		4:4:4 or 4:4:4:4 Y'C_B'C_R' or RGB 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 428-9	4:4:4 X'Y'Z' 12-bit	2048 X 1080p: 24
	SMPTE 428-19	4:4:4 X'Y'Z' 12-bit	1080p: 25, 30 1080PsF: 25, 30
	SMPTE 2048-2	4:2:2 Y'C_B'C_R' 10-bit	1080p: 47.95, 48, 50, 59.94, 60
		4:4:4 Y'C_B'C_R' or RGB 10-bit 4:4:4:4 Y'C_B'C_R'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit 4:2:2 Y'C_B'C_R'A 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30

Performance

The SMPTE SD/HD/3G-SDI core runs at the frequencies required to support the SDI standards. The maximum clock rate required for the SDI standards is 148.5 MHz. This clock rate is achievable in all supported device families and speed grades.

Resource Utilization

The information presented in Table 2-2 is a guide to the resource usage of the SMPTE SD/HD/3G-SDI core for Kintex-7, Virtex-7, and Zynq-7000 devices. Usage for various configurations of the core are shown.

Resource usage provided applies only to the SMPTE SD/HD/3G-SDI core. It does not include the transceiver, device-specific control logic, and the SD-SDI DRU that are required when implementing a complete SDI core using a transceiver in a Xilinx FPGA. For resource usage including these other pieces, refer to the Xilinx FPGA family-specific SDI application notes such as XAPP592 [Ref 8] for Kintex-7 devices and XAPP1097 [Ref 15] for Artix-7 devices.

Table 2-2: **Kintex-7, Virtex-7, and Zynq-7000 Devices**

Core Configuration	LUT-FF Pairs	LUTs	FFs	RAM 36/18	DSP48A1	Global Clocks
RX with EDH & TX	1866	1498	1263	0	0	2
RX w/o EDH & TX	1260	977	883	0	0	2
RX Only with EDH	1504	1192	1068	0	0	1
RX Only w/o EDH	897	686	688	0	0	1
TX Only	1348	1134	816	0	0	1

Core Architecture

This section describes the architecture of the SMPTE SD/HD/3G-SDI core.

SMPTE SD/HD/3G-SDI Core Top Level Module

The SMPTE SD/HD/3G-SDI core top level module implements two functions:

- SDI receiver
- SDI transmitter

Table 2-3 describes the ports of the SMPTE SD/HD/3G-SDI core's top level module.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports**

Port Name	I/O	Width	Description
Receive Ports			
rx_usrclk	In	1	This clock input connects to the recovered clock from the transceiver. The clock frequency must be 148.5 MHz (or 148.5/1.001 MHz) for 3G-SDI mode. It must be 74.25 MHz (or 74.25/1.001 MHz) for HD-SDI mode. When used with transceivers in Xilinx FPGAs, rx_usrclk is 148.5 MHz for SD-SDI mode, too. However, when used with external SDI transceivers, rx_usrclk can be 27 MHz in SD-SDI mode. Unless otherwise noted, all input and outputs of the core prefixed with "rx_" are synchronous with this clock.
rx_rst	In	1	This synchronous reset input usually can be tied to ground because a reset is not required. After FPGA configuration, the core is in a fully operational mode and does not require a reset. Note that both rx_ce_sd and rx_din_rdy_3G must be High when rx_rst is High in order to completely reset the receiver.
rx_data_in	In	20	The recovered data from the transceiver enters the core on this port in HD-SDI and 3G-SDI modes.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
rx_sd_data_in	In	10	The recovered data from the transceiver enters the core on this port in SD-SDI mode. When using the transceivers in Xilinx FPGAs, a data recovery unit (DRU) is used to recover the SD-SDI data stream from the oversampled data captured by the transceiver. The data output by the DRU enters the core on this port in SD-SDI mode.
rx_sd_data_strobe	In	1	In SD-SDI mode only, this port indicates to the core when a 10-bit data word is valid on the rx_sd_data_in port when it is High. This port is not used in HD-SDI and 3G-SDI modes. When using the transceivers in a Xilinx FPGA, this port is driven by the data ready output of the DRU that is recovering the SD-SDI data. This input port is used internally to the core to generate clock enables for the SD-SDI data path and the rx_ce_sd output signal.
rx_frame_en	In	1	This input enables the SDI framer function. When this input is High, the framer automatically readjusts the output word alignment to match the alignment of each timing reference signal (TRS). TRS is a generic term referring to both EAV and SAV sequences. Normally, this input should always be High. However, if controlled properly, this input can be used to implement TRS alignment filtering. For example, if the nsp output is connected to the rx_frame_en input, the framer ignores a single misaligned TRS, keeping the existing word alignment until the new word alignment is confirmed by a second matching TRS. It is important to turn off any TRS filtering during the synchronous switching lines by driving the rx_frame_en input High on the synchronous switching lines.
rx_mode_en	In	3	This port has unary bits to enable reception of each of the three SDI modes: Bit 0 enables HD-SDI mode Bit 1 enable SD-SDI mode Bit 2 enables 3G-SDI mode When a bit is High, the corresponding SDI mode is enabled. When a bit is low, the receiver will not attempt to detect incoming SDI signals of that mode. Disabling unused SDI modes using these bits will decrease the amount of time it takes for the receiver to lock to the incoming signal when it changes modes.
rx_mode	Out	2	This output port indicates the current SDI mode of the receiver: 00 = HD-SDI 01 = SD-SDI 10 = 3G-SDI When the receiver is not locked, the rx_mode port changes values as the receiver searches for the correct SDI mode. During this time, the rx_mode_locked output is Low. When the receiver detects the correct SDI mode, the rx_mode_locked output goes High.
rx_mode_hd rx_mode_sd rx_mode_3g	Out	1	These three output ports are decoded versions of the rx_mode port. They are provided for convenience. Unlike the rx_mode port, which changes continuously as the receiver seeks to identify and lock to the incoming signal, these outputs are all forced Low when the receiver is not locked. The output matching the current SDI mode of the receiver is High when rx_mode_locked is High.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
rx_mode_locked	Out	1	When this output is Low, the receiver is actively searching for the SDI mode that matches the input data stream. During this time, the rx_mode output port changes frequently. When the receiver locks to the correct SDI mode, the rx_mode_locked output goes High.
rx_mode_detect_en	In	1	This port enables the SDI mode detection feature of the core when High. When enabled, the SDI mode detector controls the receiver to search for and lock to the incoming SDI data stream. If a transceiver external to the FPGA is used, that transceiver may have such an auto detection feature built in so the SDI mode detection feature of the SD core can be disabled.
rx_forced_mode	In	2	When the rx_mode_detect_en input is Low, disabling the automatic SDI mode detection feature of the core, the core will operate in the SDI mode specified by the value on the rx_forced_mode port. 00 = HD-SDI 01 = SD-SDI 10 = 3G-SDI
rx_bit_rate	In	1	This input port indicates which bit rate is being received in HD-SDI and 3G-SDI modes. This input only is used to generate the value on the rx_t_rate output port, so if the rx_t_rate output port is not used, then it is not required that the rx_bit_rate input be driven correctly. When using the transceivers in Xilinx FPGAs, the device-specific transceiver control module contains a bit rate detector that generates the signal to be connected to the rx_bit_rate input port. HD-SDI mode: rx_bit_rate = 0: Bit rate = 1.485 Gb/s rx_bit_rate = 1: Bit rate = 1.485/1.001 Gb/s 3G-SDI mode: rx_bit_rate = 0: Bit rate = 2.97 Gb/s rx_bit_rate = 1: Bit rate = 2.97/1.001 Gb/s
rx_t_locked	Out	1	This output is High when the transport detection function in the receiver has identified the transport format of the SDI signal.
rx_t_family	Out	4	This output indicates which family of video signals is being used as the transport on the SDI interface. This output is only valid when rx_t_locked is High. This port does not necessarily identify the video format of the picture being transported. It only identifies the transport characteristics. See Table 3-1 for encoding of this port.
rx_t_rate	Out	4	This output indicates the frame rate of the transport. This is not necessarily the same as the frame rate of the actual picture. This output is only valid when rx_t_locked is High. See Table 3-2 for encoding of this port.
rx_t_scan	Out	1	This output indicates whether the transport is interlaced (Low) or progressive (High). This is not necessarily the same as the scan mode of the actual picture. This output is only valid when rx_t_locked is High.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
rx_level_b_3g	Out	1	In 3G-SDI mode, this output is asserted High when the input signal is level B and Low when it is level A. This output is only valid when rx_mode_3g is High.
rx_ce_sd	Out	1	This output is a clock enable for SD-SDI mode. When using a transceiver in a Xilinx FPGA which oversamples SD-SDI by a factor of 11X, rx_ce_sd will be asserted, on average, one cycle out of every 5.5 cycles of rx_usrclk in SD-SDI mode. The SD-SDI data stream on the rx_ds1a port and the rx video timing signals (rx_trs, rx_eav, and rx_sav) are only valid when rx_ce_sd is High in SD-SDI mode. In other SDI modes, rx_ce_sd is always High. When using a transceiver external to the FPGA, the duty cycle of rx_ce_sd will depend entirely on the duty cycle of the rx_sd_data_strobe signal. If, for example, rx_sd_data_strobe is always High, rx_ce_sd will also always be High.
rx_nsp	Out	1	When this output is High, it indicates that the framer has detected a TRS at a new word alignment. If rx_frame_en is High, this output is only asserted briefly. If rx_frame_en is Low, this output remains High until the framer is allowed to readjust to the new TRS alignment (by asserting rx_frame_en High during the occurrence of a TRS).
rx_line_a	Out	11	The current line number captured from the LN words of the Y data stream is output on this port. This output is valid in HD-SDI and 3G-SDI modes, but not in SD-SDI mode. In 3G-SDI level B mode, the output value is the line number from the Y data stream of link A or HD-SDI signal 1. For any case where the interface line number is not the same as the picture line number, such as for 1080p 60 Hz carried on 3G-SDI level B or dual link HD-SDI, the output value is the interface line number, not the picture line number.
rx_a_vpid	Out	32	All four user data bytes of the ST 352 packet from data stream 1 are output on this port in this format: MS byte to LS byte: byte4, byte3, byte2, byte1. This output port is valid only when rx_a_vpid_valid is High. This port is potentially valid in any SDI mode, if there are ST 352 packets embedded in the SDI signal. In 3G-SDI level A mode, the output data is the VPID data captured from data stream 1 (luma). In 3G-SDI level B mode, the output data is the VPID data captured from data stream 1 of link A (dual link streams,) or HD-SDI signal 1 (dual HD-SDI signals).
rx_a_vpid_valid	Out	1	This output is High when rx_a_vpid is valid.
rx_b_vpid	Out	32	All four user data bytes of the ST 352 packet from data stream 2 are output on this port in this format: MS byte to LS byte: byte4, byte3, byte2, byte1. This output is valid only in 3G-SDI mode and only when rx_b_vpid_valid is High. In 3G-SDI level A mode, the output data is the VPID data captured from data stream 2 (chroma). In 3G-SDI level B mode, the output data the VPID data captured from data stream 1 of link B (dual link streams,) or HD-SDI signal 2 (dual HD-SDI signals).

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
rx_b_vpid_valid	Out	1	This output is High when rx_b_vpid is valid.
rx_crc_err_a	Out	1	This output is asserted High when a CRC error is detected on the previous video line. For 3G-SDI level B mode, this output indicates CRC errors on data stream 1 only. There is a second output called rx_crc_err_b that indicates CRC errors on data stream 2 for 3G-SDI level B mode. This output is not valid in SD-SDI mode. This output is asserted High for one video line time when a CRC error has been detected on the previous video line. There is a six or seven video sample period latency, depending on the SDI mode, from the video sample in which the rx_eav signal is asserted until the rx_crc_err_a signal changes values.
rx_ds1a	Out	10	The recovered data stream 1 is output on this port. The contents of this data stream are dependent on the SDI mode: SD-SDI: Multiplexed Y/C data stream HD-SDI: Y data stream 3G-SDI level A: Data stream 1 3G-SDI level B-DL: Data stream 1 of link A 3G-SDI level B-DS: Y data stream of HD-SDI signal 1
rx_ds2a	Out	10	The recovered data stream 2 is output on this port. The contents of this data stream are dependent on the SDI mode: SD-SDI: Not used HD-SDI: C data stream 3G-SDI level A: Data stream 2 3G-SDI level B-DL: Data stream 2 of link A 3G-SDI level B-DS: C data stream of HD-SDI signal 1
rx_eav	Out	1	This output is asserted High for one sample time when the XYZ word of an EAV is present on the data stream output ports.
rx_sav	Out	1	This output is asserted High for one sample time when the XYZ word of an SAV is present on the data stream output ports.
rx_trs	Out	1	This output is asserted High for four consecutive sample times as all four words of an EAV or SAV, starting with the 3FF word and continuing through the XYZ word, are output on the data stream ports.
rx_line_b	Out	11	This output port is only valid in 3G-SDI level B mode, and outputs the line number for the Y data stream of link B or HD-SDI signal 2. For any case where the interface line number is not the same as the picture line number, the line number output on this port is the interface line number, not the picture line number.
rx_dout_rdy_3g	Out	1	In 3G-SDI level B mode, the output data rate is 74.25 MHz, but the rx_usrclk clock frequency is 148.5 MHz. The rx_dout_rdy_3g output is asserted at a 74.25 MHz rate in 3G-SDI level B mode. This output is always High in all other modes, allowing it to be used as a clock enable to downstream modules.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
rx_ds1b	Out	10	This output is only used in 3G-SDI level B mode. The data stream output on this port is: 3G-SDI level B-DL: Data stream 1 of link B 3G-SDI level B-DS: Y data stream of HD-SDI signal 2
rx_ds2b	Out	10	This output is only used in 3G-SDI level B mode. The data stream output on this port is: 3G-SDI level B-DL: Data stream 2 of link B 3G-SDI level B-DS: C data stream of HD-SDI signal 2
rx_crc_err_b	Out	1	This is the CRC error indicator valid only in 3G-SDI level B mode. It indicates that a CRC error was detected on link B for 3G-SDI B-DL signals and HD-SDI signal 2 for 3G-SDI level B-DS signals. This output has the same timing as the rx_crc_err_a signal.
rx_edh_errcnt_en	In	16	This input controls which EDH error conditions will increment the rx_edh_errcnt counter. See Table 3-3 for the encoding of this port.
rx_edh_clr_errcnt	In	1	When High, this input will clear the rx_ed_errcnt counter. This input port must be High during the same clock cycle when rx_ce_sd is also High in order to clear the error counter.
rx_edh_ap	Out	1	This output is asserted High when the active picture CRC calculated for the previous field does not match the AP CRC value in the EDH packet.
rx_edh_ff	Out	1	This output is asserted High when the full field CRC calculated for the previous field does not match the FF CRC value in the EDH packet.
rx_edh_anc	Out	1	This output is asserted High when an ancillary data packet checksum error is detected.
rx_edh_ap_flags	Out	5	The active picture error flag bits from the most recently received EDH packet are output on this port.
rx_edh_ff_flags	Out	5	The full field error flag bits from the most recently received EDH packet are output on this port.
rx_edh_anc_flags	Out	5	The ancillary error flag bits from the most recently received EDH packet are output on this port.
rx_edh_packet_flags	Out	4	This port outputs four error flags related to the most recently received EDH packet.
rx_edh_errcnt	Out	16	This is the SD-SDI EDH error counter. It increments once per field when any of the error conditions enabled by the rx_edh_err_en port occur during that field.
Transmit Ports			
tx_usrclk	In	1	This clock input clocks the SDI transmitter data path. It must have a frequency of 74.25 MHz or 74.25/1.001 MHz for HD-SDI and 148.5 MHz or 148.5/1.001 MHz for 3G-SDI. The combination of the tx_usrclk frequency and tx_ce must result in a 27 MHz data rate in SD-SDI mode. When used with transceivers in Xilinx FPGAs, the frequency of tx_usrclk is 148.5 MHz in SD-SDI mode.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
tx_ce	In	3	The combination of the tx_usrclk frequency and tx_ce must clock the SDI core's transmitter data path at the word rate of the current SDI mode: 148.5 or 148.5/1.001 MHz in 3G-SDI mode, 74.25 or 74.25/1.001 MHz in HD-SDI mode, and 27 MHz in SD-SDI mode. When using transceivers in Xilinx FPGAs, tx_ce must always be High in HD-SDI and 3G-SDI modes. In SD-SDI mode, tx_ce must be asserted at a 27 MHz rate with a mandatory 5/6/5/6 clock cycle cadence. Three clock enable inputs are provided. They each clock different portions of the transmitter. The values on all three bits of the port must always be the same. Three bits are provided for signal loading purposes. If difficulties arise in meeting timing on the clock enable signal when all three bits are driven from the same flip-flop, then duplicate flip-flops can be used to create separate, but identical, clock enables to drive the different bits of this port
tx_din_rdy	In	1	For SD-SDI, HD-SDI, and level A 3G-SDI modes, this input must be kept High at all times. For level B 3G-SDI mode, this input must be asserted every other clock cycle.
tx_rst	In	1	This is a synchronous reset input. It resets the transmit section when High. In order to fully reset the transmitter, both tx_ce and tx_din_rdy must be High when tx_rst is High.
tx_mode	In	2	This input port is used to select the transmitter SDI mode: 00 = HD-SDI (including dual link HD-SDI) 01 = SD-SDI 10 = 3G-SDI 11 = Invalid
tx_level_b_3g	In	1	In 3G-SDI mode, this input determines whether the module is configured for level A (level = Low) or for level B (level = High). In 3G-SDI mode, this input must be properly controlled in order to produce legal 3G-SDI data streams.
tx_insert_crc	In	1	When this input is High, the transmitter will generate and insert CRC values on each video line in HD-SDI and 3G-SDI modes. When this input is Low, CRC values are not generated and inserted. This input is ignored in SD-SDI mode.
tx_insert_ln	In	1	When this input is High, the transmitter will insert line numbers after the EAV in each video line. The line number must be supplied on the tx_line_a and tx_line_b input ports. This input is ignored in SD-SDI mode.
tx_insert_edh	In	1	When this input is High, the transmitter will generate and insert EDH packets in every field in SD-SDI mode. When this input is Low, EDH packets are not inserted. This input is ignored in HD-SDI and 3G-SDI modes.
tx_insert_vpid	In	1	When this input is High, ST 352 packets are inserted into the data streams, otherwise the packets are not inserted. ST 352 packets are mandatory in 3G-SDI and dual link HD-SDI modes and optional in HD-SDI and SD-SDI modes.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
tx_overwrite_vpid	In	1	If this input is High, ST 352 packets already present in the data streams are overwritten. If this input is Low, existing ST 352 packets are not overwritten. When transporting ST 372 dual link data streams on a 3G-SDI level B interface, existing ST 352 packets in the data streams must be updated to indicate that the interface is 3G-SDI rather than HD-SDI mode. This module updates these packets only when overwrite is High. So, unless the ST 352 packets are being updated externally to the SMPTE SD/HD/3G-SDI core, this input must be High when transmitting in 3G-SDI level B-DL mode.
tx_video_a_y_in	In	10	This is the data stream A Y input. The data on this port depends on the SDI mode: SD-SDI: Multiplexed Y/C data stream HD-SDI: Y component 3G-SDI level A: Data stream 1 Dual link HD-SDI or 3G-SDI level B-DL: Data stream 1 of link A 3G-SDI level B-DS: Y component of HD-SDI signal 1
tx_video_a_c_in	In	10	This is the data stream A C input. The data on this port depends on the SDI mode. SD-SDI: Unused HD-SDI: Interleaved CB and CR components 3G-SDI level A: Data stream 2 Dual link HD-SDI or 3G-SDI level B-DL: Data stream 2 of link A 3G-SDI level B-DS: Interleaved CB and CR components of HD-SDI signal 1
tx_video_ b_y_in	In	10	This is the data stream B Y input: The data stream on this port depends on the SDI mode: Dual link HD-SDI or 3G-SDI level B-DL: Data stream 1 of link B 3G-SDI level B-DS: Y component of HD-SDI signal 2 For other SDI modes, this input port is unused.
tx_video_b_c_in	In	10	This is the data stream B C input: The data stream on this port depends on the SDI mode. Dual link HD-SDI or 3G-SDI level B-DL: Data stream 2 of link B 3G-SDI level B-DS: Interleaved CB and CR components of HD-SDI signal 2 For other SDI modes, this input port is unused.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
tx_line_a	In	11	The current line number must be provided to the module through this port if either ST 352 packet insertion is enabled (tx_insert_vpid = High) or if HD-SDI and 3G-SDI line number insertion is enabled (tx_insert_ln = High). SD-SDI only uses 10-bit line numbers, so bit 10 of the port must be 0 in SD-SDI mode. The line number must be valid at least one clock cycle before the start of the HANC space (by the XYZ word of the EAV) and must remain valid during the entire HANC interval. This input is the only line number input used for SD-SDI, HD-SDI, and 3G-SDI level A modes. For 3G-SDI level B mode, a second line number input port, tx_line_b, is also provided. For video formats where the picture line number is different than the transport line number, the value supplied on this port must be the transport line number.
tx_line_b	In	11	This is the second line number input port and is used only for 3G-SDI level B mode. This additional line number port allows the two separate HD-SDI signals to be vertically unsynchronized in level B-DS mode. When using either 3G-SDI level B-DL or B-DS, this port must be given a valid line number input. This input port has the same timing and other requirements described for tx_line_a.
tx_vpid_byte1	In	8	This value is inserted as the first user data word of the ST 352 packet. It must be valid during the entire HANC interval.
tx_vpid_byte2	In	8	This value is inserted as the second user data word of the ST 352 packet. It must be valid during the entire HANC interval.
tx_vpid_byte3	In	8	This value is inserted as the third user data word of the ST 352 packet. It must be valid during the entire HANC interval.
tx_vpid_byte4a	In	8	This value is inserted as the fourth user data word of the ST 352 packet. This word is used for the ST 352 packets inserted into SD-SDI, HD-SDI, and 3G-SDI level A data streams. For 3G-SDI level B and dual link HD-SDI modes, this value is used for the ST 352 packet inserted into Y channel of link A only. This input must be valid during the entire HANC interval.
tx_vpid_byte4b	In	8	This value is inserted as the fourth user data word of ST 352 packets inserted in the Y channel of link B for 3G-SDI level B and dual link HD-SDI modes only. This input value is not used for SD-SDI, HD-SDI, or 3G-SDI level A modes. This input must be valid during the entire HANC interval.
tx_vpid_line_f1	In	11	The ST 352 packet is inserted in the HANC space of the line number specified by this input port. For interlaced video, this input port specifies a line number in field 1. For progressive video, this specifies the only line in the frame where the packet is inserted. The input value must be valid during the entire HANC interval. If tx_insert_vpid is low, this input is ignored.

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
tx_vpid_line_f2	In	11	For interlaced video, a ST 352 packet is inserted on the line number in field 2 indicated by this value. For progressive video, this input port must be disabled by holding the tx_vpid_line_f2_en port Low. The input value must be valid during the entire HANC interval. This input is ignored if either tx_insert_vpid or tx_vpid_line_f2_en are Low.
tx_vpid_line_f2_en	In	1	This input controls whether or not ST 352 packets are inserted on the line indicated by line_f2. For interlaced video, this input must be High. For progressive video, this input must be Low. For progressive video transported on an interlaced transport, such as 1080p 60 Hz transported by either 3G-SDI level B-DL or dual link HD-SDI, ST 352 packets must be inserted into both fields of the interlaced transport, so this input must be High. This input must be valid during the entire HANC interval. This input is ignored if tx_insert_vpid is Low.
tx_ds1a_out	Out	10	This is the link A data stream 1 output. The data stream output on this port contains ST 352 packets if tx_insert_vpid is High. If the application needs to insert ancillary data packets, they should be inserted into the data stream output on this port. The resulting data stream should then be supplied to the tx_ds1a_in port. The data on this port depends on the SDI mode: SD-SDI: Interleaved Y/C data stream HD-SDI: Y component 3G-SDI level A: Data stream 1 Dual link HD-SDI or 3G-SDI level B-DL: Data stream 1 of link A 3G-SDI level B-DS: Y component of HD-SDI signal 1
tx_ds2a_out	Out	10	This is the link A data stream 2 output. The data stream output on this port contains ST 352 packets if tx_insert_vpid is High. If the application needs to insert ancillary data packets, they should be inserted into the data stream output on this port. The resulting data stream should then be supplied to the tx_ds2a_in port. The data on this port depends on the SDI mode: HD-SDI: Interleaved C_B/C_R component Dual link HD-SDI or 3G-SDI level B-DL: Data stream 2 of link A 3G-SDI level B-DS: Interleaved C_B/C_R component data stream of HD-SDI signal 1
tx_ds1b_out	Out	10	This is the link B data stream 1 output. The data stream output on this port contains ST 352 packets if tx_insert_vpid is High. If the application needs to insert ancillary data packets, they should be inserted into the data stream output on this port. The resulting data stream should then be supplied to the tx_ds1b_in port. The data on this port depends on the SDI mode: Dual link HD-SDI or 3G-SDI level B-DL: Data stream 1 of link B 3G-SDI level B-DS: Y component of HD-SDI signal 2 For other SDI modes, this input port is unused

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
tx_ds2b_out	Out	10	This is the data stream B C input: The data stream on this port depends on the SDI mode: Dual link HD-SDI or 3G-SDI level B carrying dual link HD-SDI: the C data stream of link B enters the module on this port. Dual link HD-SDI or 3G-SDI level B carrying dual link HD-SDI: Data stream 2 of link B. 3G-SDI level B carrying dual HD-SDI signals: Interleaved C_B/C_R component of HD-SDI signal 2. For other SDI modes, this input port is unused
tx_use_dsin	In	1	This input controls the source of the data streams sent by the transmitter. When this input is High, the sources of the transmitted data streams are the tx_ds1a_in, tx_ds2a_in, tx_ds1b_in, and tx_ds2b_in input ports. When this input is Low, the source of the transmitted data streams are internal to the core, coming directly from the video payload ID insertion function. When the application needs to do ancillary data insertion, the tx_use_dsin port is set High to allow the application to modify the data streams and provide the modified data streams to the transmitter on the tx_dsxx_in ports. When no ancillary data insertion is required, the tx_use_dsin input is set Low and the tx_dsxx_in ports are ignored.
tx_ds1a_in	In	10	This is the link A data stream 1 input. This port is ignored if tx_use_dsin is Low. If tx_use_dsin is High, this port supplied a data stream to be transmitted. The data stream supplied on this port depends on the SDI mode: SD-SDI: Interleaved Y/C data stream HD-SDI: Y component 3G-SDI level A: Data stream 1 Dual link HD-SDI or 3G-SDI level B-DL: Data stream 1 of link A 3G-SDI level B-DS: Y component of HD-SDI signal 1
tx_ds2a_in	In	10	This is the link A data stream 2 input. This port is ignored if tx_use_dsin is Low. If tx_use_dsin is High, this port supplied a data stream to be transmitted. The data stream supplied on this port depends on the SDI mode: HD-SDI: Interleaved C_B/C_R component Dual link HD-SDI or 3G-SDI level B-DL: Data stream 2 of link A 3G-SDI level B-DS: Interleaved C_B/C_R component data stream of HD-SDI signal 1
tx_ds1b_in	In	10	This is the link B data stream 1 input. This port is ignored if tx_use_dsin is Low. If tx_use_dsin is High, this port supplied a data stream to be transmitted. The data stream supplied on this port depends on the SDI mode: Dual link HD-SDI or 3G-SDI level B-DL: Data stream 1 of link B 3G-SDI level B-DS: Y component of HD-SDI signal 2 For other SDI modes, this input port is unused

Table 2-3: **SMPTE SD/HD/3G-SDI Ports *(Cont'd)***

Port Name	I/O	Width	Description
tx_ds2b_in	In	10	This is the link B data stream 2 input. This port is ignored if tx_use_dsin is Low. If tx_use_dsin is High, this port supplied a data stream to be transmitted. The data stream supplied on this port depends on the SDI mode: Dual link HD-SDI or 3G-SDI level B carrying dual link HD-SDI: Data stream 2 of link B 3G-SDI level B carrying dual HD-SDI signals: Interleaved C_B/C_R component of HD-SDI signal 2 For other SDI modes, this input port is unused
tx_sd_bitrep_bypass	In	1	This input bypasses the 11X bit replicator used in SD-SDI mode when High. When used with transceivers in Xilinx FPGAs, this input must be Low to enable the bit replicator because the transceiver is running at 11X the 270 Mbps SD-SDI data rate so every bit must be sent 11 consecutive times. When using an external transceiver, the bit replicator can be bypassed by asserting this input High.
tx_txdata	In	20	This is the data stream output port of the SDI transmitter. When used with transceivers in Xilinx FPGAs, this port should be directly connected to the TXDATA port of the transceiver. If tx_sd_bitrep_bypass is High, the SD-SDI data stream is only 10-bit wide and is output on bits [19:10] of this port.
tx_ce_align_err	Out	1	This output indicates problems with the 5/6/5/6 clock cycle cadence on the tx_ce clock enable in SD-SDI mode. In SD-SDI mode, the tx_ce signal must follow a regular 5/6/5/6 clock cycle cadence. If it does not, the SD-SDI bit stream will be formed incorrectly. The tx_ce_align_err will go High if the cadence is incorrect. This port is only valid in SD-SDI mode and only if tx_sd_bitrep_bypass is Low.

Designing with the Core

This chapter includes guidelines and additional information to make designing with the core easier.

General Design Guidelines

SDI Receiver Operation

The SDI receiver has these features:

- The receiver automatically detects the SDI standard of the input signal (3G-SDI, HD-SDI, or SD-SDI) and reports the current SDI mode on an output port. This mode detection feature can be disabled if desired, in which case the receiver must be told which SDI mode to operate in.
- The receiver detects and reports the video transport format (e.g.,1080p 30 Hz, 1080i 50 Hz) for HD-SDI and 3G-SDI modes.
- The receiver supports 3G-SDI level A and level B formats, and automatically detects whether 3G-SDI data streams are level A or B. The 3G-SDI level is reported on an output port.
- The receiver performs CRC error checking for HD-SDI and 3G-SDI modes.
- Optional EDH error checking for SD-SDI format is available. The optional EDH processor also includes an SD-SDI flywheel, an SD-SDI locked detector, and a video format (NTSC or PAL) detector.
- Line numbers are captured and output from the SDI receiver. For the 3G-SDI level B format, line numbers are captured for each of the two HD-SDI streams carried on the 3G-SDI interface.
- SMPTE ST 352 payload ID packets are captured for all SDI modes. The captured ST 352 packet data is available on output ports for one or two data streams (for those formats that require ST 352 packets in both streams).
- All ancillary data embedded in the SDI data streams is preserved and output from the receiver on the video data stream outputs.

Figure 3-1 is a detailed block diagram of the RX section of the SMPTE SD/HD/3G-SDI core.

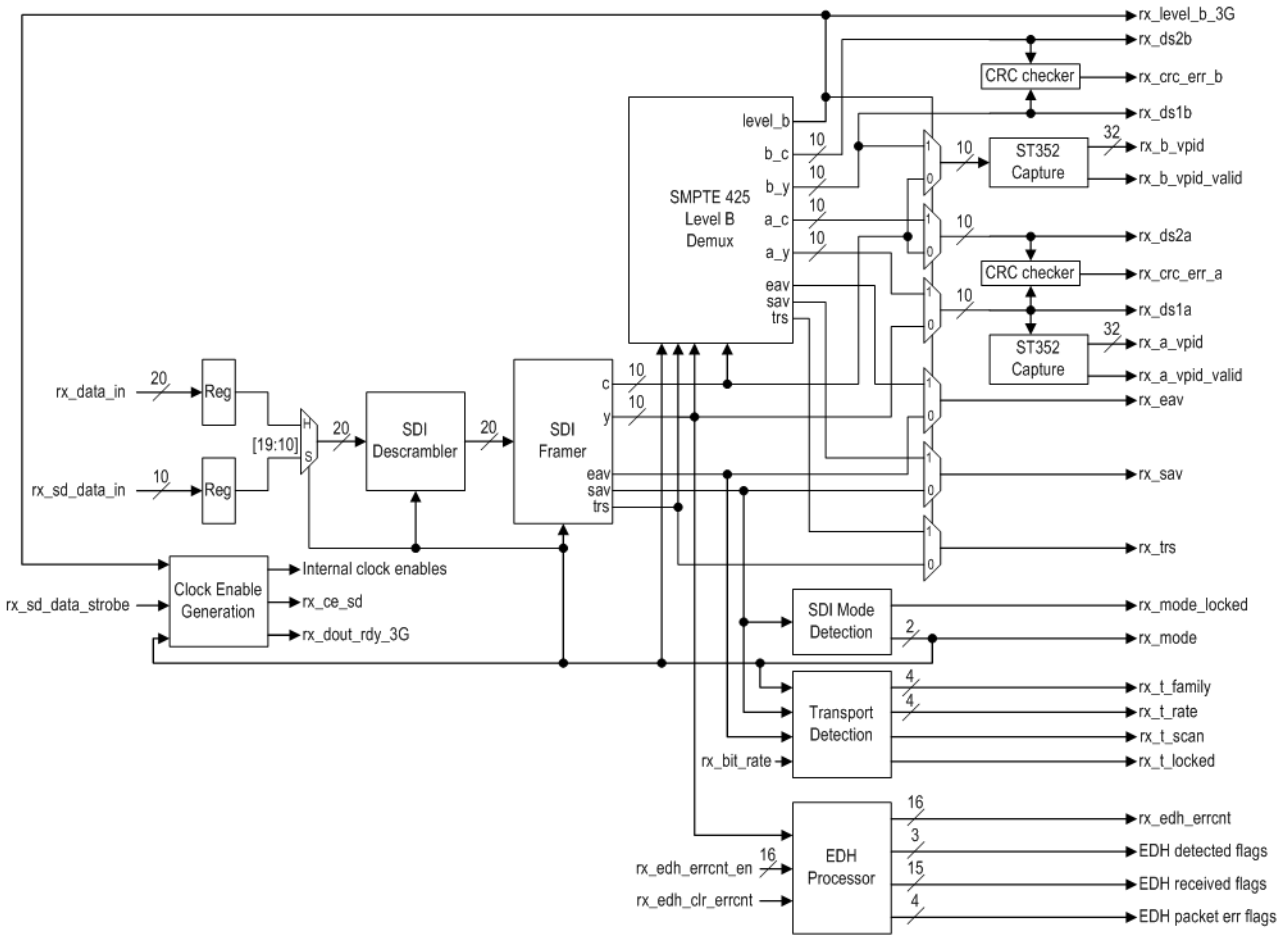

Figure 3-1: **SMPTE SD/HD/3G-SDI Core RX Section**

Transport Format Detection

The SDI receiver has an automatic transport format detector. This function examines the timing of the video signals in the SDI data streams and determines which video format they are. The operation of this function is independent of and not dependent on ST 352 payload ID packets. This function determines the transport format, not the picture format. Usually these are the same, but not always. For example, when 1080p 60 Hz video is transported on 3G-SDI level B-DL, the video transport is actually 1080i 60 Hz - the transport is interlaced, but the picture is progressive.

The `rx_t_family` output port provides a 4-bit code to indicate to which format family the transport timing output corresponds. The encoding of this output port is shown in Table 3-1. The transport detection unit also determines whether transport is interlaced or progressive and reports this on the `rx_t_scan` output port.

Table 3-1: **rx_t_family Encoding**

rx_t_family	Transport Video Format	Active Pixels
0000	SMPTE ST 274	1920 x 1080
0001	SMPTE ST 296	1280 x 720
0010	SMPTE 2048-2	2048 x 1080
0011	SMPTE 295	1920 x 1080
1000	NTSC	720 x 486
1001	PAL	720 x 576
1111	Unknown	
Others	Reserved	

The transport detector also determines the frame rate of the transport signal. This feature is dependent on the `rx_bit_rate` input in HD-SDI and 3G-SDI modes to distinguish between the N/1 and the N/1.001 frame rates. The `rx_t_rate` port indicates the frame rate of the transport signal, as shown in Table 3-2. The encoding of the frame rate matches the encoding used as the picture rate field of SMPTE ST 352 video payload ID packets. However, the `rx_t_rate` shows the transport frame rate, not the picture rate. Also, the `rx_t_rate` port value is always the frame rate, even for interlaced transports.

Table 3-2: **rx_t_rate Encoding**

rx_t_rate	Frame Rate
0000	None
0010	23.98 Hz
0011	24 Hz
0100	47.95 Hz
0101	25 Hz
0110	29.97 Hz
0111	30 Hz
1000	48 Hz
1001	50 Hz
1010	59.94 Hz
1011	60 Hz
Others	Reserved

It can take the transport format detector up to two video frames to identify the transport format after the receiver locks to the SDI signal.

Operation of the SDI Receiver in the Various SDI Modes

The SDI receiver automatically determines the standard of the incoming SDI mode (SD-SDI, HD-SDI, 3G-SDI level A, or 3G-SDI level B). It does this by sequentially trying to lock to each

SDI mode until it finds the correct SDI mode. When locked to the correct SDI mode, the receiver configures itself for correct operation in that mode. The recovered clock frequency and the number and data rate of the output data streams depend on the SDI mode.

This automatic SDI mode detection feature can be disabled by driving the `rx_mode_detect_en` input port Low. If this port is low, then the SDI receiver must be told which SDI mode to operate in using the `rx_forced_mode` port.

SD-SDI RX Operation

The 270 Mbps bit rate of SD-SDI is too slow for the transceivers in Xilinx FPGAs to receive directly. Therefore, when using a Xilinx transceiver to receive SD-SDI, the transceiver is locked to its reference clock and oversamples the SD-SDI bit stream by a factor of 11X. The frequency of the clock from the Xilinx transceiver is related directly to the frequency of its reference clock and is nominally 148.5 MHz. A data recovery unit (DRU) is implemented in the fabric of the FPGA to recover the SD-SDI data from the oversampled data output by the transceiver. The 10-bit data stream from the DRU must be connected to the `rx_sd_data_in` port of the SMPTE SD/HD/3G-SDI core. The DRU also provides a data ready signal that is asserted when it has recovered each 10-bit data word. This data ready signal from the DRU must be connected to the `rx_sd_data_strobe` input of the SMPTE SD/HD/3G-SDI core. Normally, this data strobe is asserted at a 5/6/5/6 clock cadence resulting in a 27 MHz data rate. However, because the clock from the transceiver is not necessarily locked to the recovered data rate, this cadence may vary occasionally.

The DRU required to receive SD-SDI when using transceivers in Xilinx FPGAs is not supplied with the core. It is supplied as part of the device-specific SDI interface control logic in a family of application notes that describe how to use the SMPTE SD/HD/3G-SDI core with the transceivers of each device family.

When using some other transceiver that can directly receive 270 Mbps SD-SDI, the SD-SDI data must still enter the SDI core in 10-bit words on the `rx_sd_data_in` port. And, the `rx_sd_data_strobe` signal must be High every clock cycle when data is valid. For example, if the transceiver recovers a 27 MHz clock in SD-SDI mode, this 27 MHz clock would be applied to the `rx_usrclk` input and `rx_sd_data_strobe` would need to be asserted High all of the time.

Figure 3-2 shows the timing of the SD video and timing signals output by the SMPTE SD/HD/3G-SDI core. This figure illustrates the use of a Xilinx transceiver, so the `rx_usrclk` frequency from is 148.5 MHz and the `rx_sd_data_strobe` signal from the DRU is asserted in a 5/6/5/6 clock cycle cadence most of the time. The outputs only change on the rising edge of `rx_usrclk`, when `rx_ce_sd` is High. The timing of the EAV sequence is shown. The `rx_sav` output signal has the same timing as the `rx_eav` signal, except that it is asserted during SAV sequences. If the cadence of the `rx_sd_data_strobe` varies from 5/6/5/6, so will the cadence of the `rx_ce_sd` output.

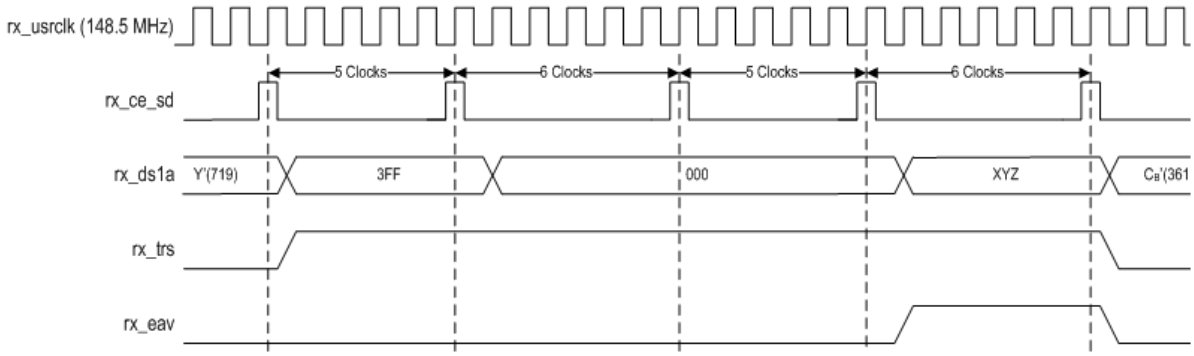

Figure 3-2: **SD-SDI RX Timing Diagram**

HD-SDI RX Operation

When the SDI receiver is operating in HD-SDI mode, the frequency of `rx_usrclk` must be 74.25 MHz or 74.25/1.001 MHz, depending on the HD-SDI bit rate. The Y and C data streams of the HD-SDI signal are output on the **rx_ds1a** and **rx_ds2a** ports, respectively, along with the timing signals `rx_trs`, `rx_eav`, and `rx_sav`. The line number is output on the `rx_line_a` port. In HD-SDI mode, the line number changes during the CRC0 word. Figure 3-3 shows the timing of the HD-SDI outputs.

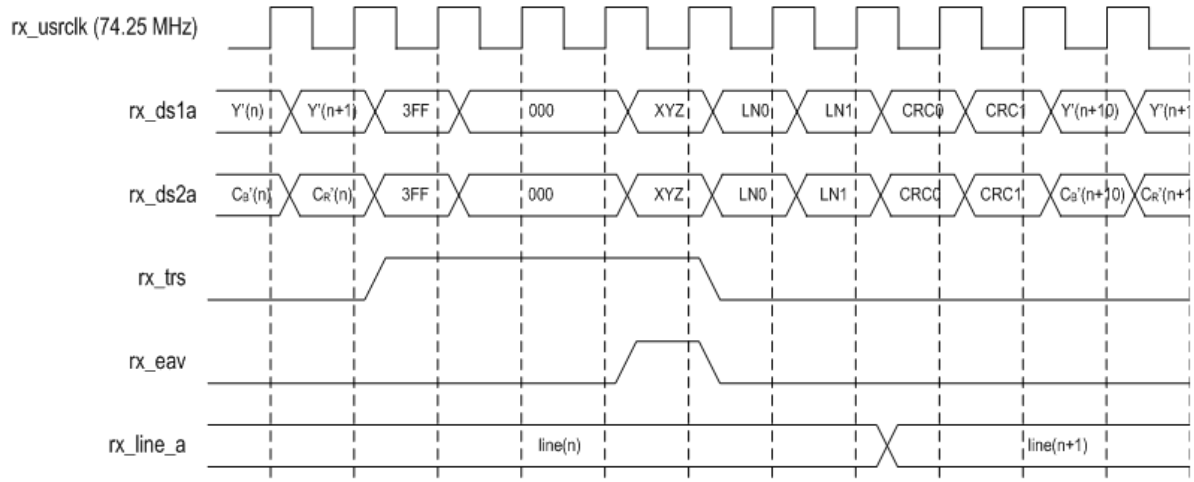

Figure 3-3: **HD-SDI RX Timing Diagram**

3G-SDI Level A RX Operation

When the SDI receiver is operating in 3G-SDI level A mode, the frequency of `rx_usrclk` must be 148.5 MHz or 148.5/1.001 MHz, depending on the 3G-SDI bit rate.

Figure 3-4 shows the output timing of the SDI receiver when receiving a 1080p 50, 59.94, or 60 Hz signal in 3G-SDI level A mode. These video formats do not require any further unpacking of the data streams, because rx_ds1a carries the luma component and rx_ds2a carries the multiplexed chroma components.

Other video formats, such as 4:4:4 10-bit or 12-bit, have identical timing to that shown in Figure 3-4, but the video samples are packed as specified by the SMPTE ST 425-1 so that it takes two consecutive words on each data stream to carry a single video sample. The SMPTE SD/HD/3G-SDI core does not unpack these other video formats, but outputs the two data streams exactly as described in the 3G-SDI level A data stream mapping sections of SMPTE ST 425-1.

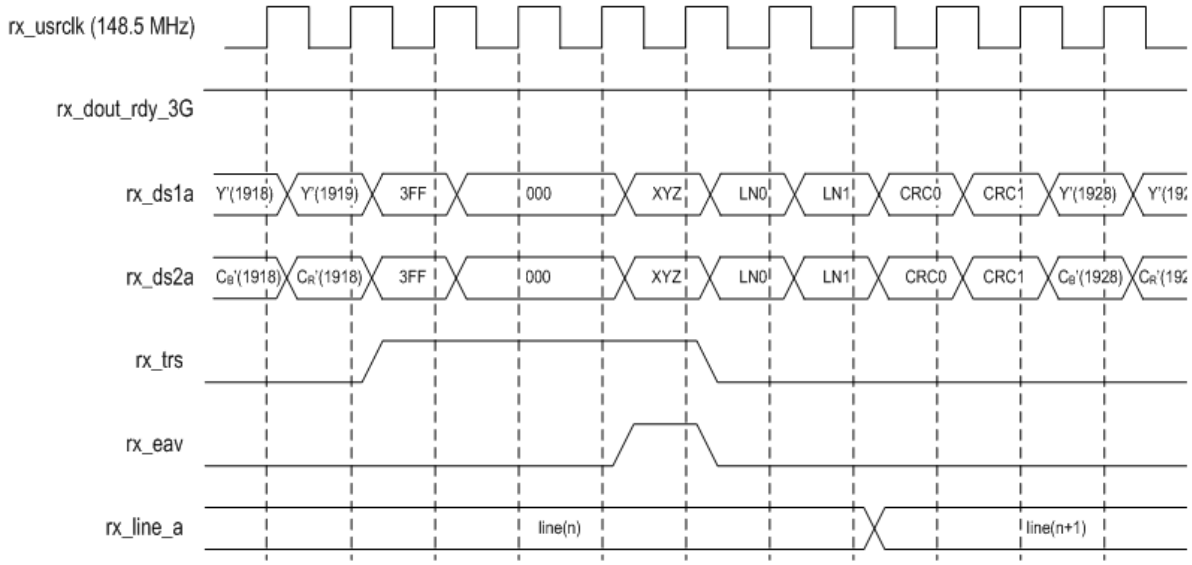

Figure 3-4: **3G-SDI Level A RX Timing (1080p 50 Hz or 60 Hz)**

3G-SDI Level B RX Operation

When the SDI receiver is operating in 3G-SDI level B mode, the frequency of `rx_usrclk` must be 148.5 MHz or 148.5/1.001 MHz, depending on the 3G-SDI bit rate. However, in this mode, there are four 10-bit data streams output by the SDI receiver. The data rate of these data streams is half the frequency of `rx_usrclk`, therefore, the `rx_dout_rdy_3g` signal is asserted every other clock cycle, and acts as a clock enable.

Both line number output ports are active. When the level B signal is transporting SMPTE ST 372 dual link data streams (level B-DL), the values on both `rx_line_a` and `rx_line_b` are identical and indicate the interface line number, not the picture line number. When the level B signal is transporting two independent HD-SDI signals, the two line number values are not necessarily the same, depending on whether the two HD-SDI signals are frame-locked or not. The `rx_line_a` and `rx_line_b` ports, not shown on the diagram, change at the same relative position as they do for 3G-SDI level A and HD-SDI, as the CRC0 word is output on the data streams.

When the 3G-SDI level B signal carries SMPTE ST 372 dual link data streams, the link A data streams are output on `rx_ds1a` and `rx_ds2a` and the link B data streams are output on `rx_ds1b` and `rx_ds2b`. These four links carry video mapped as required by SMPTE ST 372.

The SDI receiver does not unpack the data streams into video, but outputs them as SMPTE ST 372 data streams.

When the 3G-SDI level B signal carries two independent HD-SDI streams (level B-DS), the first HD-SDI stream is output with the luma component on `rx_ds1a` and the multiplexed chroma components on `rxds2a`. The second HD-SDI stream is output with the luma component on `rx_ds1b` and the multiplexed chroma component on `rx_ds2b`. These two HD-SDI streams are horizontally synchronized such that their EAVs and SAVs always line up exactly, therefore there is only a single set of `rx_eav`, `rx_sav`, and `rx_trs` timing signals.

Figure 3-5 shows the output timing of the SDI receiver when receiving a 3G-SDI level B signal.

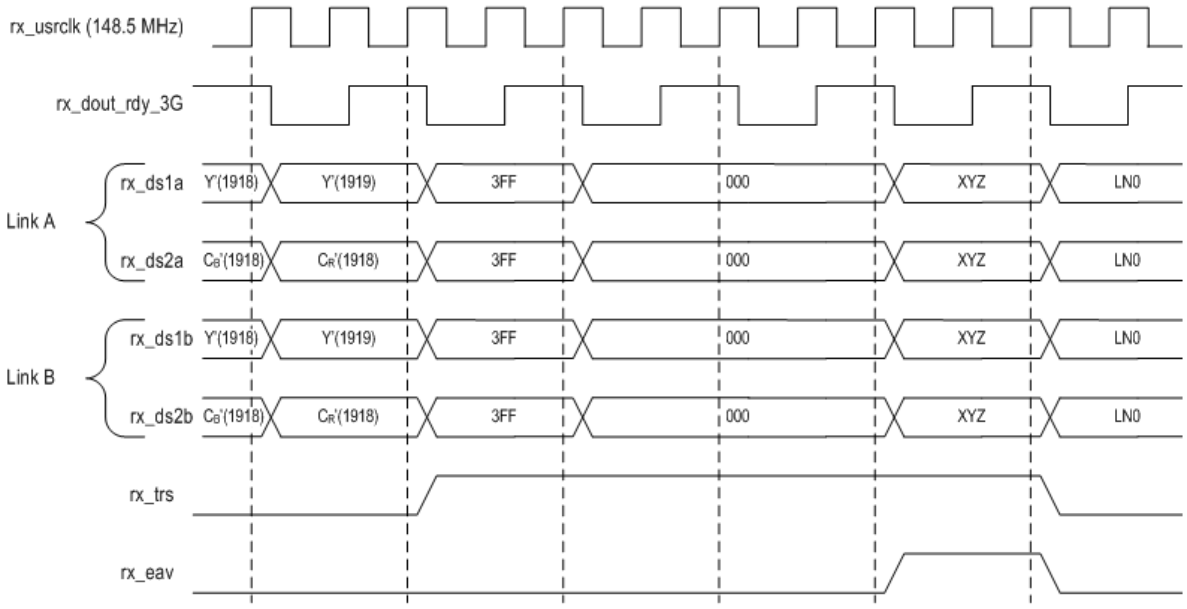

Figure 3-5: **3G-SDI Level B RX Timing**

Other SDI RX Design Considerations

Dual Link HD-SDI

To implement a dual link HD-SDI receiver, two SDI receivers are paired together with one receiving link A, and the other receiving link B. Typically, the received data streams for the two links are skewed, so the application must remove the skew. The data streams can then be unpacked into video streams, if desired.

Deskewing the data streams involves watching the EAV or SAV signals from each link, and delaying the data streams of the link whose EAV becomes asserted first by an appropriate amount to match the timing of the other link. The SRLC32E elements make perfect delay devices for implementing this deskew function. Prior to 2010, the SMPTE ST 372 specification stated that the maximum skew between the two links at the output of the transmitters must not exceed 40 ns. However, it is common in the industry for dual link

HD-SDI transmitters to have much more skew between the two links than this. The ST 372 specification now states that the skew between the links may be as high as 500 ns.

Processing Embedded Audio and Other Ancillary Data

The output data streams from the SDI receiver always have all ancillary data, including embedded audio packets, intact. Modules designed to process ancillary data can be connected to the data streams, clock enables, and other timing signals output by the SDI receiver.

SMPTE ST 352 Video Payload ID Packets

The receiver in the SMPTE SD/HD/3G-SDI core captures SMPTE ST 352 packets present in the data streams for all SDI modes. For SD-SDI and HD-SDI modes, the four data bytes of the ST 352 packet are output on the `rx_a_vpid` port. The `rx_a_vpid_valid` port indicates when valid ST 352 packets have been captured. This output has some hysteresis so that ST 352 packets can be missing from a few fields or frames before the valid signal is negated. During the time that the valid output is asserted and new ST 352 packets are not found, the data from the last valid ST 352 packet received is output on the `rx_a_vpid` port.

The 3G-SDI standard requires ST 352 packets in both data streams. The SDI receiver captures the ST 352 packets from both streams, outputting the data from the packet in data stream 1 on `rx_a_vpid`, and the data from the packet in data stream 2 on `rx_b_vpid`. The module also supplies individual `rx_a_vpid_valid` and `rx_b_vpid_valid` outputs.

SD-SDI EDH Error Detection

The receiver in the SMPTE SD/HD/3G-SDI core optionally contains an EDH processor that checks the SD-SDI signal for errors. This EDH processor does not update EDH packets in the SD-SDI stream. It simply reports any errors found and also captures the error flags from each EDH packet. The receiver EDH processor can be set to either include in the SMPTE SD/HD/3G-SDI core or not using the Vivado IDE.

The EDH processor has a 16-bit counter which counts the number of fields that have errors. The current error count is output on the `rx_edh_errcnt` port. The counter can be cleared by asserting `rx_edh_clr_errcnt` High. You can specify which types of errors are counted using the `rx_edh_errcnt_en` input port. This port has 16 unary bits which enable and disable 16 different error types. Any bit that is High enables the corresponding error. When this type of error is detected, the error counter increments. Any bit that is Low disables the corresponding error. Table 3-3 shows the encoding of the bits on the `rx_edh_errcnt_en` port.

Table 3-3: **Encoding of rx_edh_errcnt_en**

Bit #	Error
0	ANC EDH error
1	ANC EDA error

Table 3-3: **Encoding of rx_edh_errcnt_en *(Cont'd)***

Bit #	Error
2	ANC IDH error
3	ANC IDA error
4	ANC UES error
5	FF EDH error
6	FF EDA error
7	FF IDH error
8	FF IDA error
9	FF UES error
10	AP EDH error
11	AP EDA error
12	AP IDH error
13	AP IDA error
14	AP UES error
15	EDH packet checksum error

The ANC error conditions occur when there are errors in the ancillary data packets. The FF error conditions occur when there are errors in the full field. And, the AP error conditions occur when there are errors in the active portion of the picture. The EDH packet checksum error indicate a checksum error found within the EDH packet itself.

The ANC, FF, and AP error condition sets each have five individual error flags, described below. All flags are asserted High to indicate an error condition. For a complete description of the EDH, EDA, IDH, IDA, and UES error flags in the EDH packet, refer to the SMPTE RP 165 document available from SMPTE [Ref 1].

- EDH error: This error condition occurs when the EDH processor detects a CRC error (checksum error for ANC packets) in a field.
- EDA error: This error condition occurs when the EDA or EDH flags of the received EDH packet are asserted.
- IDH error: This error conditions is currently not supported.
- IDA error: This error condition occurs when the IDA or IDH flags of the received EDH packet are asserted.
- UES error: This error condition occurs when the UES flag in the received EDH packet is asserted.

The actively computed EDH errors for the ANC, AP, and FF are also output on the `rx_edh_anc`, `rx_edh_ap`, and `rx_edh_ff` ports, respectively. Thus, the `rx_edh_anc` port is asserted whenever a checksum error is detected in an ancillary data packet. The `rx_edh_ap` port is asserted when the calculated active picture CRC does not match the AP

CRC in the EDH packet. And, the rx_edh_ff port is asserted when the calculated full field CRC does not match the FF CRC in the EDH packet.

The EDH processor also outputs the ANC, AP, and FF flags from the EDH packet on the rx_edh_anc_flags, rx_edh_ap_flags, and rx_edh_ff_flags ports, respectively. These output ports are exact copies of the flags found in the last received EDH packet. This means they differ from the actively computed error conditions shown above. For example, the EDH flag (bit 0) of the rx_edh_ap_flags port indicates that the AP EDH flag is set in the last received EDH packet. But, the rx_edh_ap port indicates that the active picture CRC calculated locally by the EDH processor does not match the AP CRC value in the EDH packet. The rx_edh_anc_flags, rx_edh_ap_flags, and rx_edh_ff_flags ports are each 5 bits wide and are encoded as shown in Table 3-4.

Table 3-4: **Encoding of rx_edh_anc_flags, rx_edh_ap_flags, and rx_edh_ff_flags Ports**

Bit #	Flag
0	EDH
1	EDA
2	IDH
3	IDA
4	UES

The EDH processor also produces four error flags related to the format and contents of the EDH packet, itself. These error flags are output on the rx_edh_packet_flags port. The encoding of this port is shown in Table 3-5.

Table 3-5: **Encoding of rx_edh_packet_flags Port**

Bit #	Error
0	EDH packet is missing
1	Parity error in user data words of EDH packet
2	Checksum error in EDH packet
3	Format error in EDH packet – such as invalid data count

SDI Transmitter Operation

The transmitter in the SMPTE SD/HD/3G-SDI core has these features:

- Directly supports 3G-SDI level A transmission of 1080p 50 Hz, 59.94 Hz, and 60 Hz video.
- Transmits pre-formatted dual link HD-SDI streams via either dual link HD-SDI or 3G-SDI level B-DL formats.
- With the addition of a 3G-SDI level A mapping module (not supplied), supports all 3G-SDI level A compatible video formats.

- Directly supports transmission of two independent HD-SDI streams in the 3G-SDI level B-DS mode.
- Generates and updates EDH packets for the SD-SDI mode.
- Generates and inserts CRC values for HD-SDI and 3G-SDI modes.
- Inserts line number words for HD-SDI and 3G-SDI modes.
- Can generate and insert ST 352 payload ID packets in all SDI modes.

The SDI transmitter performs two main functions. The first is insertion of ST 352 video payload ID packets. The second function encompasses all of the formatting that needs to be done to generate a data stream to send to the `TXDATA` port of a GTX transmitter.

Figure 3-6 is a detailed block diagram of the TX section of the SMPTE SD/HD/3G-SDI core.

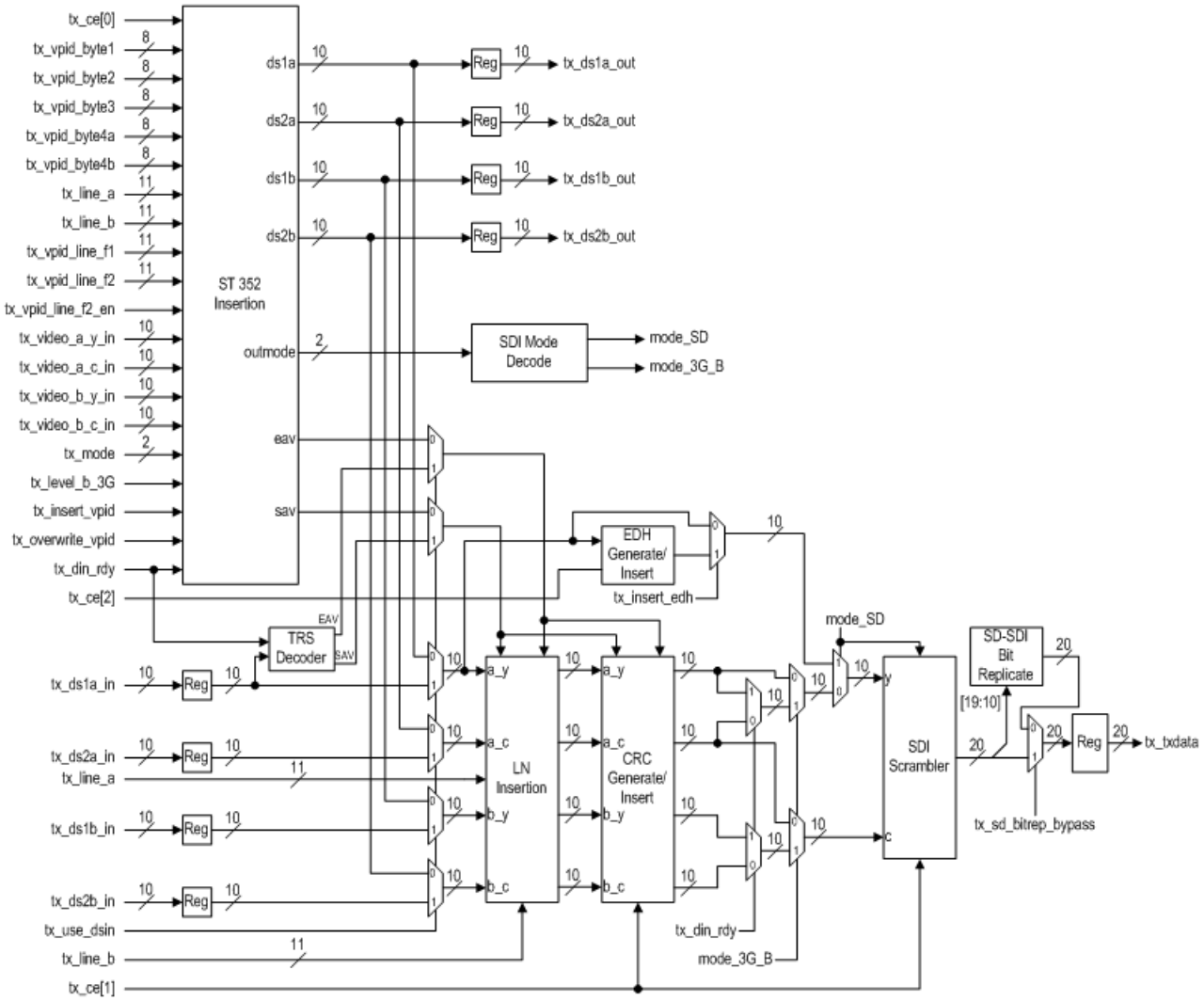

Figure 3-6: **SMPTE SD/HD/3G-SDI Core TX Section**

Operation of the SDI Transmitter in the Various SDI Modes

The SDI mode (SD-SDI, HD-SDI, 3G-SDI level A or 3G-SDI level B) of the SDI transmitter is determined by the `tx_mode` and `tx_level_b_3g` inputs. The clock frequency requirements and the number of data streams expected by the SDI transmitter data path depend on the SDI mode.

SD-SDI Transmitter Operation

When operating in SD-SDI mode with a transceiver in a Xilinx device, the `tx_usrclk` has a frequency of 148.5 MHz because the transceiver runs at 11 times the 270 Mb/s SD-SDI bit rate. The interleaved Y/C data stream is connected to the `tx_video_a_y_in` port of the SMPTE SD/HD/3G-SDI core. The `tx_ce` clock enable input of SMPTE SD/HD/3G-SDI core must be asserted at a 27 MHz rate, as shown in Figure 3-7. This means that `tx_ce` must be asserted with a 5/6/5/6 clock cycle cadence. Any other cadence of the `tx_ce` signal causes the SD-SDI bit replication logic to underflow or overflow. The `tx_din_rdy` port must always be held High in SD-SDI mode.

Note that the `tx_ce` port of the SMPTE SD/HD/3G-SDI core is three bits wide. All three bits must be driven with duplicate copies of the clock enable signal. Three separate bits are provided for loading purposes. They can all be tied together an driven by one signal, but if the loading is so high that it is difficult to meet timing, then separate duplicate copies of the clock enable should be generated and connected to each bit of the `tx_ce` port.

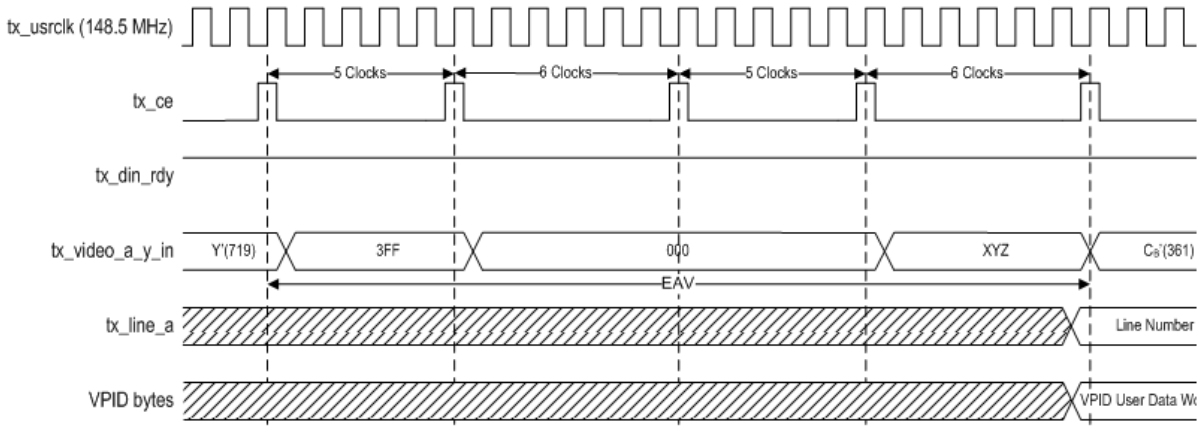

Figure 3-7: **SD-SDI TX Timing**

1. All inputs except tx_ce have an entire sample time in which to become stable. Data is only sampled on the inputs on the rising edge of tx_usrclk when tx_ce is High. The sample time is the time between rising edges of tx_usrclk when tx_ce is High. As shown in Figure 3-7, the tx_ce signal must always have a 5/6/5/6 clock cycle cadence. Any other cadence underflows or overflows the SDI bit replication logic. Although Figure 3-7 shows that the first word of the EAV is a 5-clock cycle sample, there is no such relationship required. The first word of the EAV could instead be a 6-clock cycle sample.
2. In SD-SDI mode, the line number value on the tx_line_a input port is only used to insert ST 352 packets. If ST 352 packet insertion is disabled (tx_insert_vpid is Low), then line numbers are not required on the tx_line_a port in SD-SDI mode. When used, the line number on tx_line_a must be stable starting with the XYZ word of the EAV, and must remain valid through the entire HANC interval. The VPID data bytes also have the same timing requirements as tx_line_a.

When using a transceiver other than a Xilinx transceiver, the tx_usrclk and the tx_ce signals may be used differently. For example, it may be possible to use a 27 MHz tx_usrclk in which case tx_ce must always be driven High. The tx_sd_bitrep_bypass input must be driven High is such a case to bypass the 11X bit replicator that produces an 11X oversampled output stream for Xilinx transceivers. When the bit replicator is bypassed, the SD-SDI data stream output by the SMPTE SD/HD/3G-SDI core is a 10-bit stream on bits [19:10] of the tx_txdata port.

If the bit replicator is not bypassed (tx_sd_bitrep_bypass High), then the data is output from the SDI core on all 20-bits of the tx_txdata port and is suitable for direct connection to the TXDATA port of Xilinx transceivers.

HD-SDI Transmitter Operation

When operating in HD-SDI mode, the frequency of tx_usrclk must be 74.25 MHz or 74.25/1.001 MHz. The tx_ce and tx_din_rdy input ports must always be High. Figure 3-8 shows the timing of the input signals for HD-SDI mode.

HD video enters the SMPTE SD/HD/3G-SDI core as two 10-bit data streams with the Y data stream on the tx_video_a_y_in port and the C data stream on the tx_video_a_c_in port. The input data rate is 74.25 MHz or 74.25/1.001 MHz. If the tx_insert_vpid input is High, ST 352 packets are generated and inserted.

The SMPTE SD/HD/3G-SDI core inserts line numbers into both data streams immediately after the EAV, if tx_insert_ln is High. It calculates and inserts CRC values immediately after the line numbers if tx_insert_crc is High. It scrambles the data streams and outputs one 20-bit data stream running at 74.25 MHz or 74.25/1.001 MHz on the tx_txdata output port.

Line numbers must be supplied on the tx_line_a port if either ST 352 packet insertion or line number insertion are enabled.

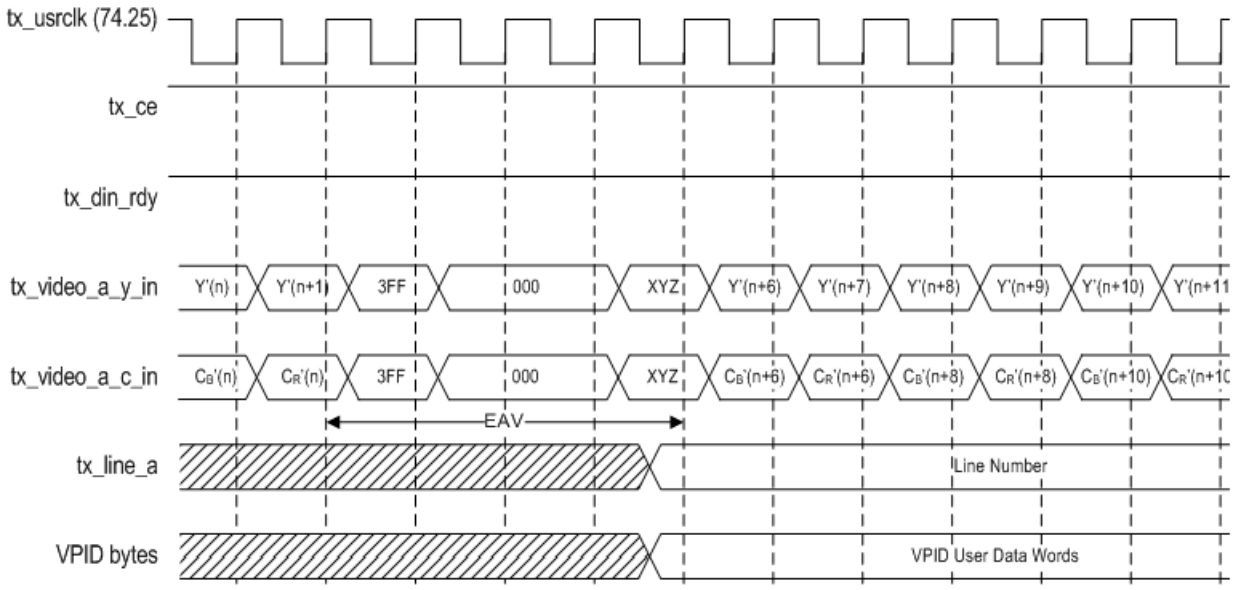

Figure 3-8: **HD-SDI TX Timing**

1. In HD-SDI mode, the line number value on the tx_line_a input port must be stable starting with the XYZ word of the EAV, and must remain valid through the entire HANC interval.
2. The VPID input bytes must be stable beginning with the XYZ word of the EAV, and must remain stable during the entire HANC interval on lines where SMPTE ST 352 packets are inserted.

3G-SDI Transmitter Operation

When operating in 3G-SDI mode, the transmitter can operate in level A mode or level B mode, as selected by the `tx_level_b_3g` input (level A = Low, level B = High).

Level A Mode

In 3G-SDI level A mode, the SMPTE SD/HD/3G-SDI core requires two 10-bit data streams on the `tx_a_y_in` (data stream 1) and `tx_a_c_in` (data stream 2) input ports. The frequency of `tx_usrclk` must be 148.5 MHz or 148.5/1.001 MHz. The tx_ce and `tx_din_rdy` inputs must always be High. For 1080p 50 Hz, 59.94 Hz, and 60 Hz, the Y component data stream is input on the `tx_video_a_y_in` port, and the C component data stream is input on the `tx_video_a_y_in` port. For all other 3G-SDI video formats, the video must be mapped to the two SDI data streams as described in SMPTE ST 425-1 [Ref 7] before they go into the SMPTE SD/HD/3G-SDI core.

Figure 3-9 shows the timing of the inputs signals for 3G-SDI level A mode.

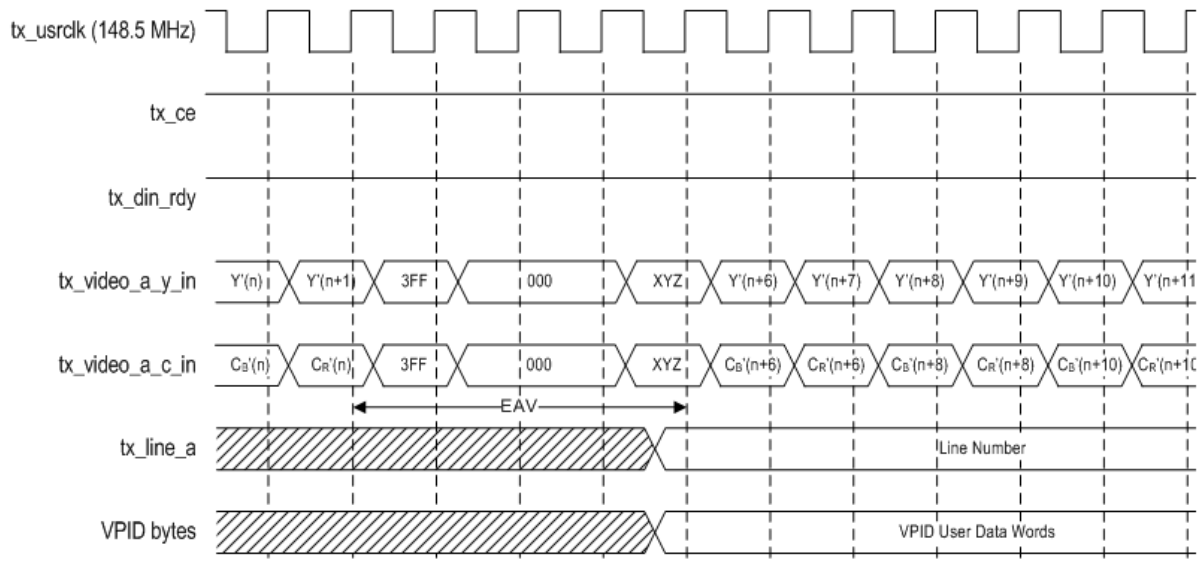

Figure 3-9: **3G-SDI Level A TX Timing**

1. In 3G-SDI level A mode, the line number value on the tx_line_a input port must be stable starting with the XYZ word of the EAV, and must remain valid through the entire HANC interval.
2. The VPID input bytes must be stable beginning with the XYZ word of the EAV, and must remain stable during the entire HANC interval on lines where SMPTE ST 352 packets are inserted.

The SMPTE SD/HD/3G-SDI core inserts SMPTE ST 352 packets into both data streams, before outputting the data streams on the `tx_ds1a_out` and tx_ds2a_out output ports or, if `tx_user_dsin_is` Low, routing these data streams to the rest of the transmitter. The SDI transmitter inserts the line number on the `tx_line_a` port into both data streams immediately after the EAV, if `tx_insert_ln` is High. It calculates and inserts CRC values immediately after the line numbers, if `tx_insert_crc` is High. It scrambles the data streams and outputs one 20-bit data stream running at 148.5 MHz on the `tx_txdata` output port.

Line numbers are required on the `tx_line_a` port if either ST 352 packet insertion or line number insertion are enabled.

Level B Mode

Operation of the SDI transmitter is the same for both 3G-SDI level B-DL and level B-DS. When running in 3G-SDI level B mode, the SMPTE SD/HD/3G-SDI core requires four 10-bit data streams on its `tx_video_a_y_in` (Y channel of link A), `tx_video_a_c_in` (C channel of link A), `tx_video_b_y_in` (Y channel of link B), and `tx_video_b_c_in` (C channel of link B) ports. These four data streams must be ST 372 dual link HD-SDI data streams for level B-DL, or two independent HD-SDI streams that are to be combined onto a single 3G-SDI signal for level B-DS. The frequency of `tx_usrclk` must be 148.5 MHz or 148.5/1.001 MHz, therefore the transmitter must be clocked every other clock cycle in 3G-SDI level B mode, as shown in Figure 3-10. The `tx_ce` signal cannot be used to cause the SDI transmitter to clock every other clock cycle in 3G-SDI mode. For 3G-SDI mode, `tx_din_rdy` must be used. Thus, in 3G-SDI B mode, the correct way to control the data

rate of the SDI transmitter is to keep tx_ce High and toggle the tx_din_rdy signal every other clock cycle as shown in Figure 3-10.

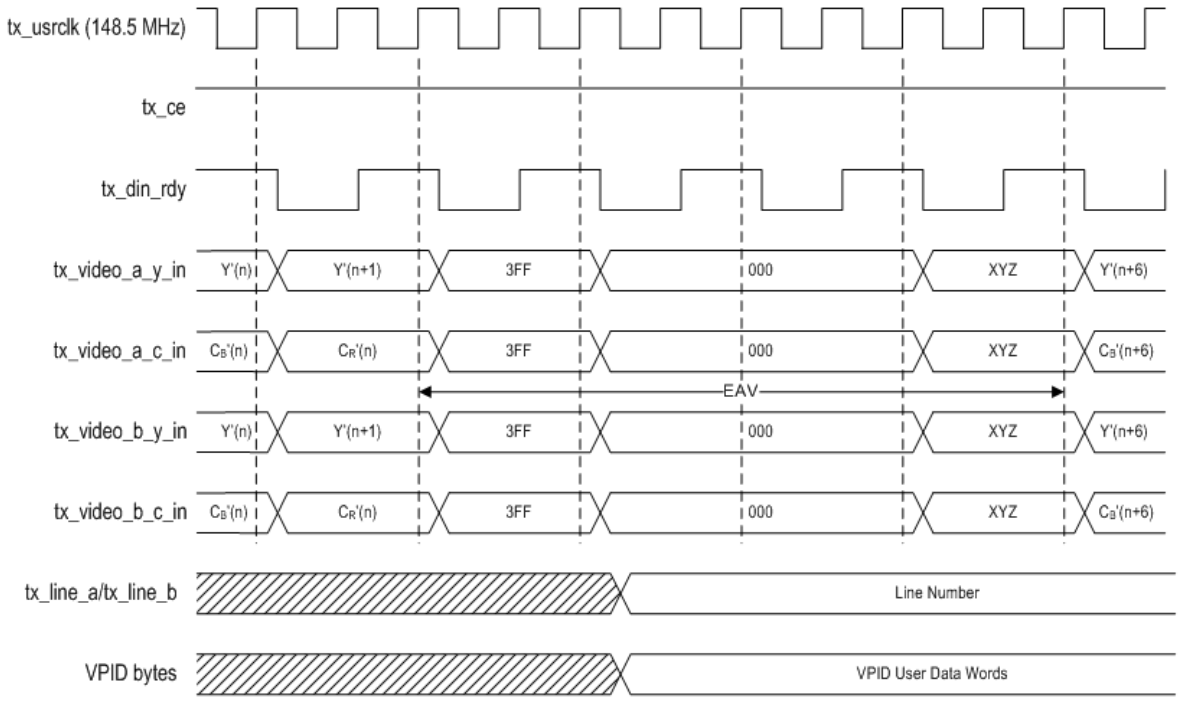

Figure 3-10: **3G-SDI Level B TX Timing**

1. In 3G-SDI mode, the line number values on the tx_line_a and tx_line_b input ports must be stable starting with the XYZ word of the EAV, and must remain valid through the entire HANC interval.
2. The VPID input bytes must be stable beginning with the XYZ word of the EAV, and must remain stable during the entire HANC interval on lines where ST 352 packets are inserted.

The SDI transmitter inserts ST 352 packets in the Y data streams of both link A and link B. The four data streams are output on the tx_ds1a_out, tx_ds2a_out, tx_ds1b_out, and tx_ds2b_out ports or routed directly to the rest of the transmitter if tx_use_din is Low.

If tx_insert_ln is High, the transmitter inserts line numbers into all four data streams. If tx_insert_crc is High, it calculates and inserts CRC values immediately after the line numbers in all four data streams. The data streams are then interleaved to produce a single 20-bit data stream running at 148.5 MHz or 148.5/1.001 MHz on the tx_txdata output port.

If ST 352 packets are to be inserted, line numbers are required on both the tx_line_a (for link A) and tx_line_b (for link B) input ports. ST 352 packets are mandatory for 3G-SDI. If line number insertion is enabled, line numbers are also required on the tx_line_a and tx_line_b ports. Two different line number ports are provided to support 3G-SDI level B-DS where the two independent HD-SDI signals being carried on the 3G-SDI interface may not be vertically synchronized. For 3G-SDI level B-DL mode tx_line_a and tx_line_b must be driven with identical line numbers. For video formats where the picture line number

and the transport line number are not the same, the line numbers must always be transport line numbers.

Dual Link HD-SDI Transmitter Operation

The SMPTE SD/HD/3G-SDI core does not contain the formatting logic to map the various video formats into ST 372 dual link HD-SDI streams. However, formatted ST 372 dual link HD-SDI streams can be transmitted by a pair of SDI transmitters. One transmitter implements the A link while the second implements the B line. Both transmitters operate in HD-SDI mode. The first transmitter takes in the Y and C data streams of link A on its `tx_video_a_y_in` and `tx_video_a_c_in` ports, respectively. The second transmitter takes in the Y and C data streams of link B on its `tx_video_a_y_in` and `tx_video_a_c_in` ports (not its `tx_video_b_y_in` and `tx_video_b_c_in` ports).

Summary of SDI TX Modes

The input data rates and connections for all SDI modes are summarized in Table 3-6.

Table 3-6: **SDI TX Modes**

SDI Mode	Level B	tx_usrclk frequency	tx_ce	tx_din_rdy	Input Data Rate	tx_video_a_y_in	tx_video_a_c_in	tx_video_b_y_in	tx_video_b_c_in
HD-SDI and Dual Link HD-SDI	N/A	74.25 MHz or 74.25/1.001 MHz	High	High	74.25 MHz or 74.25/1.001 MHz	Y	C		
SD-SDI	N/A	148.5 MHz	5/6/5/6 Cadence	High	27 MHz	Y/C			
3G-SDI A	No	148.5 MHz or 148.5/1.001 MHz	High	High	148.5 MHz or 148.5/1.001 MHz	Data Stream 1	Data Stream 2		
3G-SDI B	Yes	148.5 MHz or 148.5/1.001 MHz	High	Asserted every other clock cycle	74.25 MHz or 74.25/1.001 MHz	Link A Y	Link A C	Link B Y	Link B C

SDI TX

This section provides some additional details about the operation of the SMPTE SD/HD/3G-SDI core transmitter.

ST 352 Packet Insertion

The SMPTE SD/HD/3G-SDI core can insert ST 352 payload ID packets into SD-SDI, HD-SDI, dual link HD-SDI, and 3G-SDI (both level A and level B) streams. The dual link HD-SDI and 3G-SDI standards require ST 352 packets in the data streams. The packets are optional in SD-SDI and HD-SDI data streams.

The ST 352 packet insertion function takes the user data words of the ST 352 packet from the VPID input ports: `tx_vpid_byte1`, `tx_vpid_byte2`, `tx_vpid_byte3`, `tx_vpid_byte4a`, and `tx_vpid_byte4b`. The `tx_vpid_byte4b` port is only used in 3G-SDI mode to allow unique identification between the two data streams carried on the 3G-SDI interface.

ST 352 packets are inserted on one designated video line in each frame if the transport is progressive, and one designated video line in each field if the transport is interlaced. The designated video lines that carry ST 352 packets vary depending on the SDI mode and the video format as described in the SMPTE ST 352 standard. The ST 352 packet will be inserted at the beginning of the HANC space of the line specified by the `tx_line_f1` input port for progressive video or for the first field of interlaced video. For interlaced video, a ST 352 packet is also inserted on the line specified by the `tx_line_f2` input port. The `tx_line_f2_en` input determines whether packets are inserted in the line specified by `tx_line_f2`. The `tx_line_f2_en` input must be Low for a progressive transport and High for an interlaced transport.

The `tx_line_f2_en` input must be controlled correctly. This input must be High for interlaced video and Low for progressive video. However, this input must be controlled based on whether the transport is interlaced or progressive, not the picture. The 1080p 50 Hz and 60 Hz 4:2:2 10-bit video formats, when carried by dual link HD-SDI or 3G-SDI level B (but not 3G-SDI level A) are transported in an interlaced manner, even though the picture is progressive. The same is true for progressive segmented frame transport. It is essential that the ST 352 packets are inserted into both fields of the transport data streams for these formats. Some receiving equipment fail to lock properly if the ST 352 packets are only present in one field rather than in both fields of interlaced transports.

Dual link HD-SDI data streams coming from a dual link SDI receiver may already have ST 352 packets in the Y data streams of each link, because ST 372 mandates these packets. If the packets are present, the first user data word should be hex 87, indicating that the data streams are carried on a dual link HD-SDI interface. If these dual link data streams are to be retransmitted on a 3G-SDI level B-DL interface, the first user data word of the packet must be replaced with a value of hex 8A, indicating a ST 372 signal carried on a 3G-SDI level B-DL interface. Therefore the ST 352 packets must be modified when sending the dual link HD-SDI streams on a 3G-SDI level B-DL interface. Only the first byte of the VPID data must be modified. The values of the other bytes do not need to change. However, they must be captured first and applied to the VPID byte inputs SDI transmitter so that they are re-inserted when the packet is overwritten (as part of the process of updating the packet). This is because the inserter overwrites the entire packet, not just the first user data word.

In 3G-SDI level B-DS mode, two independent HD-SDI signals are carried by the 3G-SDI level B interface. These two HD-SDI signals can be vertically unsynchronized (not frame-locked). If this is the case, then ST 352 packets are inserted independently on the two HD-SDI signals carried by the 3G-SDI level B-DS interface. The `tx_line_b` input port on the SMPTE SD/HD/3G-SDI core allows two separate line numbers to be provided for level B, one for each HD-SDI signal. As there is only one set of VPID data inputs to the insertion module, the ST 352 packets, with the exception of byte 4, are identical. This means that the two HD-SDI

streams must be carrying identical video formats. This is normally the case because of the restrictions in 3G-SDI level B-DS mode requiring the two HD-SDI streams to be of the same format. If an application requires insertion of different VPID packets into the two HD-SDI signals carried by a 3G-SDI level B signal the ST 352 packets must be generated and inserted into the data streams prior to entering the SDI transmitter and the `tx_insert_vpid` input must be Low.

Line Number Insertion

Both 3G-SDI and HD-SDI modes require that line numbers are present in the two words that follow each EAV. If the `tx_insert_ln` input is High, the SDI transmitter inserts those line numbers appropriately for HD-SDI and both levels of 3G-SDI (inserting them into all four data streams for level B 3G-SDI). The line numbers inserted are provided to SDI transmitter on the `tx_line_a` and `tx_line_b` inputs. In some cases, it might not be necessary or desirable to overwrite line numbers that are already present in the data streams. In that case, the `tx_insert_ln` input can be driven Low and no line numbers are inserted. If the `tx_insert_ln` input is hard wired Low, the line number insertion logic is optimized out of the design by the synthesis tool.

For dual link HD-SDI data streams carried either by dual link HD-SDI or 3G-SDI level B interfaces, if the video format is 1080p 50 Hz, 59.94 Hz, or 60 Hz, the line numbers are required to be transport line numbers, not video line numbers.

For HD-SDI, dual link HD-SDI, and 3G-SDI level A formats, only the line number on `tx_line_a` is used. For 3G-SDI level B, the line number on `tx_line_a` is inserted into the Y and C data streams of link A and the line number on `tx_line_b` is inserted into the Y and C data streams of link B (again, only if `tx_insert_ln` is asserted).

CRC Generation and Insertion

Both 3G-SDI and HD-SDI modes require that CRC values are present in the two words that follow the line numbers after the EAV. If the `tx_insert_crc` input is High, the SDI transmitter calculates and inserts CRC values for each line for HD-SDI, and both levels of 3G-SDI (inserting them into all four data streams for level B 3G-SDI). In some cases, it might not be necessary or desirable to overwrite the CRC values already present in the data stream. In that case, the `tx_insert_crc` input can be driven Low and no CRC values are inserted. If the `tx_insert_crc` input is hard wired Low, the CRC generation and insertion logic is optimized out of the design by the synthesis tool.

EDH Generation and Insertion

EDH packets are optional, but usually present, in SD-SDI. They are never used for HD-SDI and 3G-SDI modes. The EDH packets contain CRC values that can be used to detect errors in the SD-SDI data stream. When running in SD-SDI mode, the SDI transmitter generates and inserts EDH packets when `tx_insert_edh` is High. If `tx_insert_edh` is hard wired Low, the synthesis tool optimizes the EDH generator out of the design. The EDH processor has a flywheel function which generate and inserts EAV and SAV sequences for the SD-SDI

data stream. Once locked to the timing of the SD-SDI data stream, the flywheel will continue to generate and insert valid EAV and SAV sequences in the transmitted data stream, even if the input data stream stops. This flywheel function is a necessary part of the EDH processor and cannot be disabled when EDH packets are being generated and inserted (`tx_insert_edh` is High). This flywheel only works in SD-SDI mode. There is no equivalent flywheel for 3G-SDI or HD-SDI modes.

Ancillary Data Insertion

It is often necessary to embed ancillary data into the SDI data streams before transmission. This is best performed after the ST 352 packets have been inserted, but before any other formatting occurs. Thus, ancillary data insertion is normally performed between the two main functions of the SDI transmitter. The SMPTE SD/HD/3G-SDI core allows this by providing raw data stream outputs after ST 352 packet insertion is completed and accepting data streams in from a ancillary data inserter.

The use of these data paths for ancillary data insertion is, however, optional and the data streams from the ST 352 packet inserter can be routed internally to the remainder of the transmitter section. This is controlled by the `tx_use_dsin` port. When this port is High, the core is configured for operation with a user supplied ancillary data inserter. The data streams containing the ST 352 packets are output on the `tx_dsxx_out` ports to feed to the ancillary data inserter. The data streams from the ancillary data inserter must be connected to the core's `tx_dsxx_in` ports of the core. The number of `tx_dsxx_out` and `tx_dsxx_in` ports that are active vary depending on the SDI mode and level. When the `tx_use_dsin` port is Low, the data streams from the ST 352 inserter are routed, internally, directly to the rest of the transmitter section and the `rx_dsxx_in` ports are not used.

Resets

The RX and TX sections of the core have separate reset input ports named `rx_rst` and `tx_rst`.

The signal on the `rx_rst` input port must be synchronous with the `rx_usrclk` clock. Asserting this input high will reset the entire RX section of the core. However, for all portions of the RX section to be reset, the `rx_ce` and `rx_din_rdy_3G` ports must be High when `rx_rst` is asserted.

The signal on the `tx_rst` input port must be synchronous with the `tx_usrclk` clock. Asserting this input high will reset the entire TX section of the core. However, for all portions of the TX section to be reset, the `tx_ce` and `tx_din_rdy` ports must be High when `tx_rst` is asserted.

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the Vivado® Design Suite environment.

Vivado Integrated Design Environment

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click on the selected IP or select the Customize IP command from the toolbar or popup menu.

For details, see the sections, "Working with IP" and "Customizing IP for the Design" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 10] and the "Working with the Vivado IDE" section in the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 12].

If you are customizing and generating the core in the Vivado IP Integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* (UG994) [Ref 14] for detailed information. IP Integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value you can run the `validate_bd_design` command in the Tcl console.

Note: Figures in this chapter are illustrations of the Vivado IDE. This layout might vary from the current version.

Interface

The SMPTE SD/HD/3G-SDI core is easily configured to meet your specific needs through the Vivado tools interface. This section provides a quick reference to parameters that can be configured at generation time.

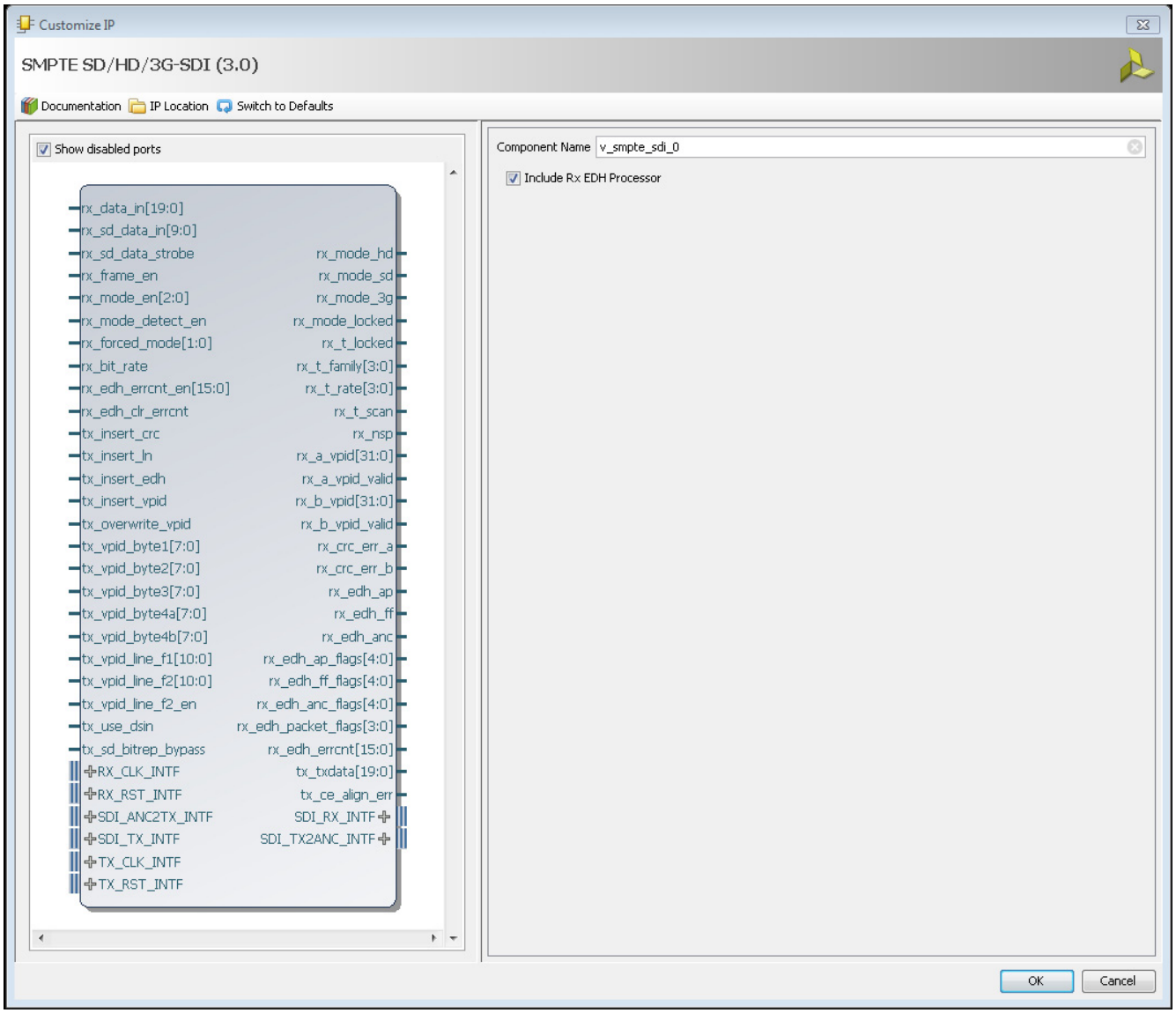

Figure 4-1: **Vivado IP Catalog GUI**

Only one parameter/generic is exposed and editable in the GUI. This is the parameter `INCLUDE_RX_EDH_PROCESSOR`. If this parameter is **ENABLED**, then the EDH processor for the receiver section of the SMPTE SD/HD/3G-SDI core is included. If this parameter is **DISABLED**, then the EDH processor for the receiver section is not included.

Output Generation

For details, see "Generating IP Output Products" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 10].

Constraining the Core

Required Constraints

The only constraints required by the SMPTE SD/HD/3G-SDI core are clock period constraints on the `rx_usrclk` and `tx_usrclk`. These constraints are provided in the XDC constraints file included with the core.

IMPORTANT: *Apply constraints as appropriate to your design. Refer to References in Appendix D for a list of device-specific application notes.*

Clock Frequencies

When using the transceivers in Xilinx FPGAs, the maximum frequency of the `rx_usrclk` and `tx_usrclk` clocks is 148.5 MHz. The following example constraints could be used for a design with two SDI interfaces where the clocks connected to the `rx_usrclk` ports of the two SDI cores are named `rx1_usrclk` and `rx2_usrclk` and the clocks connected to the `tx_usrclk` ports of the two SDI cores are named `tx1_usrclk` and `tx2_usrclk`.

```
create_clock -name rxusrclk -period 6.667 -waveform (0.0000 3.3333) [get_nets
{rx1_usrclk rx2_usrclk}]

create_clock -name txusrclk -period 6.667 -waveform (0.0000 3.3333) [get_nets
{tx1_usrclk tx2_usrclk}]
```

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 13].

Synthesis and Implementation

For details about synthesis and implementation, see "Synthesizing IP" and "Implementing IP" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 10].

Detailed Example Design

No example design is available at the time for the SMPTE SD/HD/3G-SDI 3.0 core.

Test Bench

This chapter contains information about the provided test bench in the Vivado® Design Suite environment.

Demonstration Test Bench

A demonstration test bench is provided with the core which enables you to observe core behavior in a typical scenario. This test bench is generated together with the core in Vivado Design Suite. The test bench applies a video signal to the inputs of the TX section of the SDI core. The output of the TX section is connected to the input RX section of the SDI core. The outputs of the RX section are examined to make sure that the RX locks to the signal and receives it correctly. 10 different video formats are tested in this manner, testing SD-SDI, HD-SDI, 3G-SDI level A and 3G-SDI level B.

Directory and File Contents

The following file is expected to be generated in the demonstration test bench output directory:

The test bench

- tb_<IP_instance_name>.v

Test Bench Structure

The top-level entity is **tb_<IP_instance_name>**.

It instantiates the following module:

- DUT

  The <IP> core instance under test.

Verification, Compliance, and Interoperability

Hardware Testing

The SMPTE SD/HD/3G-SDI core has been fully tested to with standard off-the-shelf SDI test equipment and is compliant with the SDI standards.

Upgrading

This appendix contains information about migrating from an ISE design to the Vivado Design Suite, and for upgrading to a more recent version of the IP core. For customers upgrading their IP core, important details (where applicable) about any port changes and other impact to user logic are included.

Migrating to the Vivado Design Suite

For information about migration to Vivado Design Suite, see *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 9].

Upgrading in Vivado Design Suite

This section provides information about any changes to the user logic or port designations that take place when you upgrade to a more current version of this IP core in the Vivado Design Suite.

Parameter Changes

There are no parameter changes.

Port Changes

The following port names are changed to lower case letters to match the common standard followed by all the cores.

- rx_mode_HD changed to rx_mode_hd
- rx_mode_SD changed to rx_mode_sd
- rx_mode_3G changed to rx_mode_3g
- rx_level_b_3G changed to rx_level_b_3g
- rx_dout_rdy_3G changed to rx_dout_rdy_3g
- tx_level_b_3G changed to tx_level_b_3g

Other Changes

From v1.0 to v2.0 of the core, the following change took place:

- Removed ISE support.

From v2.0 to v3.0 of the core, the following change took place:

- Converted the ports to all lower case to match with the common standard for all the cores.
- Added Artix-7 device family support.
- Added Virtex-7 GTH transceiver support.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the SMPTE core, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for opening a Technical Support WebCase.

Documentation

This product guide is the main document associated with the SMPTE SD/HD/3G-SDI core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core are listed below, and can also be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)

- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Answer Records for the SMPTE SD/HD/3G-SDI Core

AR 54531

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Xilinx provides premier technical support for customers encountering issues that require additional assistance.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Support Quick Links.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Note: Access to WebCase is not available in all cases. Please login to the WebCase tool to see your specific support options.

Debug Tools

There are many tools available to address SDI design issues. It is important to know which tools are useful for debugging various situations.

Example Design

No example designs are provided with the SMPTE SD/HD/3G-SDI core itself. Instead, example designs are provided in device-specific application notes. See References in Appendix D for a list of device-specific application notes.

Vivado Lab Tools

Vivado inserts logic analyzer and virtual I/O cores directly into your design. Vivado Lab Tools allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature represents the functionality in the Vivado IDE that is used for logic debugging and validation of a design running in Xilinx FPGA devices in hardware.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

Reference Boards

Various Xilinx development boards support the SMPTE SD/HD/3G-SDI core. Typically, a FMC mezzanine board that has an SDI cable driver and cable equalizers is required to implement SDI interfaces with these evaluation boards. These boards can be used to prototype designs and establish that the core can communicate with the system.

7 series FPGA evaluation boards:

- KC705
- VC707
- VC709
- ZC706
- AC701

License Checkers

The SMPTE SD/HD/3G-SDI core does not require a license.

Simulation Debug

Simulation of an SDI interface is not typically done on only the SMPTE SD/HD/3G-SDI core itself, but usually also includes a simulation module of the transceiver plus device-specific logic to control that transceiver and interface it to the SMPTE SD/HD/3G-SDI core. The required transceiver interface and control logic is found in device-specific application notes listed in the Example Design section. One of the pieces of the control and interface logic is the DRU, which allows data to be recovered for 270 Mb/s SD-SDI (a bit rate too slow to be supported by the CDR section of the transceiver). The DRU is only provided as a pre-compiled and encrypted module and it cannot be simulated. In fact, adding it to a design prevents the entire design from being simulated. The device-specific application notes include a simplified simulation model of the DRU that can be used to allow simulation of the complete SDI interface, but these simplified simulation model must be removed and replaced with the actual DRU when targeting an actual hardware implementation. This does prevent a full simulation of a placed and routed design. At this time, there is no work around to this issue.

Simulation of the transmit portion of the SMPTE SD/HD/3G-SDI core requires a source of video providing one or more digital video standards that are supported by the core. The example designs in the device-specific application notes provide video test pattern generators that can provide digital video to the SDI transmitter.

Simulation of the receive portion of the SMPTE SD/HD/3G-SDI core requires a SDI signal source. The easiest way to provide this the simulation model is with a complete simulation of the SDI transmitter including a video source, the TX portion of the SMPTE SD/HD/3G-SDI core, and the transceiver simulation model.

IMPORTANT: *Note that the loopback modes of the transceiver can be used to loop the transceiver's TX section back into the RX section. This is often convenient for simulation as well as hardware debug.*

To determine if the RX section is correctly receiving the SDI signal, look for pulses on the `rx_eav` and `rx_sav` signals at the correct places on each line, absence of pulses on the `rx_crc_err_a` signal, assertion of the `rx_mode_locked` signal. Verify that the `rx_mode` output port is indicating the correct SDI mode when `rx_mode_locked` is asserted. Verify that the video streams output by the receiver match the video streams input to the transmitter, with some amount of latency. Assertion of `rx_t_locked` takes much longer than assertion of `rx_mode_locked` because the transport format detector may take up to two frames of video before it can determine the video format, so the format detector outputs (`rx_t_locked`, `rx_t_family`, `rx_t_rate`, and `rx_t_scan`) are not correct unless the simulation is allowed to run for two full frames of video.

Hardware Debug

Experience has shown that most of the issues that occur when implementing SDI interfaces with Xilinx transceivers are related to clocking and with incorrect use of the transceivers. The SDI core itself is very robust and when the transceiver is properly connected to the SDI core and the clocks are connected correctly, the SDI core will almost always work correctly.

The first thing to check when a SDI receiver or transmitter is not working is that the associated clock from transceiver is running at the correct frequency as shown in Figure C-1. For HD-SDI the receive and transmit clocks that are connected, usually through a BUFG, to the `rx_usrsclk` and `tx_usrclk` ports of the SMPTE SD/HD/3G-SDI core should have a frequency of either 74.25 MHz or 74.1758 MHz, depending on which HD-SDI bit rate is being received or transmitted. For 3G-SDI, these clocks should have a frequency of 148.5 MHz or 148.35 MHz, again depending on which 3G-SDI bit rate is being received or transmitted. For SD-SDI, the `rx_usrclk` frequency could be either 148.5 MHz or 148.35 MHz, depending on the frequency of the reference clock used by the RX section of the transceiver. Also for SD-SDI TX, the `tx_usrclk` must always be 148.5 MHz, never 148.35 MHz.

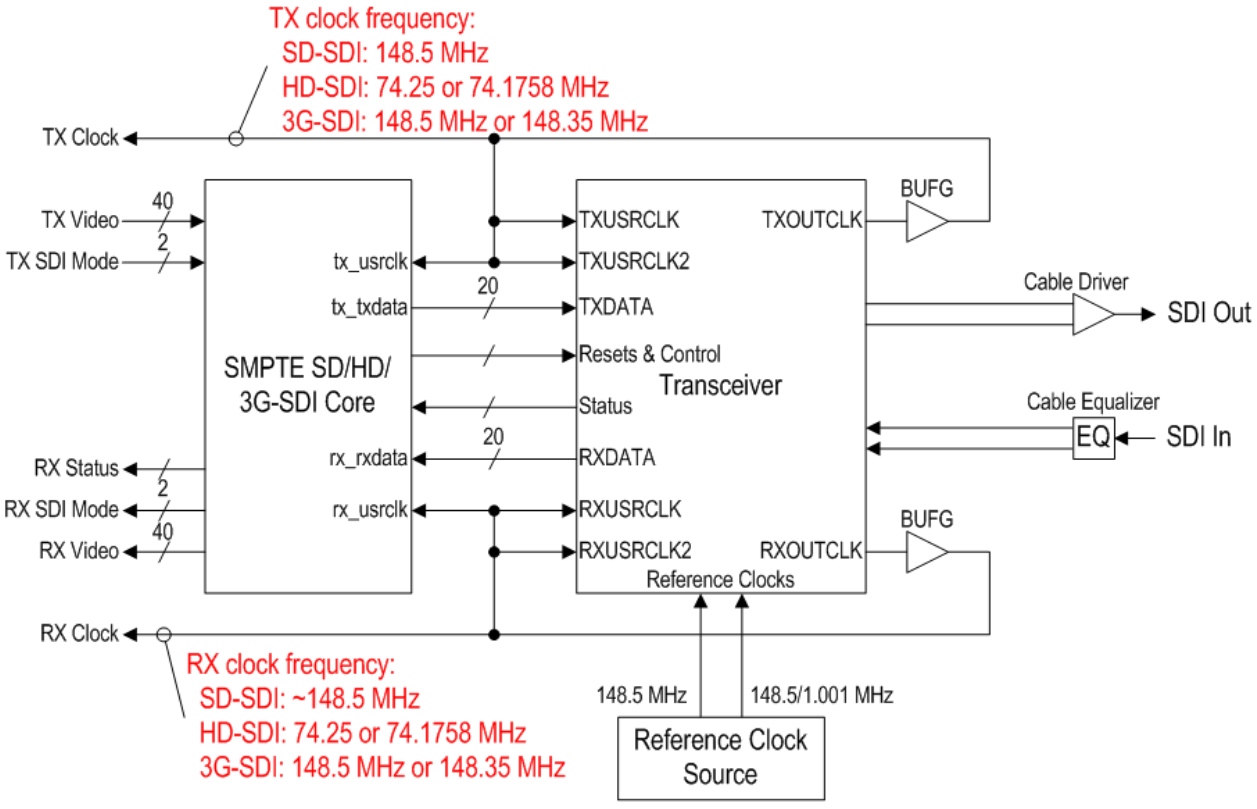

Figure C-1: **Correct RX and TX Clock Frequencies**

If the clocks are halted or running at incorrect frequencies, then there is probably a problem with the transceiver or the reference clocks to the transceiver. Perhaps the PMA PLLs did not get properly reset after the reference clocks became stable. Using ChipScope to manually assert various resets on the transceiver can help to determine if there is a problem with a reset signal not getting asserted or not being asserted at the right time. Also check that the resets to the transceiver are not being asserted all of the time and preventing the transceiver from operating properly.

Another issue that occurs commonly is that the clock driving `tx_usrclk` port of the SMPTE SD/HD/3G-SDI core and the `TXUSRCLK` and `TXUSRCLK2` ports of the transceiver is not frequency locked to the reference clock used by the TX portion of the transceiver. This problem is avoided if the `TXOUTCLK` of the transceiver is the clock driving `tx_usrclk`, `TXUSRCLK`, and `TXUSRCLK2` as shown in Figure C-1. But, if another clock is used to drive these clock inputs, then this clock must be frequency locked to `TXOUTCLK` and the reference clock driving the TX section of the transceiver. If these clocks are not frequency locked, then the `TXBUFFER` in the transceiver will quickly under or overflow, causing corruption of the serial bit stream generated by the transceiver. Xilinx transceivers have a status port that can be monitored to determine if the `TXBUFFER` is under or overflowing. On the 7-series transceiver, the `TXBUFFER` under/overflow signal is bit 1 of the `TXBUFSTATUS` port. If this signal ever becomes asserted High, then the `TXBUFFER` has under or overflowed.

The loopback mechanism built into Xilinx transceivers is a very useful debugging tool. This mechanism allows you to loop the TX portion of the transceiver back to the RX portion, internally to the transceiver. Thus, if you have a working SDI transmitter, you can use that to test that the SDI receiver is working. Or if you have a working SDI receiver, you can use that to test that the SDI transmitter is working correctly, shown in Figure C-2.

Another useful technique, also shown in Figure C-2, used to determine if the data stream going into the `TXIN` port of the transceiver from the TX section of the SMPTE SD/HD/3G-SDI core is a valid SDI data stream involves connecting the data stream that goes the transceiver's `TXDATA` port to the `rx_data_in` port of the RX section of the SMPTE SD/HD/3G-SDI core and then monitor the status and video output ports of the RX section of the core with ChipScope. If the RX section of the core locks to the data stream and produces correct video and status signals on its output, then the data stream going into the TX section of the transceiver is correct. Note that to verify SD-SDI with this technique, the appropriate device-specific SDI wrapper should be used instead of just the SMPTE SD/HD/3G-SDI core or the extra SDI receiver used to monitor the `TXDATA` data stream. The SDI wrapper will include the DRU allowing receipt of SD-SDI as well as HD-SDI and 3G-SDI.

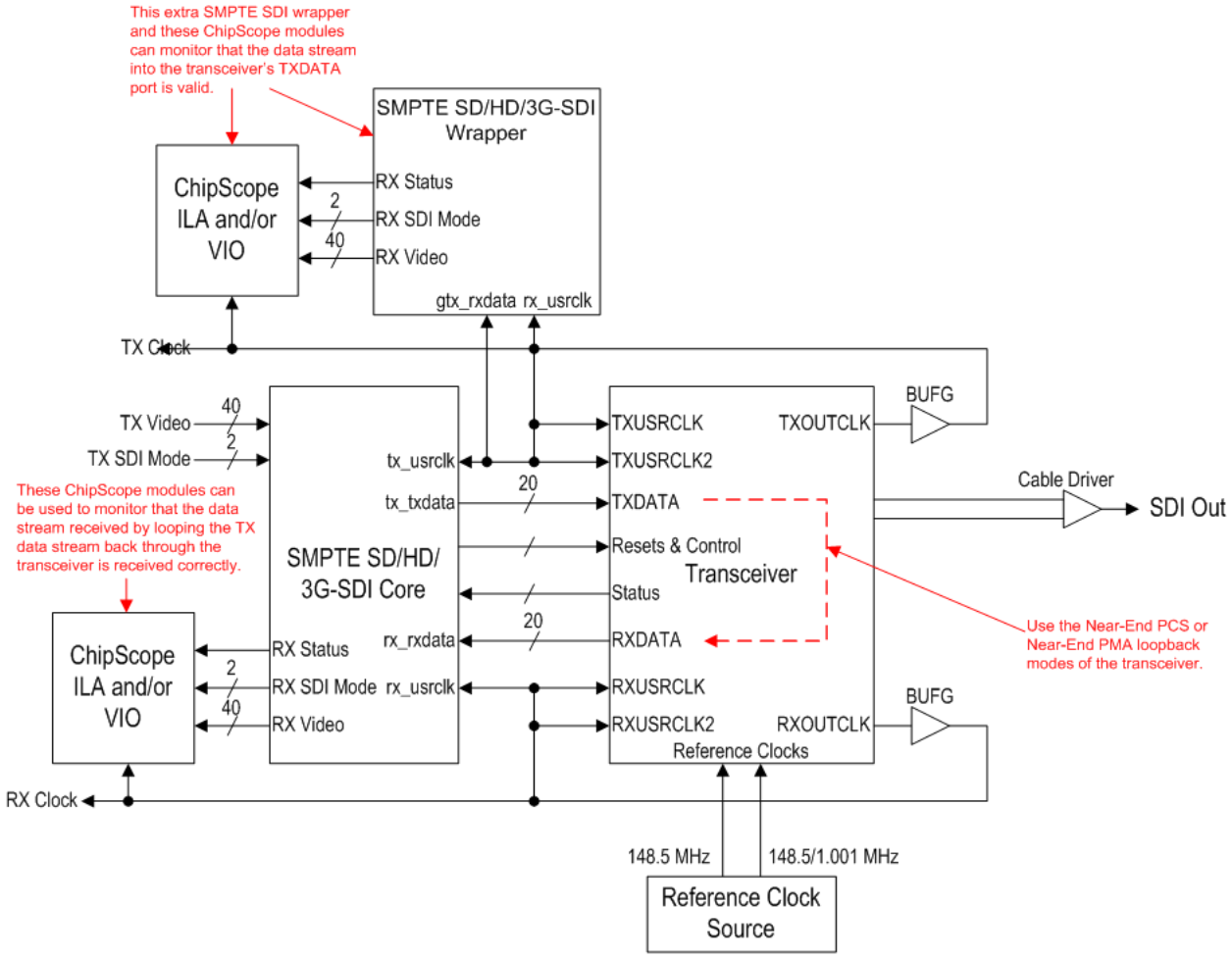

Figure C-2: **Using ChipScope with Loopback to Debug SDI Interfaces**

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The following documents are available from the Society of Motion Picture and Television Engineers web site (www.smpte.org):

1. SMPTE RP 165: Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
2. ST 259M: SDTV Digital Signal/Data Serial Digital Interface
3. ST 292-1: 1.5 Gb/s Signal/Data Serial Interface
4. ST 352: Payload Identification Codes for Serial Digital Interfaces
5. ST 372: Dual Link 1.5 Gb/s Digital Interface for 1920 x 1080 and 2048 x 1080 Picture Formats
6. ST 424: 3 Gb/s Signal/Data Serial Interface
7. ST 425-1: Source Image Format and Ancillary Data Mapping for the 3 Gb/s Serial Interface
8. *Implementing SMPTE SDI Interfaces with Kintex-7 GTX Transceivers* (XAPP592)
9. *ISE to Vivado Design Suite Migration Guide* (UG911)
10. *Vivado Design Suite User Guide: Designing with IP* (UG896)
11. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
12. *Vivado Design Suite User Guide: Getting Started* (UG910)
13. *Vivado Design Suite User Guide: Logic Simulation (*UG900*)*
14. *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* (UG994)
15. Implementing SMPTE SDi Interfaces with Artix-7 GTP Transceivers (XAPP1097)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/02/2018	3.0	Removed references to discontinued Xilinx application notes.
04/06/2016	3.0	Updated for Kintex® UltraScale™ and Virtex® UltraScale family support.
10/02/2013	3.0	Synch document version with core version. Updated Constraints. Added Migration appendix. Added Artix®-7 device family support. Changed the ports to from upper case to lower case.
03/20/2013	1.2	Updated for core version. Removed ISE chapters.
12/18/2012	1.1	Updated Designing with the Core chapter and Debugging appendix.

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