

HDMI 1.4/2.0 Receiver Subsystem v3.0

Product Guide

Vivado Design Suite

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Introduction

The HDMI 1.4/2.0 Receiver Subsystem is a hierarchical IP that bundles a collection of HDMI® RX IP sub-cores and outputs them as a single IP. It is an out-of-the-box ready-to-use HDMI 1.4/2.0 Receiver Subsystem and avoids the need to manually assemble sub-cores to create a working HDMI RX system.

Features

- HDMI 2.0 and 1.4b compatible
- 2 or 4 symbol/pixel per clock input
- Supports resolutions up to 4,096 x 2,160 @ 60 fps
- 8, 10, 12, and 16-bit Deep-color support
- Support color space for RGB, YUV 4:4:4, YUV 4:2:2, YUV 4:2:0
- Support AXI4-Stream Video output stream and Native Video output stream
- Audio support for up to 8 channels
- High bit rate (HBR)
- Info frames
- Data Display Channel (DDC)
- Hot-Plug Detection
- 3D video support
- Optional High Bandwidth Digital Content Protection (HDCP) 1.4 support
- Optional HDCP 2.2 support
- Optional Video over AXIS compliant NTSC/PAL Support
- Optional Video over AXIS compliant YUV420 Support
- Optional HPD Active polarity
- Optional Cable Detect Active polarity

LogiCORE™ IP Facts Table	
Subsystem Specifics	
Supported Device Family ⁽¹⁾	UltraScale+™ Families (GTHE4) UltraScale™ Architecture (GTHE3) Zynq®-7000 All Programmable SoC 7 Series (GTXE2, GTHE2) Artix®-7 (GTPE2) ⁽²⁾
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Resources	Performance and Resource Utilization web page
Provided with Subsystem	
Design Files	RTL
Example Design	Vivado IP Integrator and associated software application example
Test Bench	Not Provided
Constraints File	XDC
Simulation Model	Not Provided
Supported S/W Driver ⁽³⁾	Standalone
Tested Design Flows⁽⁴⁾	
Design Entry	Vivado® Design Suite
Simulation	Simulation is not supported for HDMI Receiver Subsystem
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. Only HDMI 1.4 is supported in Artix and Kintex -1 devices.
3. Standalone driver details can be found in the SDK directory (<install_directory>/SDK/<release>/data/embeddedsw/doc/xilinx_drivers.htm). Linux OS and driver support information is available from the [Xilinx Wiki page](#).
4. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Overview

The HDMI 1.4/2.0 Receiver Subsystem is a feature-rich soft IP incorporating all the necessary logic to properly interface with PHY layers and provide HDMI decoding functionality. The subsystem is a hierarchical IP that bundles a collection of HDMI RX-related IP sub-cores and outputs them as a single IP. The subsystem receives the captured TMDS data from the video PHY layer. It then extracts the video and audio streams from the HDMI stream and converts it to video and audio streams.

The subsystem can be configured at design time through a single interface in the Vivado® Integrated Design Environment (IDE) for performance and quality.

Applications

High-Definition Multimedia Interface (HDMI) is a common interface used to transport video and audio and is seen in almost all consumer video equipment such as DVD and media players, digital televisions, camcorders, mobile tablets and phones. The omnipresence of the interface has also spread to most professional equipment such as professional cameras, video switchers, converters, monitors and large displays used in video walls and public display signs.

For tested video resolutions for the subsystem see [Appendix A, Verification, Compliance, and Interoperability](#).

Unsupported Features

The following features are not supported in this subsystem:

- Lip sync
- CEC
- HEAC
- HDMI 2.0 dual view
- HDMI 2.0 multi stream audio

Licensing and Ordering Information

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado synthesis
- Vivado implementation
- write_bitstream (Tcl command)



IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

If a Hardware Evaluation License is being used, the core stops transmitting HDMI Stream after timeout. This timeout is based on system CPU clock. For example, if system is running at 100 Mhz, the IP times out after approximately 4 hours of normal operation when Hardware Evaluation License is being used.

License Type

This Xilinx® LogiCORE™ IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado® Design Suite. For full access to all subsystem functionalities in simulation and in hardware, you must purchase a license for the subsystem. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the Xilinx HDMI [web page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

Product Specification

This chapter includes a description of the subsystem and details about the performance and resource utilization.

Introduction

A high-level block diagram of the HDMI 1.4/2.0 Receiver Subsystem is shown in [Figure 2-1](#).

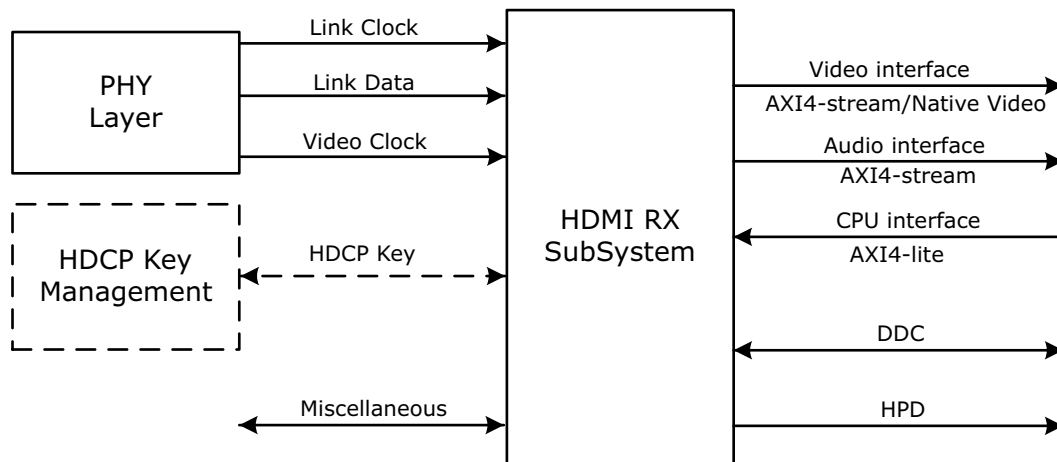


Figure 2-1: Subsystem Block Diagram

The HDMI RX Subsystem is constructed on top of an HDMI RX core. Various supporting modules are added around the HDMI RX core with respect to your configuration. The HDMI RX core is designed to support native video interface, however many of the existing video processing IP cores are AXI4-Stream based. It is a natural choice to add a converter module (Video In to AXI4-Stream) to enable the HDMI RX Subsystem to output AXI4-Stream based video. By performing this, HDMI RX Subsystem is able to work seamlessly with other Xilinx video processing IP cores. The HDMI RX Subsystem has a built-in capability to optionally support both HDCP 1.4 and HDCP 2.2 decryption.

[Figure 2-2](#) shows the internal structure of the HDMI RX Subsystem when **AXI4-Stream Video Interface** is selected as video interface. In this illustration, both HDCP 1.4 and HDCP 2.2 are selected and both Video over AXIS compliant NTSC/PAL Support and Video over AXIS compliant YUV420 Support are selected.

The HDMI 1.4/2.0 Receiver Subsystem supports two types of video interface:

- AXI4-Stream Video Interface
- Native Video Interface

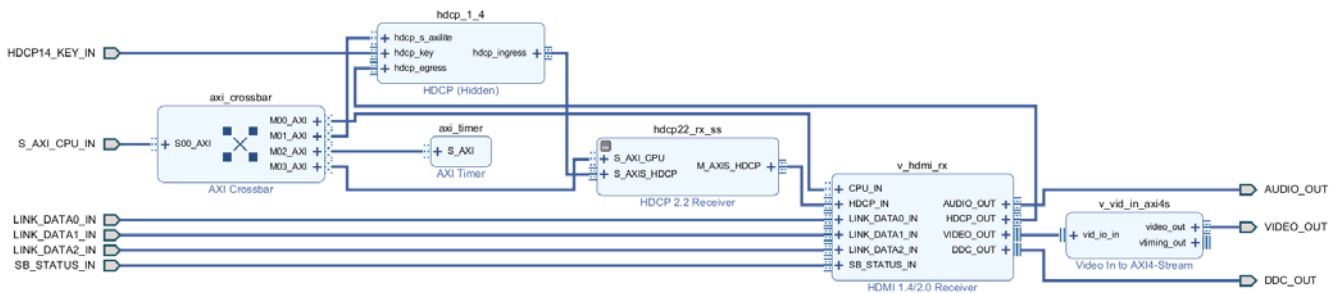


Figure 2-2: HDMI RX Subsystem Internal Structure in AXI4-Stream Video Interface Mode

The HDMI RX Subsystem also provides an option to support a native video interface by constructing the HDMI RX Subsystem without the Video In to AXI4-Stream Bridging module. Therefore, the HDMI RX Subsystem is allowed to output native video to its own video devices. In native video mode, the HDMI RX Subsystem still has a built-in capability to optionally support both HDCP 1.4 and HDCP 2.2 decryption.

Figure 2-3 shows the internal structure of the HDMI RX Subsystem when **Native Video Interface** is selected as video interface. In this illustration, both HDCP 1.4 and HDCP

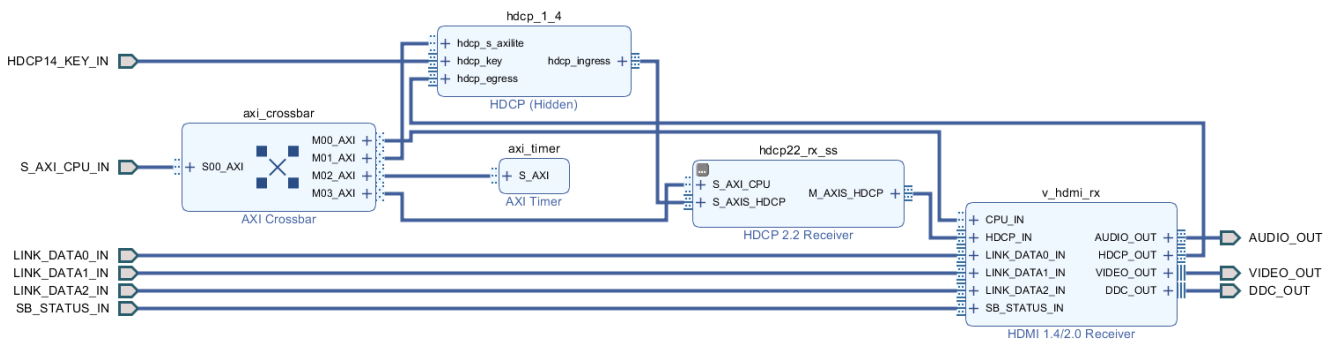


Figure 2-3: HDMI RX Subsystem Internal Structure in Native Video Interface Mode

The data width of the video interface is configured in the Vivado IDE by setting the **Number of Pixels Per Clock on Video Interface** and the **Max Bits Per Component** parameters.

The audio interface is a 32-bit AXI4-Stream master bus. The subsystem converts the captured audio to a multiple channel AXI audio stream and outputs the audio data on this interface.

The CPU interface is an AXI4-Lite bus interface, which is connected to a MicroBlaze™, Zynq®-7000 SoC, or Zynq UltraScale™+ MPSoC processor. Multiple submodules are used to construct the HDMI RX Subsystem and all the submodules which require software access are connected through an AXI crossbar. Therefore, the MicroBlaze, Zynq-7000 SoC, or Zynq

UltraScale+ MPSoC processor is able to access and control each individual submodules inside the HDMI RX Subsystem.



IMPORTANT: *The direct register level access to any of the submodules is not supported.*

The HDMI RX Subsystem device driver has an abstract layer of API to allow you to implement certain functions. This AXI4-Lite slave interface supports single beat read and write data transfers (no burst transfers).

The HDMI RX subsystem is connected to a Xilinx Video PHY Controller, which takes electronic signals from a HDMI cable and translates it into HDMI stream. Then, the HDMI RX subsystem converts the HDMI stream into video stream and audio stream. Based on the configuration selected, the HDMI RX Subsystem sends the video stream in either Native Video format or AXI4-Stream format together with the AXI4-Stream Audio to other processing modules.

The subsystem also supports the features described in the following sections.

Audio Clock Regeneration Signals

The subsystem can output Audio Clock Regeneration (ACR) signals that allow receiver audio peripherals to regenerate the audio clock.

The audio clock regeneration architecture is not part of the HDMI RX subsystem. You must provide an audio clock to the application. This can be achieved by using an internal PLL or external clock source, depending on the audio clock requirements, audio sample frequency and jitter. When HDMI TX subsystem is used in DVI mode, the ACR inputs are ignored. You can decide to leave them open or connect them to some fix values (for example, connecting `acr_cts`, `acr_n`, and `acr_valid` to 0). When HDMI RX subsystem is used in DVI mode, the ACR outputs can be left unconnected. See [Chapter 5, Example Design](#) for an example ACR module that is part of the audio pattern generation system.

Display Data Channel (DDC)

The subsystem allows the end-user to build an HDMI sink device, which negotiates with the targeted HDMI source device for supported features and capabilities. The communication between the source device(s) and the sink device is implemented through the DDC lines, which is an I2C bus included on the HDMI cable.

Note: The DDC signals can be left disconnected when using the HDMI core in DVI only mode without HDCP.

Status and Control Data Channel (SCDC)

The subsystem supports following two bits in SCDC register address offset 0x20 for TMDS configurations (Table 10-19 of HDMI 2.0 spec).

- Bit 1 TMDS_BIt_Clock_Ratio
- Bit 0 Scrambling_Enable

Two APIs are available in the driver to use this feature.

- XV_HdmiRx_DdcScdcEnable is used to enable SCDC register.
- XV_HdmiRx_DdcScdcClear is used to clear SCDC register.

Hot Plug Detect

The subsystem supports the Hot Plug Detect (HPD) feature, which is a communication mechanism between HDMI source and HDMI sink devices. For example, when an HDMI cable is inserted between the HDMI source and HDMI sink devices, the cable-detect signal is asserted. The subsystem then outputs a `hpd` signal, which triggers the start of a communication between the source device and sink device.

InfoFrames

There are two basic InfoFrames expected in any HDMI system, which are Auxiliary Video Information (AVI) Infoframe and Audio Infoframe. An InfoFrame is structured with a 4-byte header and 32-byte data (payload). All InfoFrames types are described in detail in CEA-861-F.

In the HDMI RX Subsystem driver, there is a generic API function for you to retrieve the InfoFrame. This is an example of a function call:

```
u8 AuxBuffer[36];
memcpy(AuxBuffer, XV_HdmiRxSs_GetAuxiliary(&HdmiRxSsPtr), sizeof(AuxBuffer));
```

`HdmiRxSsPtr` is a pointer to the HDMI RX Subsystem, and `AuxBuffer` is a local buffer allocated to store the AUX InfoFrame header and payload data.

Figure 2-4 graphically represents an HDMI Infoframe structure, which is one type of HDMI data island packet. For HDMI, all data island packets consist of a 4-byte packet header and a 32 bytes of packet contents. The packet header contains 24 data bits (3 bytes) and 8 bits (1 byte) of BCH ECC parity.

Byte\Bit #	7	6	5	4	3	2	1	0
HB0	Packet Type							
HB1	packet-specific data							
HB2	packet-specific data							
ECC	ECC							

Figure 2-4: Packet Header

The packet body, graphically represented in [Figure 2-5](#), is made from four subpackets; each subpacket includes 56 bits (7 bytes) of data and 8 bits (1 byte) of BCH ECC parity.

Subpacket #	Byte\Bit #	7	6	5	4	3	2	1	0
Subpacket0 (Checksum + 6 data bytes + ECC)	PB0	Checksum							
	PB1	Data Byte 1							
	PB2...PB5	Data Byte 2 - Data Byte 5							
	PB6	Data Byte 6							
	ECC1	ECC							
Subpacket1 (7 Data Bytes + ECC)	PB7	Data Byte 7							
	PB8...PB12	Data Byte 8 - Data Byte 12							
	PB13	Data Byte 13							
	ECC2	ECC							
Subpacket2 (7 Data Bytes + ECC)	PB14	Data Byte 14							
	PB15...PB19	Data Byte 15 - Data Byte 19							
	PB20	Data Byte 20							
	ECC3	ECC							
Subpacket3 (7 Data Bytes + ECC)	PB21	Data Byte 21							
	PB22...PB26	Data Byte 22 - Data Byte 26							
	PB27	Data Byte 27							
	ECC3	ECC							

Figure 2-5: Packet Body

Notes:

1. ECC is calculated in HDMI 1.4/2.0 Receiver Subsystem core. Therefore, must construct HB0...HB2, and PB0, PB1...PB26, PB27 according to HDMI specs in the software.
2. When calculating the checksum value (PB0), the ECC values are ignored.

Refer to section 5.2.3.4 and 5.2.3.5 of the HDMI 1.4 Specification [\[Ref 12\]](#) for more information on the InfoFrame structure.

HDCP

As part of the HDMI RX Subsystem, the Xilinx® LogiCORE™ IP High-bandwidth Digital Content Protection (HDCP™) receivers are designed for receiving of audiovisual content securely between two devices that are HDCP capable. In this HDMI RX Subsystem, both HDCP 1.4 and HDCP 2.2 Receiver IP cores are included. However because HDCP 2.2 supersedes the HDCP 1.4 protocol and does not provide backwards compatibility, you need to decide and choose targeted content protection schemes from the Vivado IDE. Four different options are available to choose from:

- No HDCP
- HDCP 1.4 only
- HDCP 2.2 only

- HDCP 1.4 and HDCP 2.2

As a guideline, HDCP 2.2 is used to decrypt content at Ultra-High Definition (UHD) while HDCP 1.4 is the legacy content protection scheme used at lower resolutions.

Figure 2-6 shows a configuration of the HDMI receiver where both HDCP 1.4 and 2.2 are enabled. With both HDCP protocols enabled, the HDMI Subsystem configures itself in the cascade topology where the HDCP 1.4 and HDCP 2.2 are connected back-to-back. The HDCP Egress interface of the HDMI receiver sends encrypted audiovisual data, which is decrypted by the active HDCP block and sent back into the HDMI receiver over the HDCP Ingress interface to send to other video processing modules in the system through AXI4-Stream Video interface or Native Video interface.

The HDMI receiver subsystem automatically handles HDCP protocol switching when both HDCP 1.4 and HDCP 2.2 protocols are included in the subsystem. Automatic protocol switching is comprised of protocol detection and protocol enablement. The protocol is detected based on the incoming DDC read/write transaction to the HDCP DDC slave device with address 0x74. The HDCP DDC slave is partitioned into a HDCP 1.4 section (0x00 thru 0x44) and a HDCP 2.2 section (0x50 thru 0xC0). The HDMI receiver subsystem detects the protocol based on which section of the HDCP DDC slave is accessed. Upon a protocol detection event, an interrupt is generated and the interrupt service routine disables and resets both protocols, then enable the detected protocol. The entire detection and enablement procedure is transparent to the user application. When the HDMI receiver subsystem includes only a single HDCP protocol, this procedure is not required.

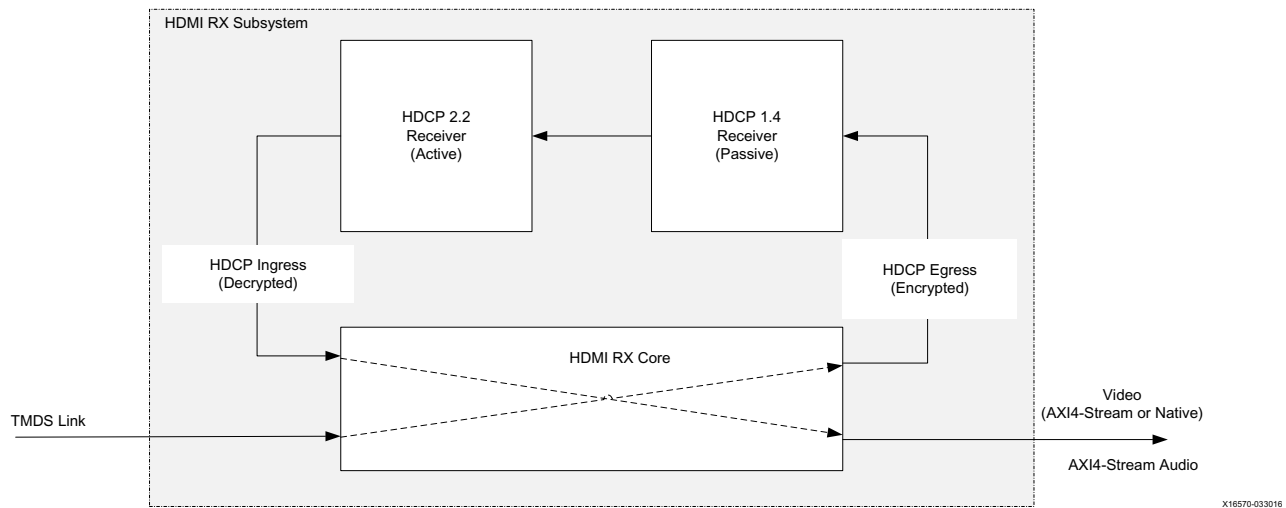


Figure 2-6: HDCP 1.4 and HDCP 2.2 over HDMI Receiver

See *HDCP v2.2 Product Guide* (PG249) [Ref 24] and *HDCP v1.4 Product Guide* (PG224) [Ref 25] for more information.

Standards

The HDMI 1.4/2.0 Receiver Subsystem is compliant with the AXI4-Stream Video Protocol and AXI4-Lite interconnect standards. See the *Vivado AXI Reference Guide* (UG1037) [Ref 1] for additional information. Also, see HDMI specifications [Ref 12].

The HDMI RX Subsystem is compliant with the HDMI 1.4b and HDMI 2.0 specification [Ref 12].

The Xilinx HDCP 1.4 is designed to be compatible with High-bandwidth Digital Content Protection system Revision 1.4 [Ref 13].

The Xilinx HDCP 2.2 is compliant with the HDCP 2.2 specification entitled High-bandwidth Digital Content Protection, Mapping HDCP to HDMI, Revision 2.2, issued by Digital Content Protection (DCP) LLC [Ref 13].

Performance and Resource Utilization

For full details about performance and resource utilization, visit the [Performance and Resource Utilization web page](#).

Maximum Frequencies

Refer to the following documents for information on DC and AC switching characteristics. The frequency ranges specified in these documents must be adhered to for proper transceiver and core operation.

- *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892) [Ref 2]
- *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893) [Ref 3]
- *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS182) [Ref 4]
- *Virtex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183) [Ref 5]
- *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS181) [Ref 6]
- *Zynq-7000 All Programmable SoC: DC and AC Switching Characteristics* (DS187) [Ref 7]
- *Zynq-7000 All Programmable SoC: DC and AC Switching Characteristics* (DS191) [Ref 8]
- *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922) [Ref 9]
- *Virtex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS923) [Ref 10]

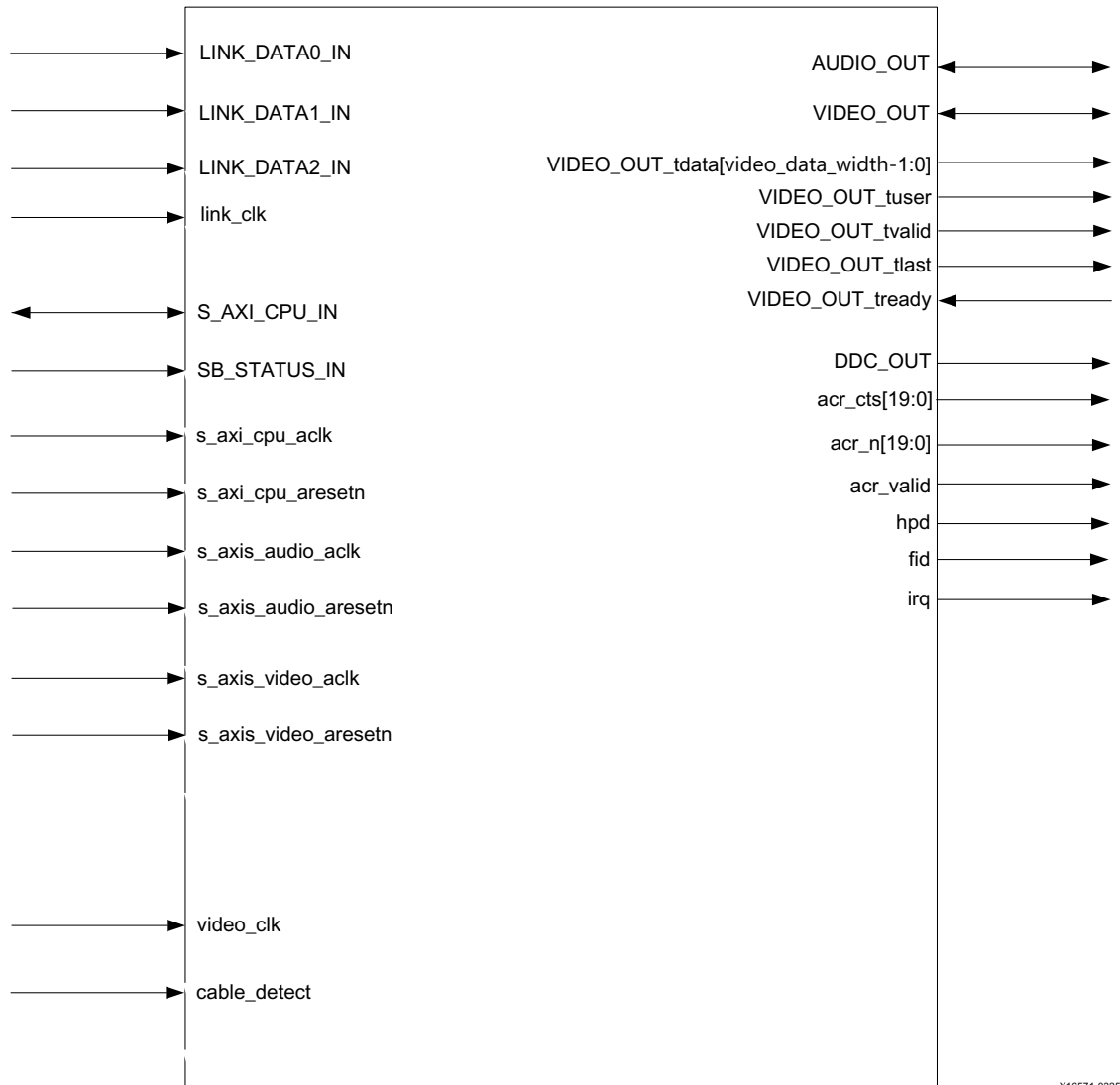
- *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925)*
[\[Ref 11\]](#)
-

Port Descriptions

[Figure 2-7](#) to [Figure 2-10](#) show the HDMI 1.4/2.0 Receiver Subsystem ports when AXI4-Stream is selected as video interface. The VIDEO_OUT port is expanded in the figure to show the detail AXI4-Stream Video bus signals.

The following subsystem has three default interfaces:

- AXI4-Lite control interface (S_AXI_CPU_IN)
- Video Interface (VIDEO_OUT)
- Audio Interface (AUDIO_OUT)



X16571-032516

Figure 2-7: HDMI RX Subsystem Pinout – AXI4-Stream Video Interface (No HDCP)

where

$$\text{video_data_width} = (\text{int}(3 * \text{BPC} * \text{PPC} + 7) / 8) * 8.$$

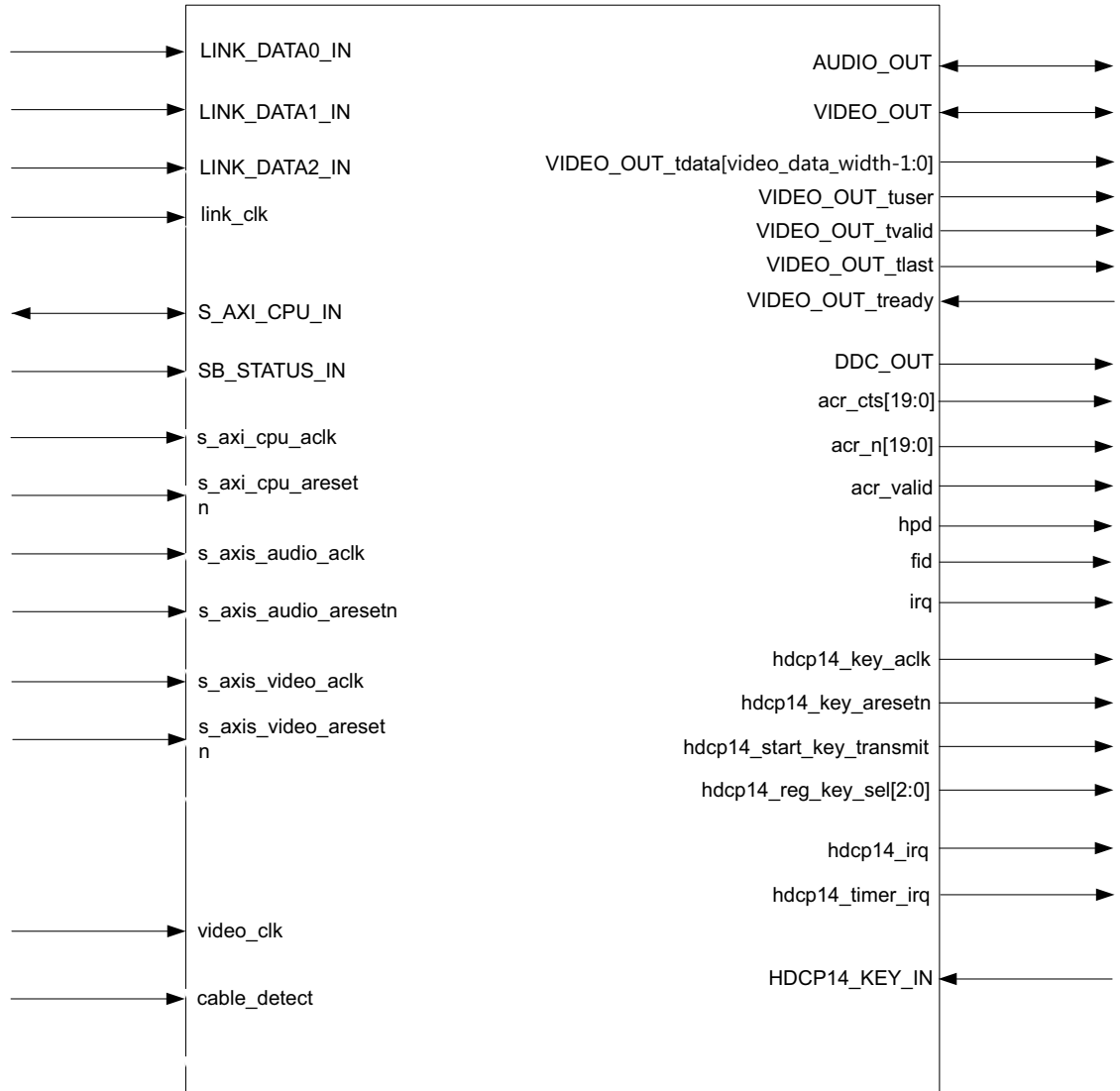
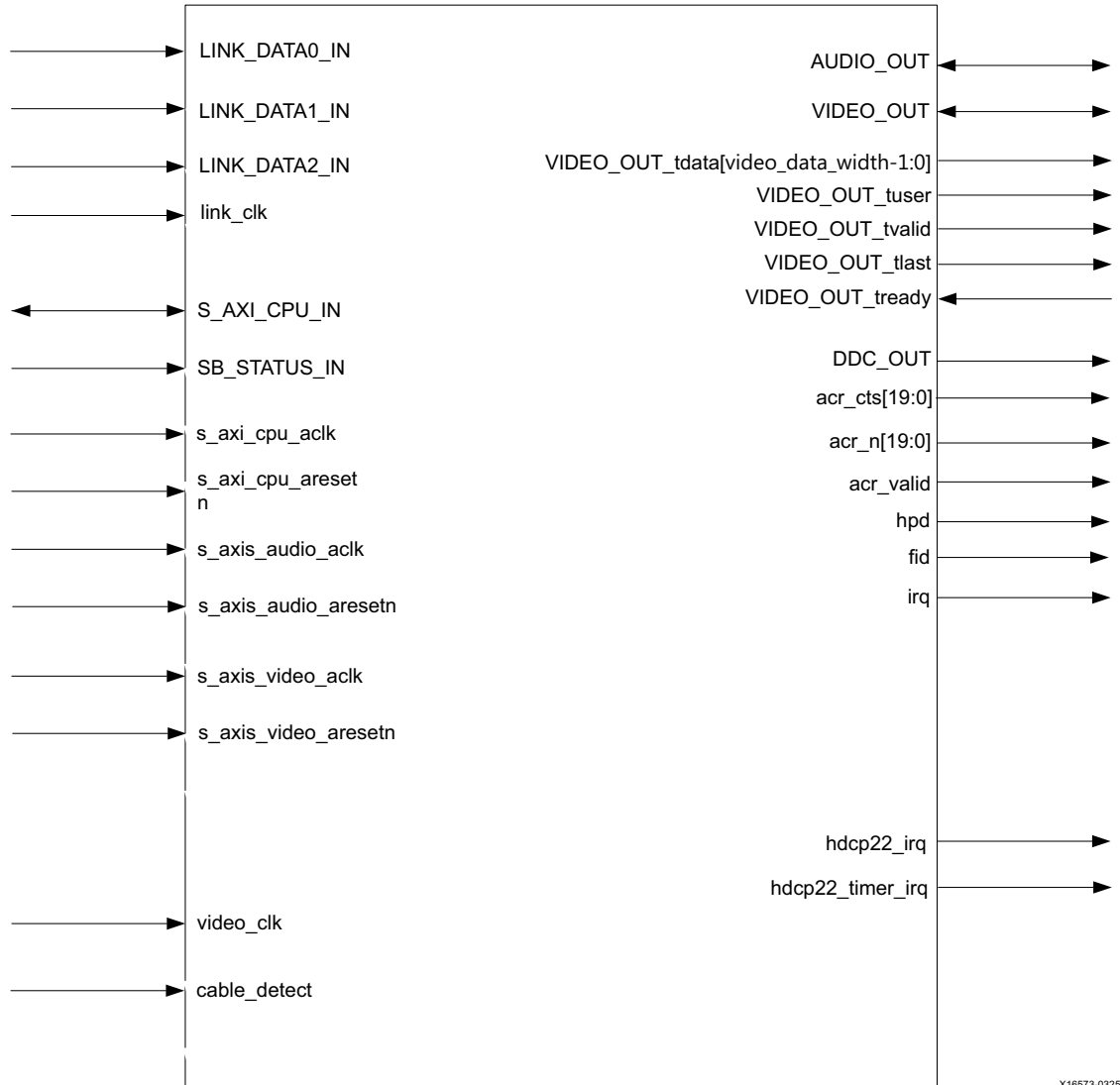
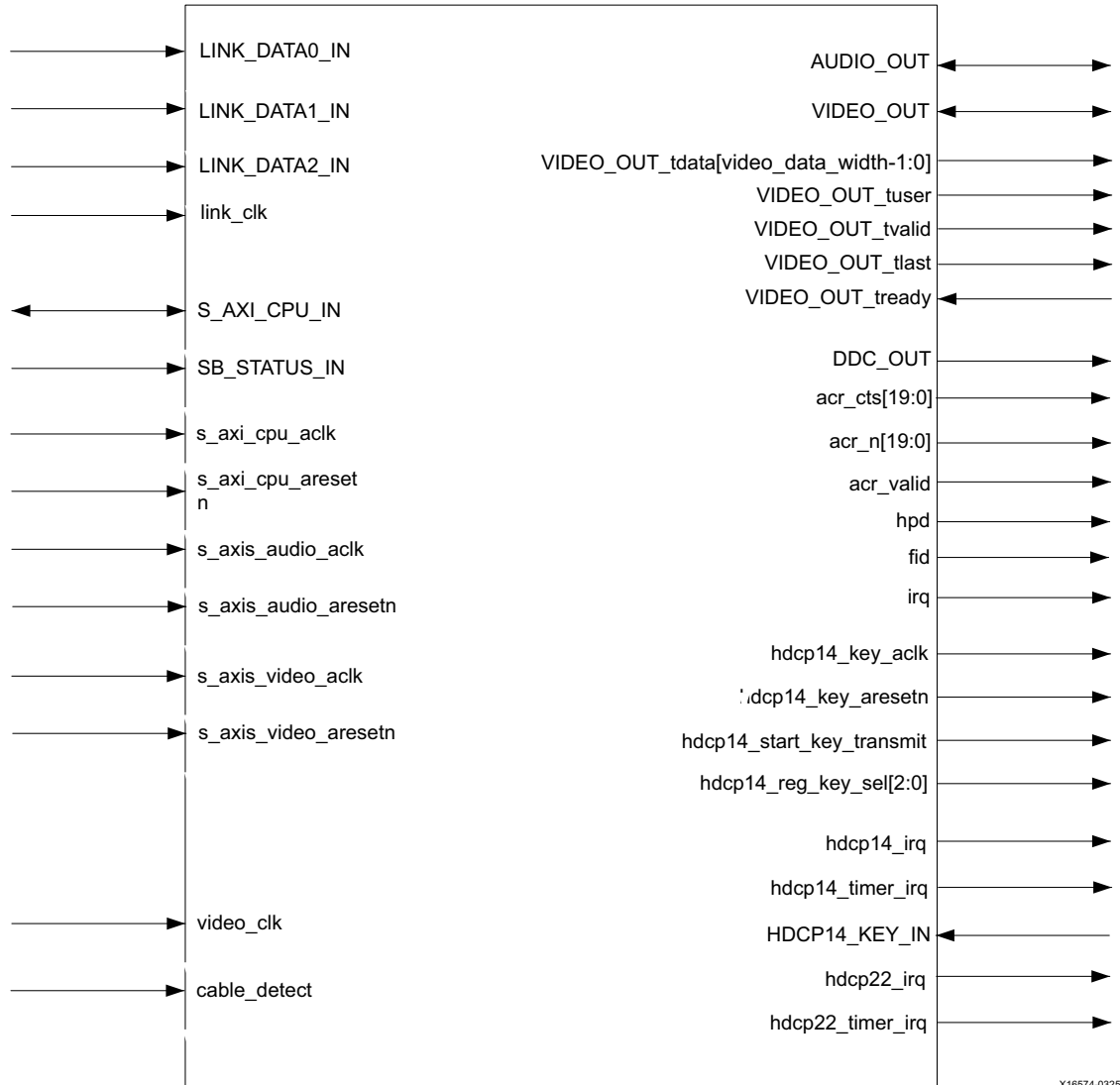


Figure 2-8: HDMI RX Subsystem Pinout – AXI4-Stream Video Interface (HDCP 1.4 Only)



X16573-032516

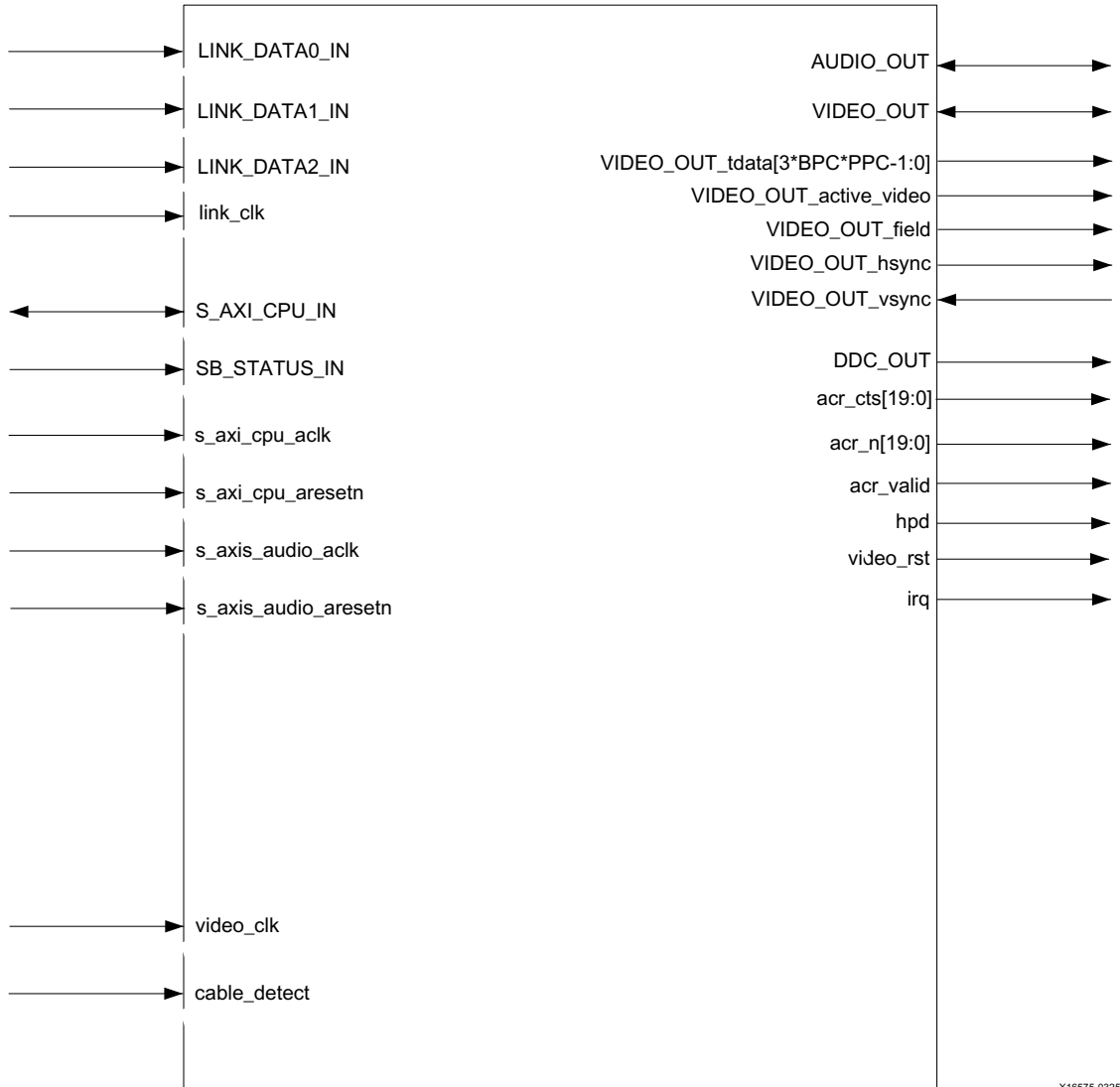
Figure 2-9: HDMI RX Subsystem Pinout – AXI4-Stream Video Interface (HDCP 2.2 Only)



X16574-032516

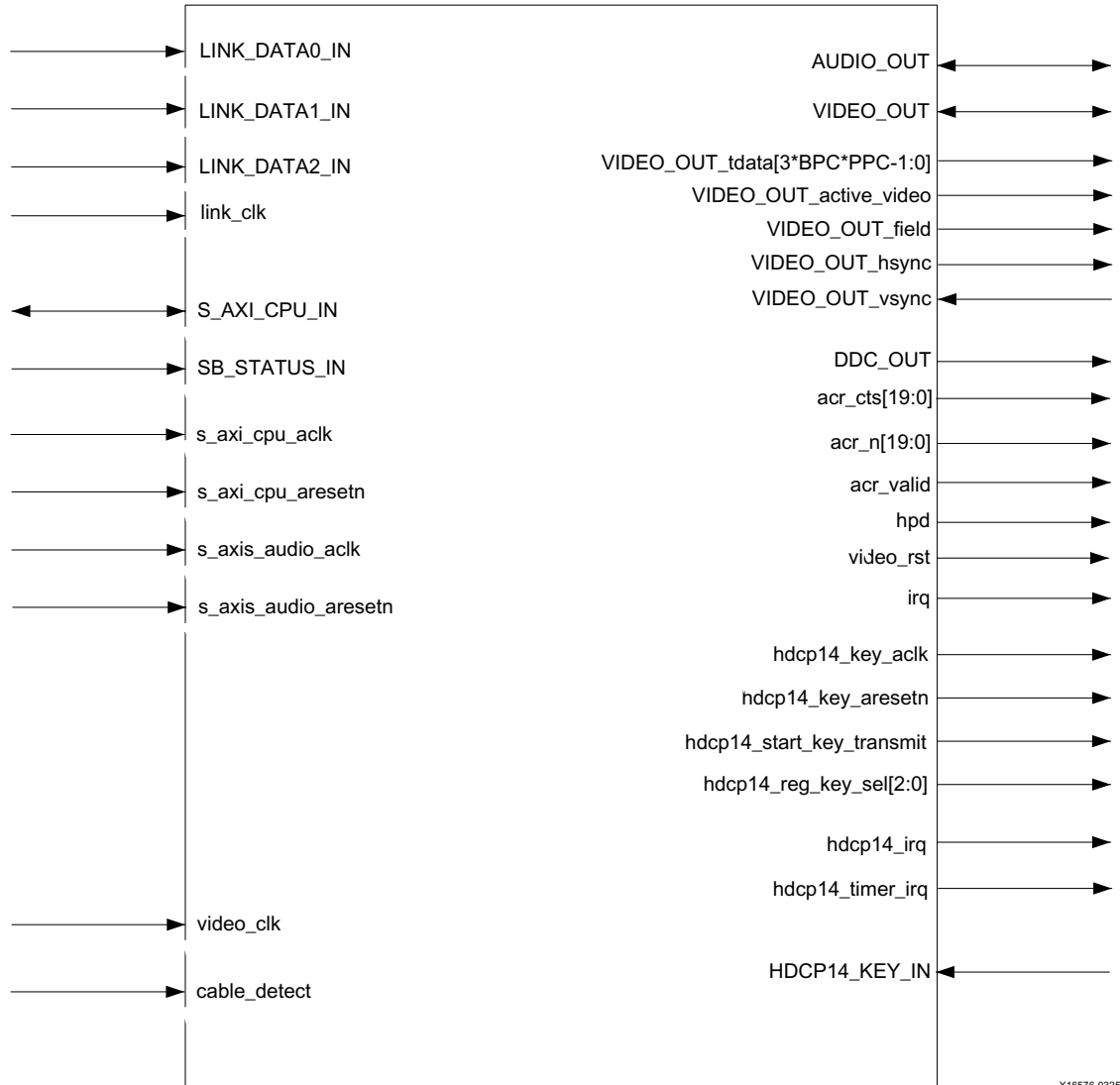
Figure 2-10: HDMI RX Subsystem Pinout – AXI4-Stream Video Interface (HDCP 1.4 and HDCP 2.2)

Figure 2-11 to Figure 2-14 show the HDMI 1.4/2.0 Receiver Subsystem ports when Native Video is selected as video interface. The VIDEO_OUT port is expanded in the figure to show the detail Native Video bus signals.



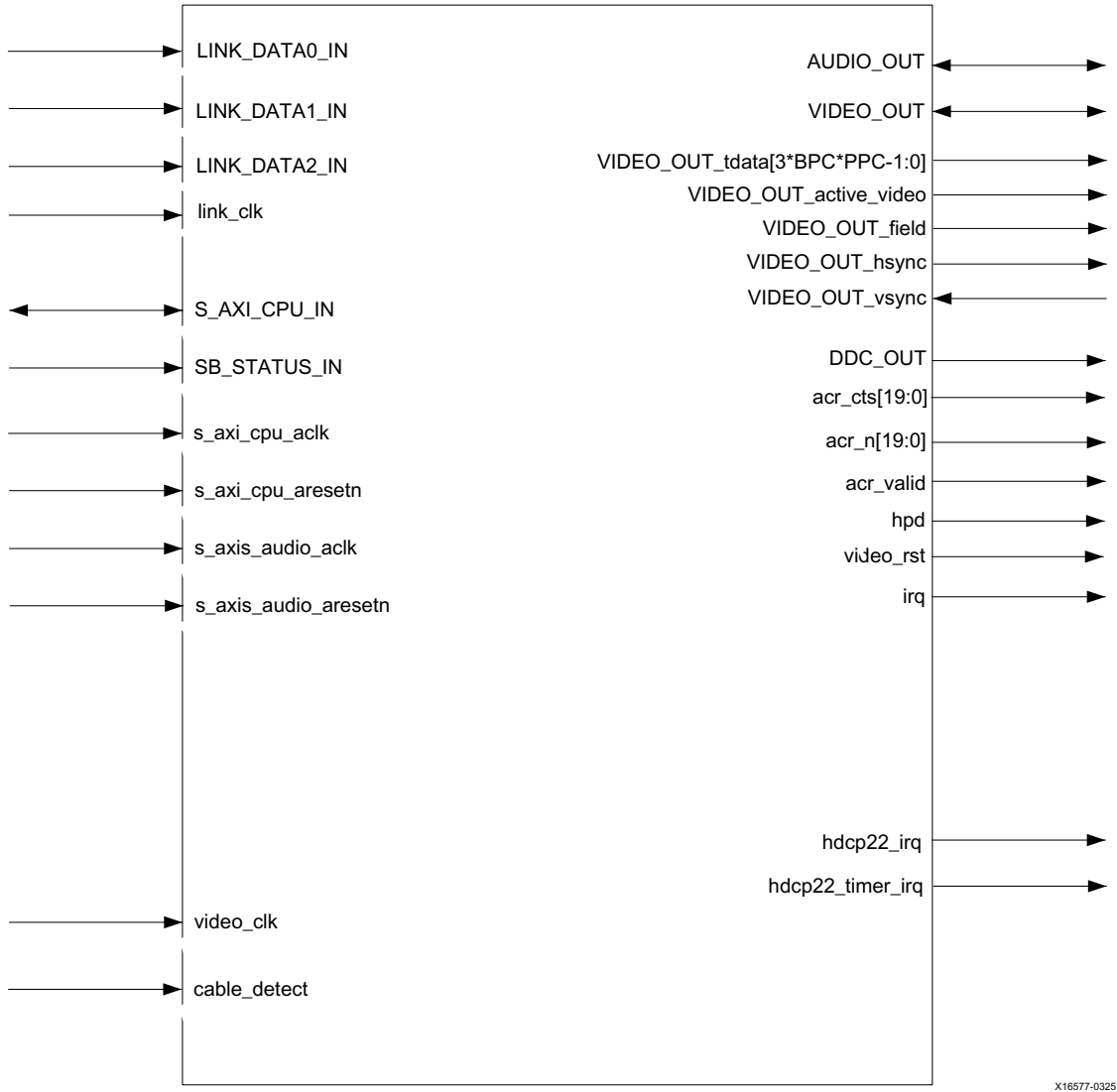
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Figure 2-11: HDMI RX Subsystem Pinout – Native Video Interface (No HDCP)



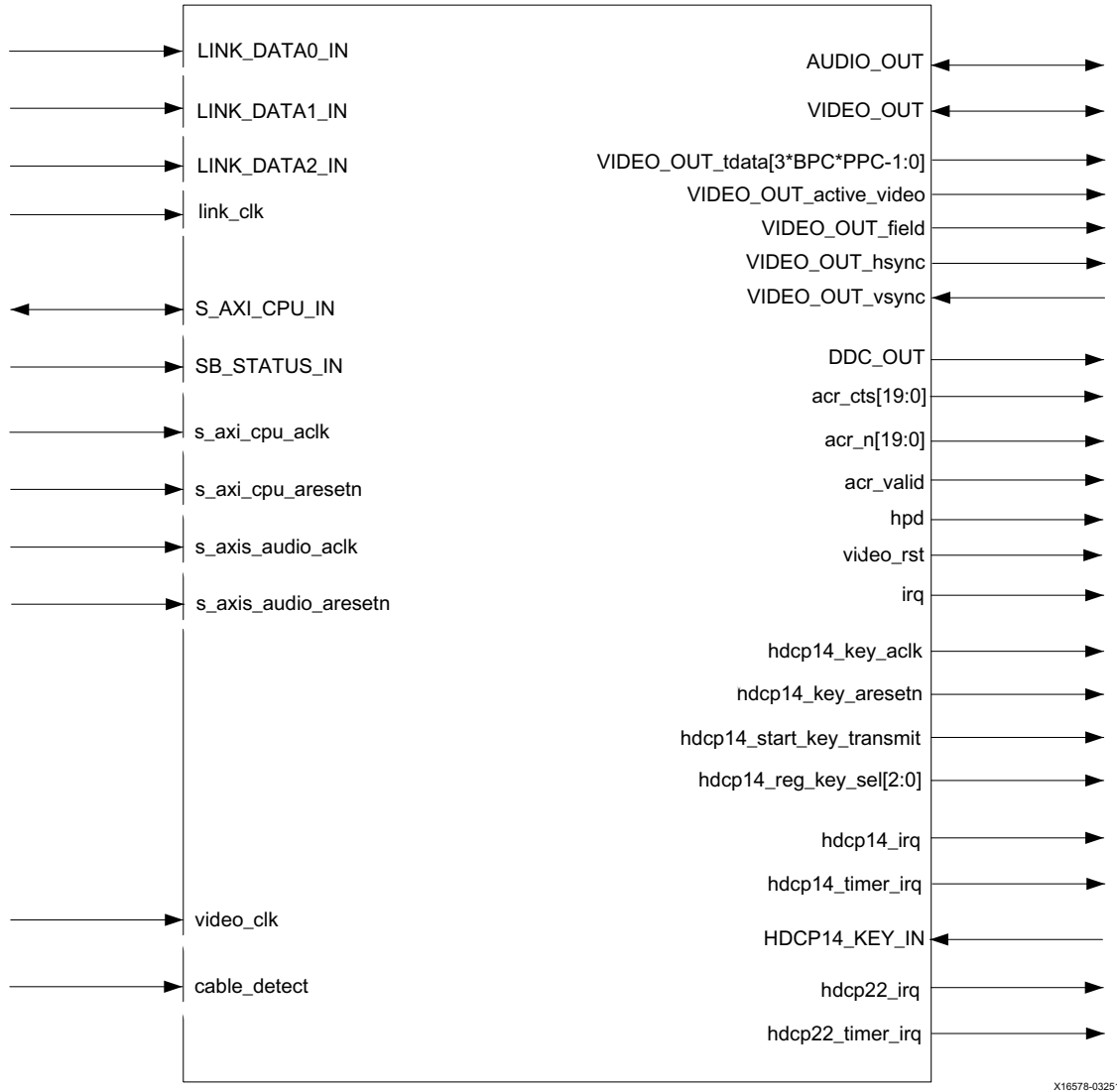
X16576-032516

Figure 2-12: HDMI RX Subsystem Pinout – Native Video Interface (HDCP 1.4 Only)



X16577-032516

Figure 2-13: HDMI RX Subsystem Pinout – Native Video Interface (HDCP 2.2 Only)



X16578-032516

Figure 2-14: HDMI RX Subsystem Pinout – Native Video Interface (HDCP 1.4 and HDCP 2.2)

CPU Interface

Table 2-1 shows the AXI4-Lite control interface signals. This interface is an AXI4-Lite interface and runs at the `s_axi_cpu_aclk` clock rate. Control of the subsystem is only supported through the subsystem driver.



IMPORTANT: *The direct register level access to any of the submodules is not supported. Instead, all the accesses are done through driver APIs.*

Table 2-1: CPU Interface Ports

Name	Direction	Width	Description
<code>s_axi_cpu_aresetn</code>	Input	1	Reset (Active-Low)
<code>s_axi_cpu_aclk</code>	Input	1	Clock for AXI4-Lite control interface
<code>S_AXI_CPU_IN_awaddr</code>	Input	9	Write address
<code>S_AXI_CPU_IN_awprot</code>	Input	3	Write address protection
<code>S_AXI_CPU_IN_awvalid</code>	Input	1	Write address valid
<code>S_AXI_CPU_IN_awready</code>	Output	1	Write address ready
<code>S_AXI_CPU_IN_wdata</code>	Input	32	Write data
<code>S_AXI_CPU_IN_wstrb</code>	Input	4	Write data strobe
<code>S_AXI_CPU_IN_wvalid</code>	Input	1	Write data valid
<code>S_AXI_CPU_IN_wready</code>	Output	1	Write data ready
<code>S_AXI_CPU_IN_bresp</code>	Output	2	Write response
<code>S_AXI_CPU_IN_bvalid</code>	Output	1	Write response valid
<code>S_AXI_CPU_IN_bready</code>	Input	1	Write response ready
<code>S_AXI_CPU_IN_araddr</code>	Input	9	Read address
<code>S_AXI_CPU_IN_arprot</code>	Input	3	Read address protection
<code>S_AXI_CPU_IN_arvalid</code>	Input	1	Read address valid
<code>S_AXI_CPU_IN_aready</code>	Output	1	Read address ready
<code>S_AXI_CPU_IN_rdata</code>	Output	32	Read data
<code>S_AXI_CPU_IN_rresp</code>	Output	2	Read data response
<code>S_AXI_CPU_IN_rvalid</code>	Output	1	Read data valid
<code>S_AXI_CPU_IN_rready</code>	Input	1	Read data ready

Video Output Stream Interface

This HDMI 1.4/2.0 Receiver Subsystem is supporting two types of video output stream interfaces, which eventually is mapped to HDMI 1.4/2.0 Receiver Subsystem VIDEO_OUT interface.

- AXI4-Stream Video interface
- Native Video Interface

Table 2-2 shows the signals for AXI4-Stream video output streaming interface. This interface is an AXI4-Stream master interface and runs at the `s_axis_video_aclk` clock rate. The data width is user-configurable in the Vivado IDE by setting **Max Bits Per Component** (BPC) and **Number of Pixels Per Clock on Video Interface** (PPC).

Table 2-2: Video Output Stream Interface

Name	Direction	Width	Description
<code>s_axis_video_aclk</code>	Input	1	AXI4-Stream clock
<code>s_axis_video_aresetn</code>	Input	1	Reset (Active-Low)
<code>VIDEO_OUT_tdata</code>	Output	$3*BPC*PPC$	Data
<code>VIDEO_OUT_tlast</code>	Output	1	End of line
<code>VIDEO_OUT_tready</code>	Input	1	Ready
<code>VIDEO_OUT_tuser</code>	Output	1	Start of frame
<code>VIDEO_OUT_tvalid</code>	Output	1	Valid

Notes:

1. For AXI4 Stream interface, Video Data width is byte aligned. For example, 10bpc,2ppc data width is 64bits.

Native Video Output Interface

Table 2-3 shows the signals for Native video output interface. This interface is a standard video interface and runs at `video_clk` clock rate. The data width is user-configurable in the Vivado IDE by setting **Max Bits Per Component** (BPC) and **Number of Pixels Per Clock on Video Interface** (PPC).

Table 2-3: Native Video Output Interface

Name	Direction	Width	Description
<code>video_clk</code>	Input	1	Video clock
<code>VIDEO_OUT_field</code>	Output	1	Field ID (only for interlaced video)
<code>VIDEO_OUT_active_video</code>	Output	1	Active video
<code>VIDEO_OUT_data</code>	Output	$(\text{int}(3*BPC*PPC+7)/8)*8$	Data
<code>VIDEO_OUT_hsync</code>	Output	1	Horizontal sync

Table 2-3: Native Video Output Interface (Cont'd)

Name	Direction	Width	Description
VIDEO_OUT_vsync	Output	1	Vertical sync

Notes:

1. When native video interface is selected, s_axis_video_aclk and s_axis_video_aresetn are removed from the HDMI 1.4/2.0 Receiver Subsystem interface ports.
2. video_clk is generated by *Video PHY Controller LogiCORE IP Product Guide* (PG230) [Ref 23].
3. When native video interface is selected, there is no hardware reset.

Audio Output Stream Interface

Table 2-4 shows the signals for AXI4-Stream audio output streaming interfaces. The audio interface transports 24-bits audio samples in the IEC 60958 format. A maximum of eight channels are supported. The audio interface is a 32-bit AXI4-Stream master interface and runs at the s_axis_audio_aclk clock rate.

Table 2-4: Audio Output Stream Interface

Name	Direction	Width	Description
s_axis_audio_aclk	Input	1	Clock (The audio streaming clock must be greater than or equal or greater than 128 times the audio sample frequency)
s_axis_audio_aresetn	Input	1	Reset (Active-Low)
AUDIO_OUT_tdata	Output	32	Data [31] P (Parity) [30] C (Channel status) [29] U (User bit) [28] V (Validity bit) [27:4] Audio sample word [3:0] Preamble code 4'b0001 Subframe 1/start of audio block 4'b0010 Subframe 1 4'b0011 Subframe 2
AUDIO_OUT_tid	Output	3	Channel ID
AUDIO_OUT_tready	Input	1	Ready
AUDIO_OUT_tvalid	Output	1	Valid

Audio Clock Regeneration Interface

The audio clock regeneration (ACR) interface has a Cycle Time Stamp (CTS) parameter vector and an Audio Clock Regeneration Value (N) parameter vector. Both vectors are 20 bits wide. The valid signal is driven High when the CTS and N parameters are stable. For more information, see Chapter 7 of the HDMI 1.4 specification [Ref 12].

The subsystem should set up the CTS and N parameters before asserting the valid signal.

Table 2-5 shows the Audio Clock Regeneration (ACR) interface signals. This interface runs at the `s_axis_audio_aclk` clock rate.

Table 2-5: Audio Clock Regeneration (ACR) Interface

Name	Direction	Width	Description
acr_cts	Output	20	CTS
acr_n	Output	20	N
acr_valid	Output	1	Valid

HDMI Link Input Interface

Table 2-6 shows the HDMI Link Input interface signals. This interface runs at the `link_clk` clock rate.

Table 2-6: HDMI Link Input Interface

Name	Direction	Width	Description
link_clk	Input	1	Link clock
LINK_DATA0_IN_tdata	Input	40	Link data 0
LINK_DATA0_IN_tvalid	Input	1	Link Data 0 Valid
LINK_DATA1_IN_tdata	Input	40	Link data 1
LINK_DATA1_IN_tvalid	Input	1	Link Data 1 Valid
LINK_DATA2_IN_tdata	Input	40	Link data 2
LINK_DATA2_IN_tvalid	Input	1	Link Data 2 Valid

Data Display Channel Interface

Table 2-7 shows the Data Display Channel interface signals.

Table 2-7: Data Display Channel (DDC) Interface

Name	Direction	Width	Description
ddc_scl_i	Input	1	DDC serial clock in
ddc_scl_o	Output	1	DDC serial clock out
ddc_scl_t	Output	1	DDC serial clock tri-state
ddc_sda_i	Input	1	DDC serial data in
ddc_sda_o	Output	1	DDC serial data out
ddc_sda_t	Output	1	DDC serial data tri-state

HDCP 1.4 Key Input Interface (AXI4-Stream Slave Interface)

Table 2-8 shows the signals for HDCP 1.4 key interface. This interface runs at the `hdcp14_key_aclk` (which is running at AXI4 Lite Clock).

Table 2-8: HDCP 1.4 Key Input Interface

Name	Direction	Width	Description
HDCP_KEY_IN_tdata	Input	64	HDCP 1.4 key data
HDCP_KEY_IN_tlast	Input	1	End of key data
HDCP_KEY_IN_tready	Output	1	Ready
HDCP_KEY_IN_tuser	Input	8	Start of key data
HDCP_KEY_IN_tvalid	Input	1	Valid
hdcp14_key_aclk	Output	1	AXI4-Stream clock
hdcp14_key_aresetn	Output	1	Reset (Active-Low)
hdcp14_start_key_transmit	Output	1	Start key transmit
hdcp14_reg_key_sel	Output	3	Key select

For the HDCP 1.4 receiver, an HDCP Key Management module is needed, which is able to send keys over the AXI4-Stream interface to the HDCP 1.4 controller. Figure 2-15 shows an example of how the HDMI RX Subsystem is connected to the HDCP Key Management module through a Key Management Bus (AXI4-Stream). The HDCP Key Management module is not part of the HDMI RX Subsystem. For HDCP 1.4 design details, see the *HDCP v1.4 Product Guide* (PG224) [Ref 25].

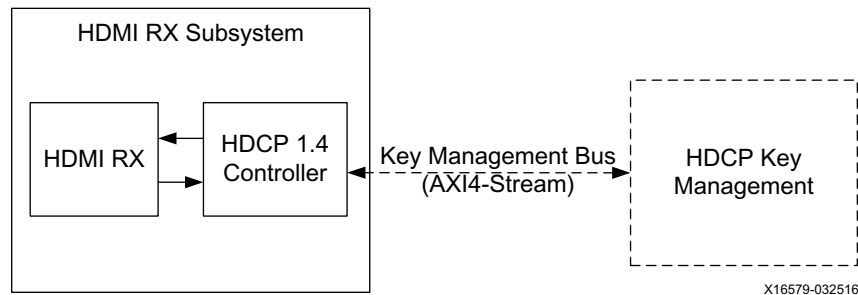


Figure 2-15: HDCP 1.4 Key Management Bus (AXI4-Stream)

However, the HDCP 2.2 key is handled slightly differently as it is solely controlled by the software application. The user application is responsible for providing the infrastructure to securely store and retrieve the keys to be loaded into the HDCP 2.2 drivers. For the detailed list of keys that are required to be loaded by the user application, see the *HDCP v2.2 Product Guide* (PG249) [Ref 24].

HDCP 2.2 Interrupt Outputs

Table 2-9 shows the signals for HDCP 2.2 interrupt output ports.

Table 2-9: HDCP 2.2 Interrupt Output Interface

Name	Direction	Width	Description
hdcp22_irq	Output	1	HDCP 2.2 interrupt
hdcp22_timer_irq	Output	1	HDCP 2.2 timer interrupt

Miscellaneous Signals with AXI4-Stream Video Interface

Table 2-10 shows the miscellaneous signals with AXI4-Stream video interface selected.

Table 2-10: Miscellaneous Signals with AXI4-Stream Video Interface

Name	Direction	Width	Description
hpd	Output	1	If XGUI option: Hot Plug Detect Active High (Default) 0 - Hot Plug Detect is released 1 - Hot Plug Detect is asserted If XGUI option: Hot Plug Detect Active Low ⁽¹⁾ 0 - Hot Plug Detect is asserted 1 - Hot Plug Detect is released
cable_detect	Input	1	If XGUI option: Cable Detect Active High (Default) 0 - Cable Detect is released 1 - Cable Detect is asserted If XGUI option: Cable Detect Active Low ⁽²⁾ 0 - Cable Detect is asserted 1 - Cable Detect is released
video_clk	Input	1	Reference Native Video Clock When AXI4-Stream is selected as Video Interface, a Video In to AXI4-Stream Bridge module is added to the HDMI RX Subsystem to convert Native Video into AXI4-Stream Video. HDMI RX core uses this video_clk to clock out the Video Data.
SB_STATUS_IN_tdata	Input	2	Side Band Status input signals Bit 0: link_rdy Bit 1: video_rdy
SB_STATUS_IN_tvalid	Input	1	Side Band Status input valid
fid	Output	1	Field ID for AXI4-Stream bus. Used only for interlaced video. 0 - even field 1 - odd field For progress video the output is always Low.

1. The Hot Plug Detect (HPD) signal is driven by an HDMI sink and asserted when the HDMI cable is connected to notify the HDMI source of the presence of an HDMI sink. When designing a HDMI sink system using HDMI Receiver Subsystem, in the PCB, if you choose to use a voltage level shifter, the HPD polarity remains as Active High. However, if you choose to add an inverter to the HPD signal, then the HPD polarity must be set to Active Low in HDMI Receiver Subsystem GUI. There are two common ways of using HPD: Toggle HPD to trigger HDCP authentication process (usually 100 ~ 500ms). Or a longer HPD toggle (>1s), the HDMI sink is notifying the source its present without cable unplug and plug. The software API used to assert and release HPD is XV_HdmiRxSs_SetHpd.
2. The Cable Detect signal is connected to a 5V power signal from the HDMI cable connector via some level shifter to notify the HDMI RX Subsystem that a HDMI source is connected.

Miscellaneous Signals with Native Video Interface

Table 2-11 shows the miscellaneous signals with native video interface selected.

Table 2-11: Miscellaneous Signals with Native Video Interface

Name	Direction	Width	Description
hpd	Input	1	If XGUI option: Hot Plug Detect Active High (Default) 0 - Hot Plug Detect is released 1 - Hot Plug Detect is asserted If XGUI option: Hot Plug Detect Active Low ⁽¹⁾ 0 - Hot Plug Detect is asserted 1 - Hot Plug Detect is released
cable_detect	Input	1	If XGUI option: Cable Detect Active High (Default) 0 - Cable Detect is released 1 - Cable Detect is asserted If XGUI option: Cable Detect Active Low ⁽²⁾ 0 - Cable Detect is asserted 1 - Cable Detect is released
irq	Output	1	Interrupt request for CPU. Active-High.
SB_STATUS_IN_tdata	Input	2	Side Band Status input signals Bit 0: link_rdy Bit 1: video_rdy
SB_STATUS_IN_tvalid	Input	1	Side Band Status input valid
video_rst	Output	1	Video reset signal in video_clk domain. Active-High.

1. The Hot Plug Detect (HPD) signal is driven by an HDMI sink and asserted when the HDMI cable is connected to notify the HDMI source of the presence of an HDMI sink. In most cases, the HDMI sink is simply connected to 5V power signal. Therefore, in the PCB, if you choose to use a voltage divider or level shifter, the HPD polarity remains as Active High. However, if you add an inverter to the HPD signal, then the HPD polarity must be set to Active Low in HDMI Transmitter Subsystem GUI. When designing a HDMI sink system using HDMI Receiver Subsystem, in the PCB, if you choose to use a voltage level shifter, the HPD polarity remains as Active High. However, if you choose to add an inverter to the HPD signal, then the HPD polarity must be set to Active Low in HDMI Receiver Subsystem GUI. There are two common ways of using HPD: Toggle HPD to trigger HDCP authentication process (usually 100 ~ 500ms). Or a longer HPD toggle (>1s), the HDMI sink is notifying the source its present without cable unplug and plug. The software API used to assert and release HPD is XV_HdmiRxSs_SetHpd.
2. The Cable Detect signal is connected to a 5V power signal from the HDMI cable connector via some level shifter to notify the HDMI RX Subsystem that a HDMI source is connected.

Clocks and Resets

Table 2-12 provides an overview of the clocks and resets. See [Clocking](#) and [Resets in Chapter 3](#) for more information.

Table 2-12: Clocks and Resets

Name	Direction	Width	Description
s_axi_cpu_aclk	Input	1	AXI4-Lite CPU control interface clock.
s_axi_cpu_aresetn	Input	1	Reset, associated with s_axi_cpu_aclk (active-Low). The s_axi_cpu_aresetn signal resets the entire subsystem including the data path and AXI4-Lite registers.
s_axis_video_aclk	Input	1	AXI4-Stream video output clock.
s_axis_video_aresetn	Input	1	Reset, associated with s_axis_video_aclk (active-Low). Resets the AXI4-Stream data path for the video output.
s_axis_audio_aclk	Input	1	AXI4-Stream Audio output clock. (The audio streaming clock must be greater than or equal to 128 times the audio sample frequency)
s_axis_audio_aresetn	Input	1	Reset, associated with s_axis_audio_aclk (active-Low). Resets the AXI4-Stream data path for the audio output.
link_clk	Input	1	HDMI Link data input clock. This connects to the Video PHY Controller Link clock output.
video_clk	Input	1	Clock for the native video interface.

Notes:

1. The reset should be asserted until the associated clock becomes stable.

Designing with the Subsystem

This chapter includes guidelines and additional information to facilitate designing with the subsystem.

General Design Guidelines

The subsystem connects to other hardware components to construct a complete HDMI RX system. These hardware components usually are different from device to device. For example, Kintex®-7 devices have a different PLL architecture from UltraScale™ devices. Therefore, you need to fully understand the system and adjust the subsystem parameters accordingly. [Appendix C, Application Software Development](#) describes how to integrate the subsystem API into a software application.

Audio Data Stream

An AXI4-Stream audio cycle is illustrated in [Figure 3-1](#). The data is valid when both the valid (TVLD) and ready (TRDY) signals are asserted. The HDMI 1.4/2.0 Receiver Subsystem sends out adjacent channels in sequential order (CH0, CH1, etc). Usually, the audio stream receiver also expects the channels in sequential order. If the channel data is not in order, the channel data might be mapped into other channel sample slots.

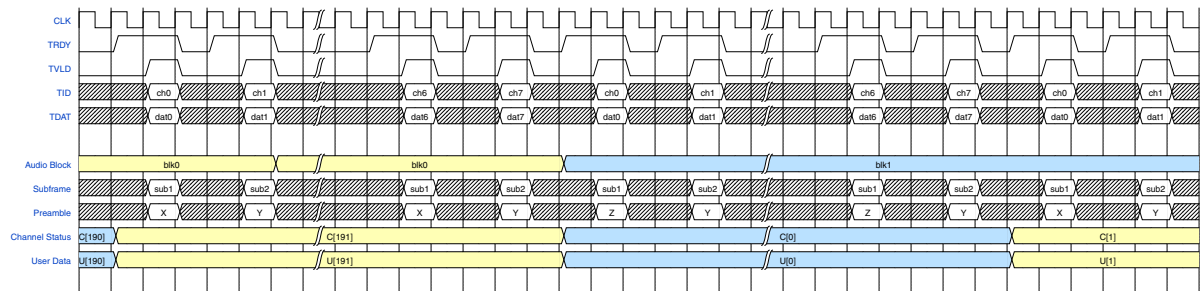


Figure 3-1: Audio Cycle

In HDMI 1.4/2.0 Receiver Subsystem, the number of Audio Channels is set through the software driver. You must enable the correct number of audio channel according to your use case and send the corresponding audio channel data mapping to the channel ID (TID). For example, if you intend to send out 8 channel audio, then you must set Audio Channel number to 8 in HDMI 1.4/2.0 Receiver Subsystem driver. Then, the corresponding audio

data must be prepared and sent to HDMI 1.4/2.0 Receiver Subsystem in the hardware, as described in [Figure 3-1](#).

If an HDMI system does not require audio, tie all audio related input ports to LOW. The ports are:

- s_axis_audio_aresetn
- s_axis_audio_aclk
- AUDIO_OUT_tready

Audio related output can be left unconnected. The ports are:

- AUDIO_OUT (except tready)
- acr_cts
- acr_n
- acr_valid

In HDMI RX Subsystem, L-PCM (IEC 60958, Packet Type 0x02) and HBR (Packet Type 0x09) are handled by the hardware. For Aux packet with packet type = 0x02, the audio data are routed to the audio interface. Therefore, even IEC 61937 compressed audio is available at the audio interface. In this case, you must develop your module to retrieve and uncompress the audio.

Video Output Stream Interface

The AXI4-Stream video interface supports dual or quad pixels per clock with 8 bits, 10 bits, 12 bits and 16 bits per component for RGB, YUV444, and YUV420 color spaces. The color depth in YUV422 color space is always 12-bits per pixel.

When the parameter, **Max Bits Per Component**, is set to 16, [Figure 3-2](#) shows the data format for quad pixels per clock to be fully compliant with the AXI4-Stream video protocol. A data format for a fully compliant AXI4-Stream video protocol dual pixels per clock is illustrated in [Figure 3-3](#).

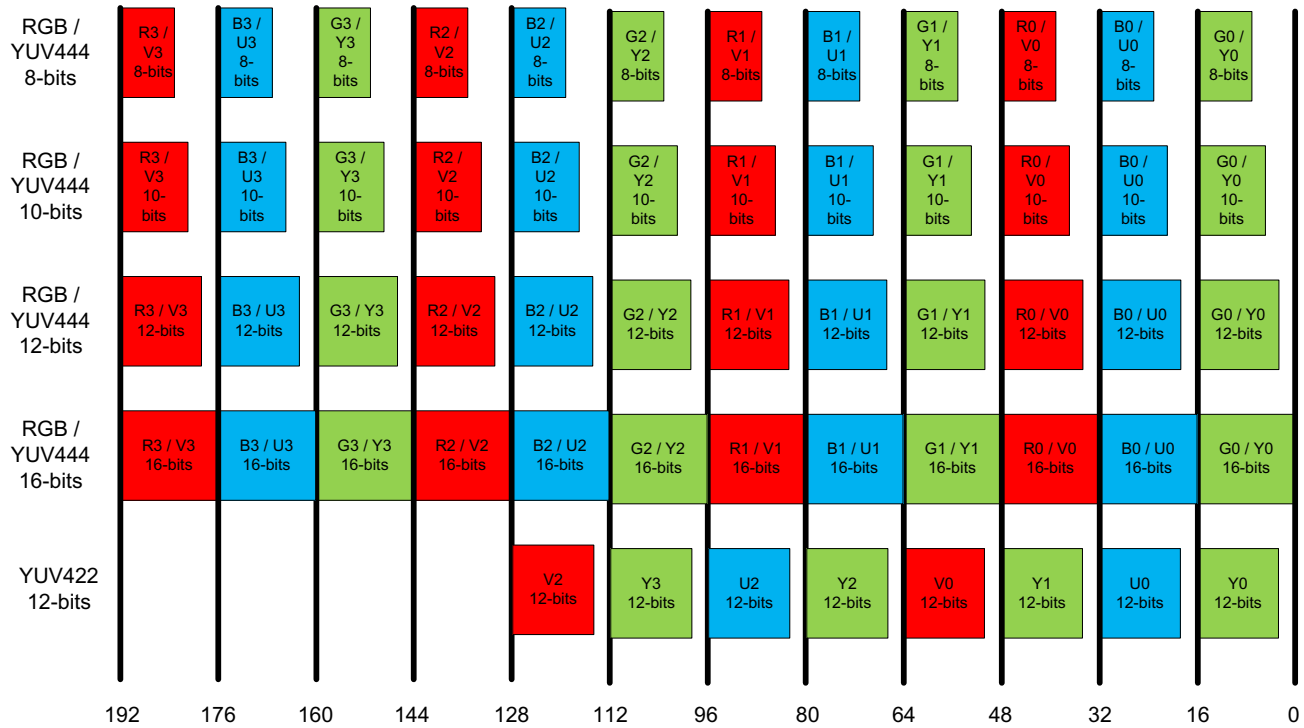
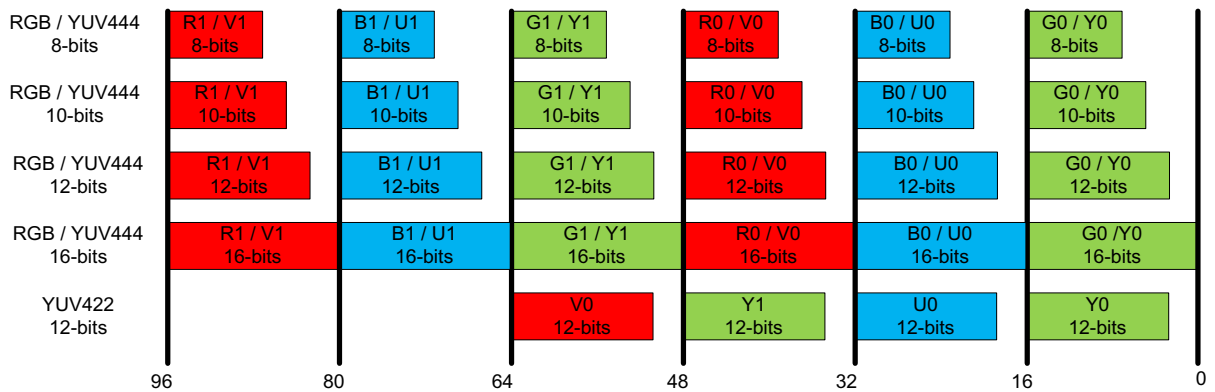


Figure 3-2: Quad Pixels Data Format (Max Bits Per Component = 16)



X15245-111615

Figure 3-3: Dual Pixels Data Format (Max Bits Per Component = 16)

When the parameter, **Max Bits Per Component**, is set to 12, video formats with actual bits per component larger than 12 is truncated to the Max Bits Per Component. The remaining least significant bits are discarded. If the actual bits per component is smaller than Max Bits Per Component set in the Vivado IDE, all bits are transported with the MSB aligned and the remaining LSB bits are padded with 0. This applies to all **Max Bits Per Component** settings.

Table 3-1: Max Bits Per Component Support

Max Bits Per Component	Actual Bits Per Component	Bits Transported by Hardware
16	8	[7:0]
	10	[9:0]
	12	[11:0]
	16	[15:0]
12	8	[7:0]
	10	[9:0]
	12	[11:0]
	16	[15:4]
10	8	[7:0]
	10	[9:0]
	12	[11:2]
	16	[15:6]
8	8	[7:0]
	10	[9:2]
	12	[11:4]
	16	[15:8]

As an illustration, when **Max Bits Per Component** is set to 12, [Figure 3-4](#) shows the data format for quad pixels per clock to be fully compliant with the AXI4-Stream video protocol. A data format for a fully compliant AXI4-Stream video protocol with dual pixels per clock is illustrated in [Figure 3-5](#).

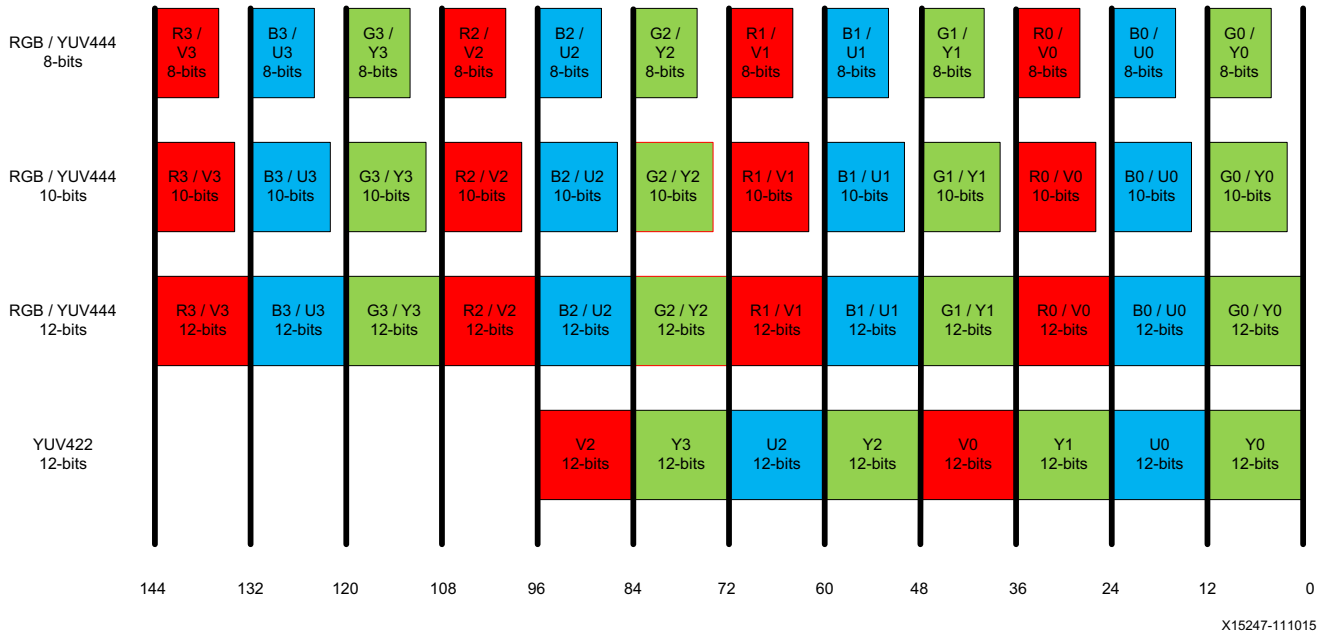


Figure 3-4: Quad Pixels Data Format (Max Bits Per Component = 12)

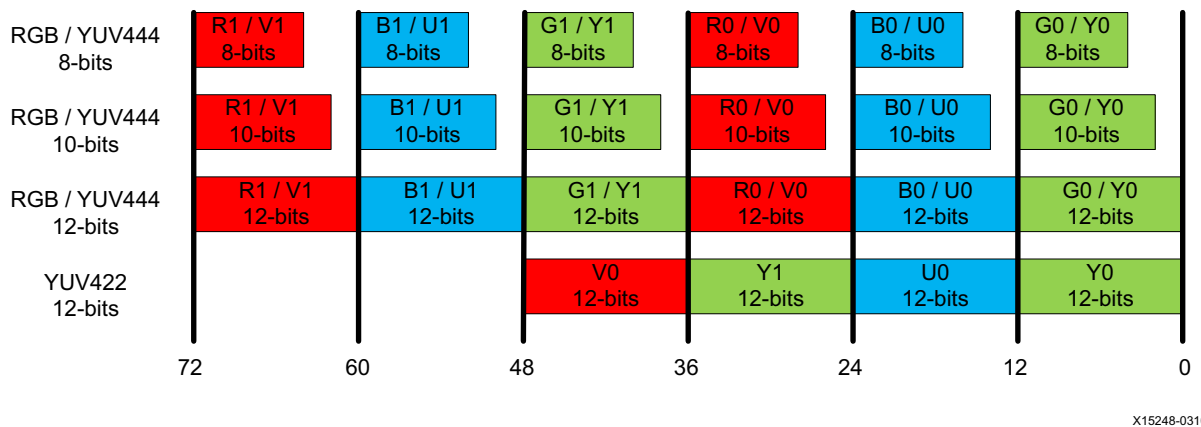


Figure 3-5: Dual Pixels Data Format (Max Bits Per Component = 12)

The video interface can also transport quad and dual pixels in the YUV420 color space. However the current data format is not compliant with the AXI4-Stream video protocol. Figure 3-6 and Figure 3-7 show the data format for quad and dual pixels formats.

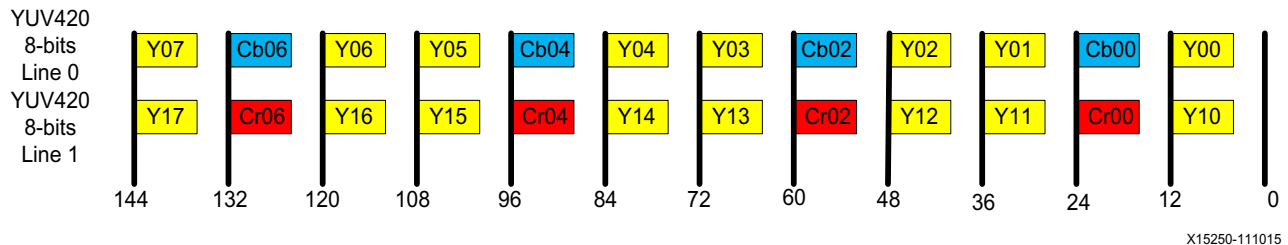


Figure 3-6: YUV420 Color Space Quad Pixels Data Format

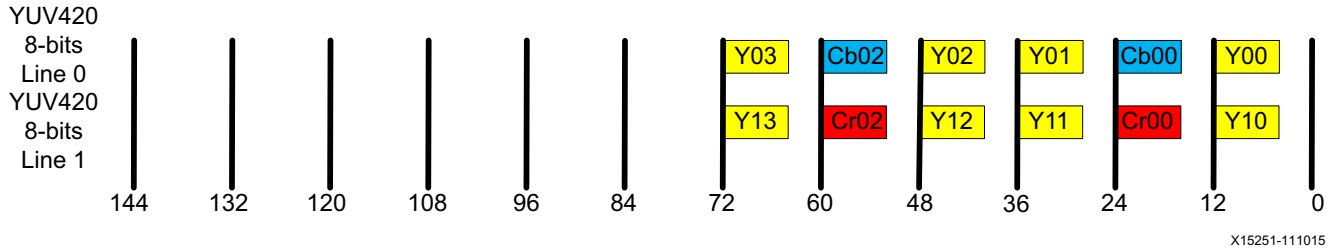


Figure 3-7: YUV420 Color Space Dual Pixels Data Format

Similarly, for YUV 4:2:0 deep color (10, 12, or 16 bits), the data representation is the same as shown in Figure 3-6 and Figure 3-7. The only difference is that each component carries more bits (10, 12, and 16). To make the YUV 4:2:0 compatible with AXI4-Stream Video IP and System Design Guide [Ref 14], enable it from the HDMI Receiver Subsystem GUI.

Using an 8-bit video as an example, Figure 3-8 illustrates the YUV 4:2:0 AXI4-Stream video data representation in AXI4-Stream Video IP and System Design Guide [Ref 14].

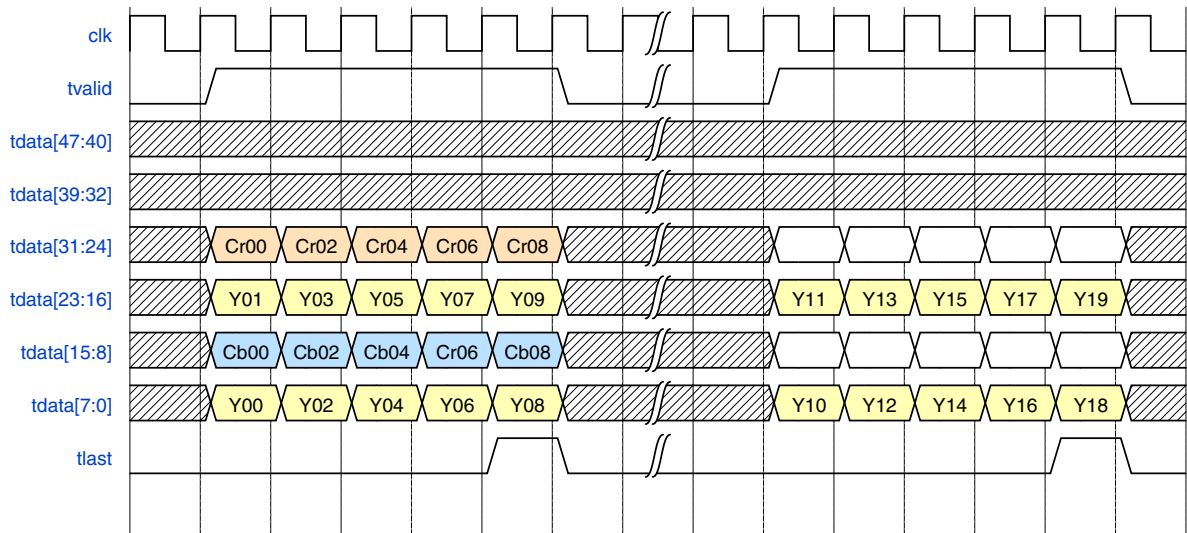


Figure 3-8: YUV 4:2:0 AXI4-Stream Video Data (Dual Pixel per Clock)

However, in the native HDMI video interface, the video data representation must be as shown in Figure 3-9.

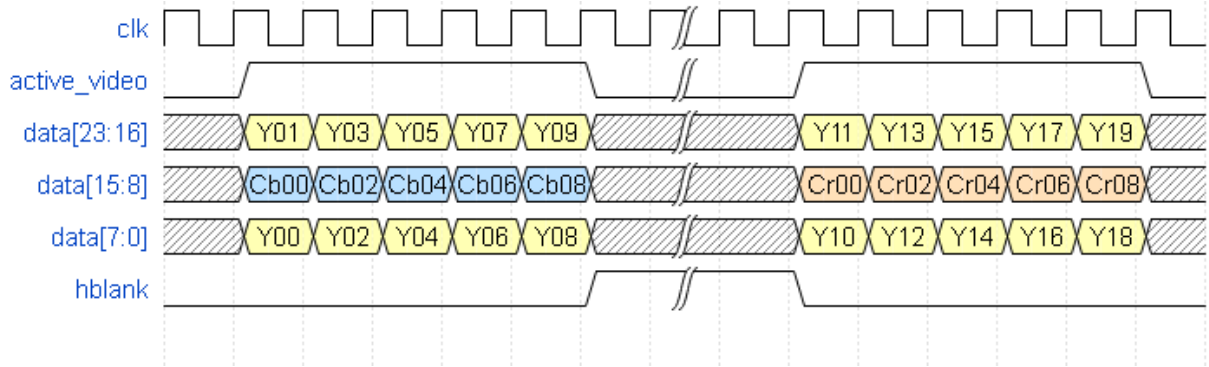


Figure 3-9: Native HDMI Video Interface

Therefore, a remapping feature is added to HDMI 1.4/2.0 Receiver Subsystem to convert AXI4-Stream video into HDMI native video.

Note: For RGB/YUV444/YUV422, Video data are directly mapped from AXI4 Stream to Native Video interface without any line buffer. Therefore, Figure 3-2 to Figure 3-5 are common to represent data interface for both AXI4 Stream and Native Video. The control signals are omitted in the figures.

The subsystem provides full flexibility to construct a system using the configuration parameters, maximum bits per component and number of pixels per clock. Set these parameters so that the video clock and link clock are supported by the targeted device. For example, when dual pixels per clock is selected, the AXI4-Stream video need to run at higher clock rate comparing with quad pixels per clock design. In this case, it is more difficult for the system to meeting timing requirements. Therefore the quad pixels per clock data mapping is recommended for design intended to send higher video resolutions.

Some video resolutions (for example, 720p60) have horizontal timing parameters (1650) which are not a multiple of 4. In this case the dual pixels per clock data mapping must be chosen.

For more information on the video AXI4-Stream interface and video data format, see the *AXI4-Stream Video IP and System Design Guide* (UG934) [Ref 14].

Clocking

The `S_AXI_CPU_IN`, `VIDEO_OUT`, and `AUDIO_OUT` can be run at their own clock rate. The HDMI link interfaces and native video interface also run at their own clock rate. Therefore, five separate clock interfaces are provided called `s_axi_cpu_aclk`, `s_axis_video_aclk`, `s_axis_audio_aclk`, `link_clk`, and `video_clk` respectively.

The audio streaming clock must be greater than or equal to 128 times the audio sample frequency. Because audio clock regeneration is not part of the HDMI RX subsystem, you must provide an audio clock to the application. This can be achieved by using an internal PLL or external clock source.



IMPORTANT: The AXI4-Lite CPU clock may run at different rates although all tests were conducted with the CPU clock running at 100 Mhz only.

The HDMI clock structure is illustrated in Figure 3-10 and Table 3-2.

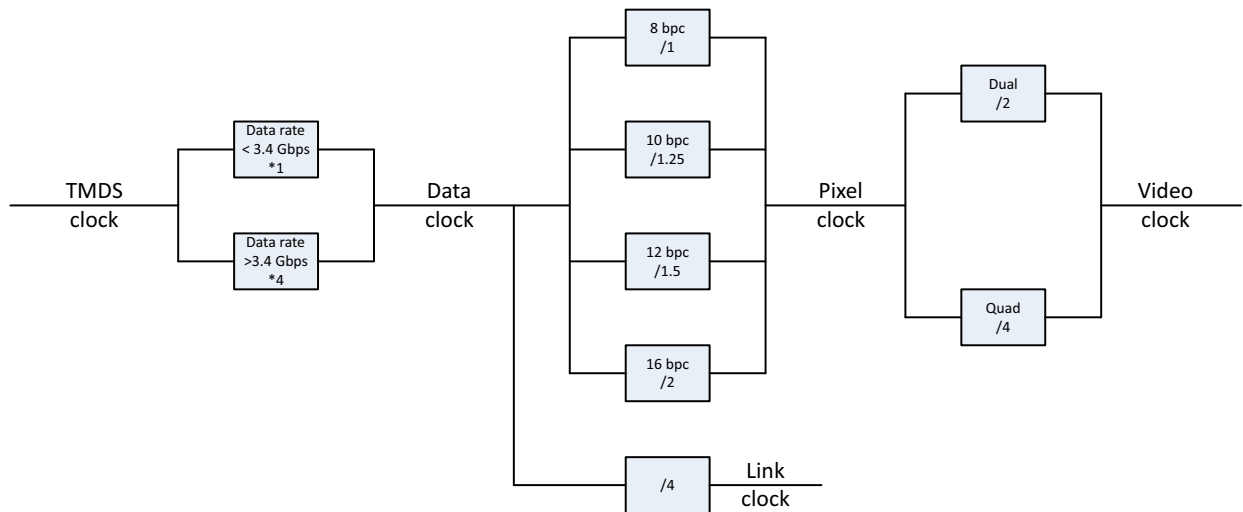


Figure 3-10: HDMI Clocking Structure

Table 3-2: Clocking

HDMI Clocking			
Clock	Function	Freq/Rate	Example ⁽¹⁾
TMDS clock	Source synchronous clock to HDMI interface (This is the actual clock on the HDMI cable).	$= 1/10$ data rate (for data rates < 3.4 Gb/s) $= 1/40$ data rate (for data rates > 3.4 Gb/s)	Data rate = 2.97 Gb/s TMDS clock = $2.97/10 = 297$ MHz Data rate = 5.94 Gb/s TMDS clock = $5.94/40 = 148.5$ MHz
Data clock	This is the actual data rate clock. This clock is not used in the system. It is only listed to illustrate the clock relations.	$=$ TMDS clock (for data rates < 3.4 Gb/s) $=$ TMDS clock * 4 (for data rates > 3.4 Gb/s)	Data rate = 2.97 Gb/s Data clock = TMDS clock * 1 = 297 MHz Data rate = 5.94 Gb/s Data clock = TMDS clock * 4 = 594 MHz TMDS clock = 148.5 MHz
Link clock	Clock used for data interface between HDMI PHY Layer Module and subsystem	$= 1/4$ of data clock	TMDS clock = 297 MHz Data clock = 297 MHz Link clock = $297 \text{ MHz}/4 = 74.25$ MHz Data clock = 594 MHz Link clock = $594 \text{ MHz}/4 = 148.5$ MHz

Table 3-2: Clocking (Cont'd)

HDMI Clocking			
Clock	Function	Freq/Rate	Example ⁽¹⁾
Pixel clock	This is the internal pixel clock. This clock is not used in the system. It is only listed to illustrate the clock relations.	for 8 bpc pixel clock = data clock for 10 bpc pixel clock = data clock/1.25 for 12 bpc pixel clock = data clock/1.5 for 16 bpc pixel clock = data clock/2	
Video clock	Clock used for video interface	for dual pixel video clock = pixel clock/2 for quad pixel video clock = pixel clock/4	297 MHz/2 = 148.5 MHz for dual pixel wide interface 297 MHz/4 = 74.25 MHz for quad pixel wide interface For more information on how to choose the correct PLL in the targeted devices, see the <i>Video PHY Controller LogiCORE IP Product Guide</i> (PG230) [Ref 23].

Notes:

- The examples in the Example column are only for reference and do not cover all the possible resolutions. Each GT has its own hardware requirements and limitations. Therefore, to use the HDMI 1.4/2.0 Receiver Subsystem with different GT devices, calculate the clock frequencies and make sure the targeted device is able to support it. When using the HDMI 1.4/2.0 Receiver Subsystem with Xilinx Video PHY Controller IP core, more information can be found in *Video PHY Controller LogiCORE IP Product Guide* (PG230) [Ref 23].

For example, 1080p60, 12BPC, and 2PPC are used to show how all the clocks are derived.

Video Resolution	Horizontal Total	Horizontal Active	Vertical Total	Vertical Active	Frame Rate (Hz)
1080p60	2200	1920	1125	1080	60

Pixel clock represents the total number of pixels need to be sent every second. Therefore,

$$\begin{aligned}
 \text{Pixel clock} &= H_{\text{total}} \times V_{\text{total}} \times \text{Frame Rate} \\
 &= 2200 \times 1125 \times 60 \\
 &= 148,500,000 \\
 &= 148.5\text{Mhz}
 \end{aligned}$$

$$\text{Link clock} = (\text{Data clock})/4 = 222.75/4 = 55.6875\text{Mhz}$$

$$\text{Video clock} = (\text{Pixel clock})/\text{PPC} = 148.5/2 = 74.25\text{Mhz}$$

$$\text{Data clock} = \text{Pixel clock} \times \text{BPC}/8 = 148.5 \times 12/8 = 222.75\text{Mhz}$$

Using the associative property in this example,

Data clock = 222.75Mhz < 340Mhz

then

TMDS clock = Data clock = 222.75Mhz

Figure 3-11 shows how the clock is distributed in HDMI RX Subsystem and the relationship to the Video PHY Controller.

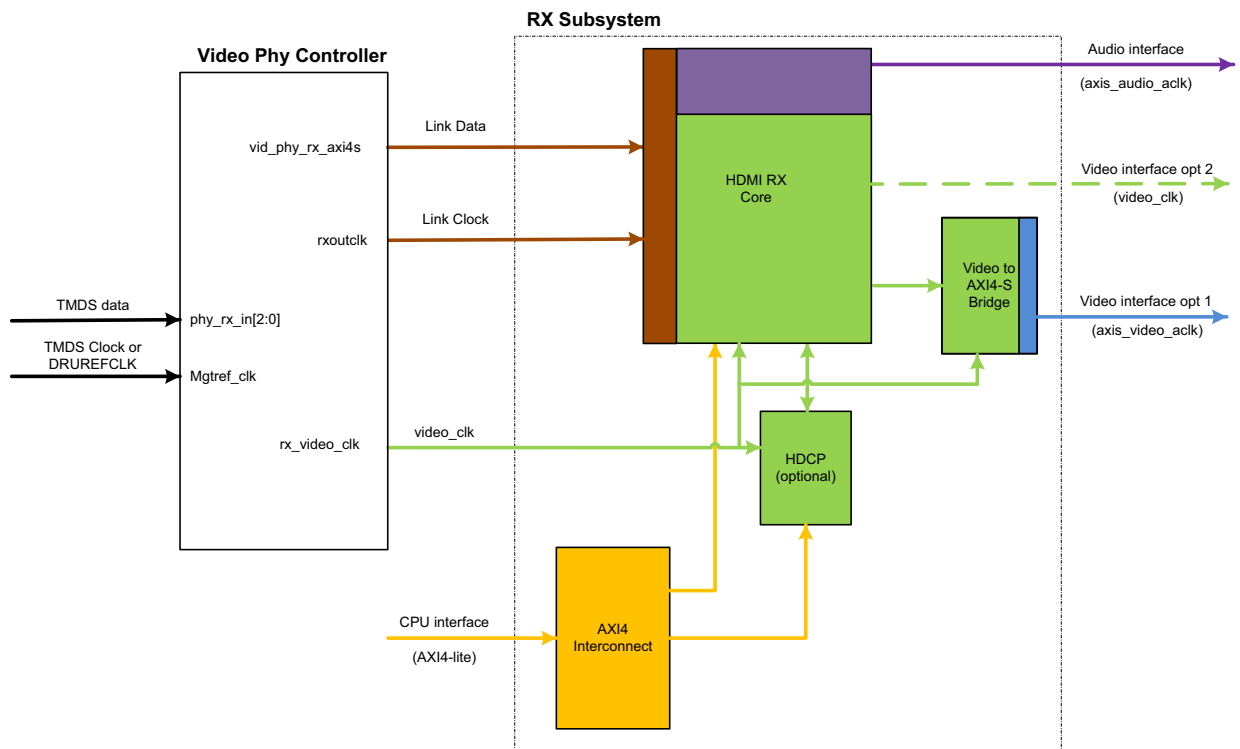


Figure 3-11: HDMI Receiver Subsystem and Video PHY Controller

The HDMI RX Subsystem is able to support either AXI4-Stream Video or Native Video.

Video PHY Controller converts serial TMDS data into parallel Link Data and sends to HDMI RX Subsystem at Link Clock. The HDMI RX core then unpack the Link data into native video stream, audio data and other auxiliary data.

- When **AXI4-Stream** is selected, a Video to AXI4_Stream Bridge core in HDMI RX Subsystem helps to convert the native video stream into AXI4-Stream, and then sent out from HDMI RX Subsystem at `axis_video_aclk`.
- When **Native Interface** is selected, native video stream is sent out from HDMI RX Subsystem directly from HDMI RX core at `video_clk`.

Based on the system requirement, Video PHY Controller is generating Link Clock and Video Clock for HDMI RX Subsystem for each targeted video resolution. Meanwhile, the `axis_audio_aclk`, `axis_video_aclk`, and AXI4-Lite clocks are free running clocks

in the system usually generated by clock wizard with reference to some on-board oscillators.

Resets

Each AXI input interface has its own reset signal. The reset signals, `s_axi_cpu_aresetn`, `s_axis_video_aresetn` and `s_axis_audio_aresetn` are for `S_AXI_CPU_IN`, `VIDEO_OUT` (AXI4-Stream Video Interface), and `AUDIO_OUT` respectively. These three reset signals are active-Low. Because the reset signal is used across multiple sub-blocks in the subsystem, keep the system in the reset state until all the clocks are stabilized. You can use the `locked` signal from the clock generation block as a reset signal.

Note: There is no dedicated hardware reset for `VIDEO_OUT` interface when Native Video interface is selected. However, HDMI RX Subsystem outputs a `video_rst` signal, which you can use to reset its supporting Native Video processing modules.

Design Flow Steps

This chapter describes customizing and generating the subsystem, constraining the subsystem, and the simulation, synthesis and implementation steps that are specific to this IP subsystem. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 15]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 16]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 17]

Customizing and Generating the Subsystem

This section includes information about using Xilinx tools to customize and generate the subsystem in the Vivado Design Suite.

The HDMI 1.4/2.0 Receiver Subsystem can be added to a Vivado IP integrator block design in the Vivado Design Suite and can be customized using IP catalog. For more detailed information on customizing and generating the subsystem in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 15]. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl Console.

You can customize the subsystem for use in your design by specifying values for the various parameters associated with the IP subsystem using the following steps:

1. In the **Flow Navigator**, click on **Create Block Diagram** or **Open Block Design** under the IP Integrator heading.
2. Right click in the diagram and select **Add IP**.

A searchable IP catalog opens. You can also add IP by clicking on the Add IP button on the left side of the IP Integrator Block Design canvas.

3. Click on the IP name and press the Enter key on your keyboard or double click on the IP name.
4. Double-click the selected IP block or select the **Customize Block** command from the right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 16] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 17].

Note: Figures in this chapter are illustrations of the Vivado Integrated Design Environment (IDE). The layout depicted here might vary from the current version.

Top Level Tab

The Top level tab is shown in Figure 4-1.

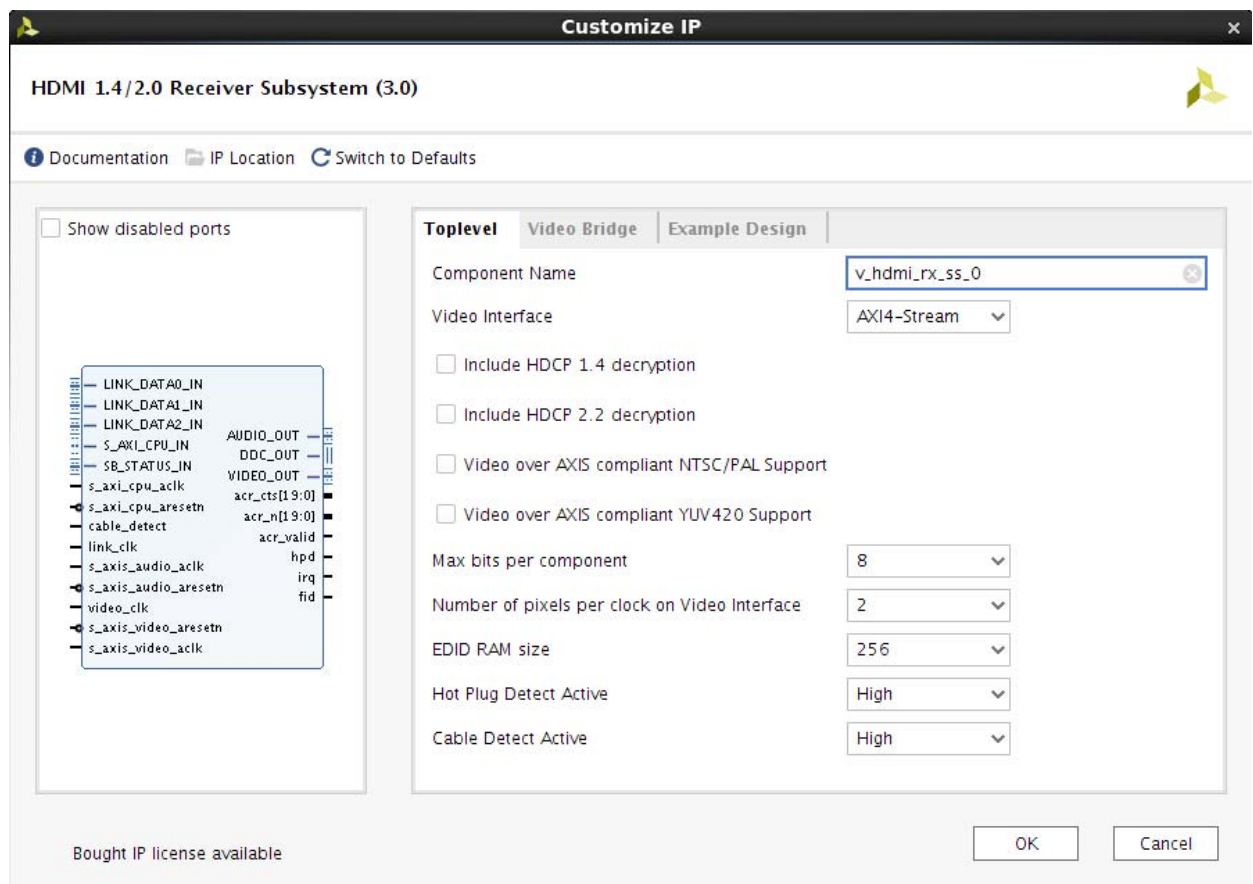


Figure 4-1: Toplevel Tab

The parameters on the Top level tab are as follows:

Component Name: The component name is set automatically by IP Integrator.

Video Interface: This option selects the Video Interface for the HDMI RX subsystem. The allowable options are **AXI4-Stream** or **Native Video**.

Include HDCP 1.4 Decryption: This option enables HDCP 1.4 decryption.

Include HDCP 2.2 Decryption: This option enables HDCP 2.2 decryption.

Note: HDCP 1.4 and 2.2 decryption options are only configurable if you have a HDCP license.

Max bits per component: This option selects the maximum bits per component. The allowable options are, 8, 10, 12 or 16 bits. This parameter is to set the maximum “allowed” bits per component, and the actual bits per component can be set from the software API to a different value. However, the actual bits per component is bounded by the **Max bits per component**. For example, if the **Max bits per component** is set to 16, the user can set the actual bits per component from the software API to any of the values, 8, 10, 12 or 16. But if the **Max bits per component** is set to 8, you can only set the actual bits per component to 8 through the software API. For more information on bits mapping, see [Table 3-1](#).

Number of pixels per clock on Video Interface: This option selects the number of pixels per clock. The allowable options are 2 or 4 pixels.



IMPORTANT: *Pixels per clock (PPC) can only be selected at IP generation time, and must remain static in the design. Some video format with a total horizontal resolution that is NOT divisible by 4 (for example, 720p60 has a total horizontal pixel of 1650, which is not divisible by 4) are not supported. If the design is intended to support this kind of video formats, ensure that **PPC=2** is selected in Vivado.*

Video over AXIS compliant NTSC/PAL Support: This option enables the HDMI RX subsystem to support Video over AXIS compliant NTSC/PAL.

- A pixel repetition of 2 is supported by current hardware
- 480i60 and 576i50 resolutions are supported in current software.

Note: Pixel Repetition only supports RGB and YUV444 color space.

Video over AXIS compliant YUV420 Support: This option enables the HDMI RX subsystem to support Video over AXIS compliant YUV420.

Hot Plug Detect Active: This option selects the HPD active polarity. The allowable options are High or Low.

EDID RAM size: The allowable options are, 256, 512, 1024 or 4096.

Cable Detect Active: This option selects the Cable Detect active polarity. The allowable options are High or Low.

Video Bridge Tab (Video AXI4 Stream Interface Only)

The Video Bridge tab is shown in [Figure 4-2](#).

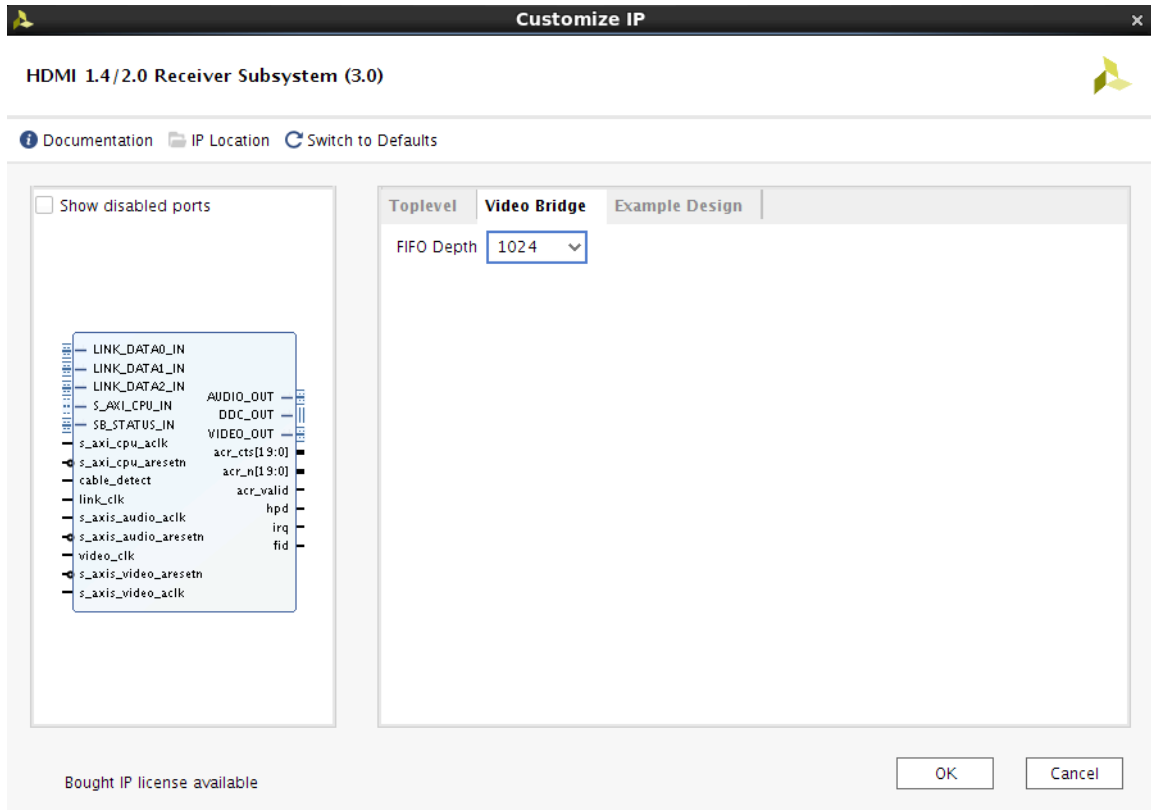


Figure 4-2: Video Bridge Tab

The parameter on the Video Bridge tab is as follows:

FIFO Depth: Specifies the number of locations in the input FIFO. The allowable values are 32, 1024, 2048, 4096, and 8192.

Example Design Tab

The Example Design tab is shown in Figure 4-3.

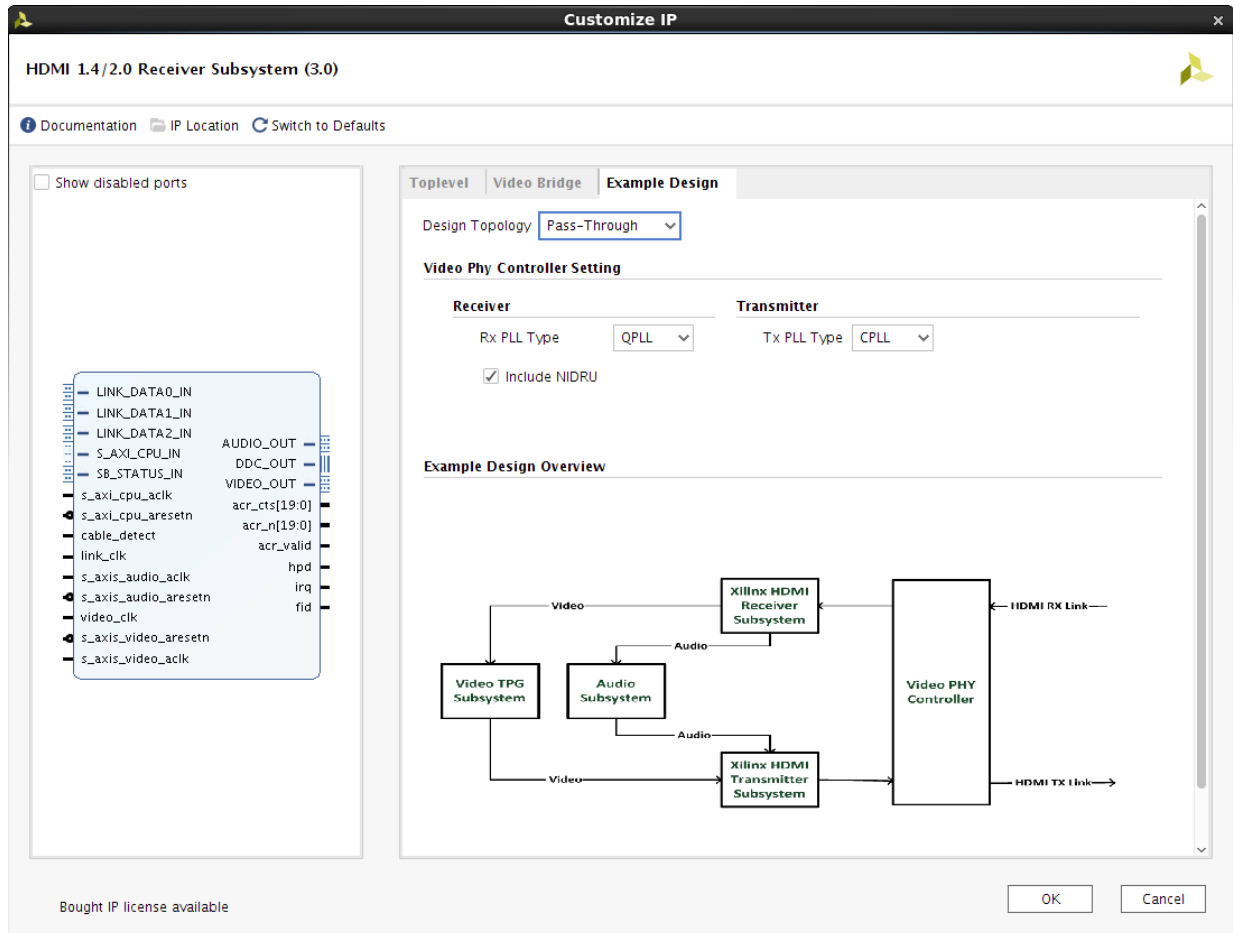


Figure 4-3: Example Design Tab (HDCP Not Included)

Design Topology: Allows you to choose the topology of example design to be generated. The allowable options are Pass-Through and Rx Only.

where,

- Pass-Through showcases the HDMI system built with one HDMI TX Subsystem and one HDMI RX Subsystem, sharing the same Video PHY Controller.
- Rx Only showcases the HDMI system built with only one HDMI RX Subsystem and Video PHY Controller. A Frame CRC helper core is added to the Rx Only topology to facilitate system monitor and debugging.

Video PHY Controller Setting Section: Allows the configuration of the Transmitter PLL type and Receiver PLL Type to the Video PHY Controller prior generating the example design. It also allows user to selectively opt-out the NI-DRU to optimize resource utilization

if the video resolution they plan to support doesn't require NI-DRU. Refer to *Video PHY Controller Product Guide* [Ref 23] for details about NI-DRU requirements.

Example Design Overview Section: A system block diagram to show the overview of the example design to be generated.

Native Video Interface Option

The native video interface option window is shown in [Figure 4-4](#).

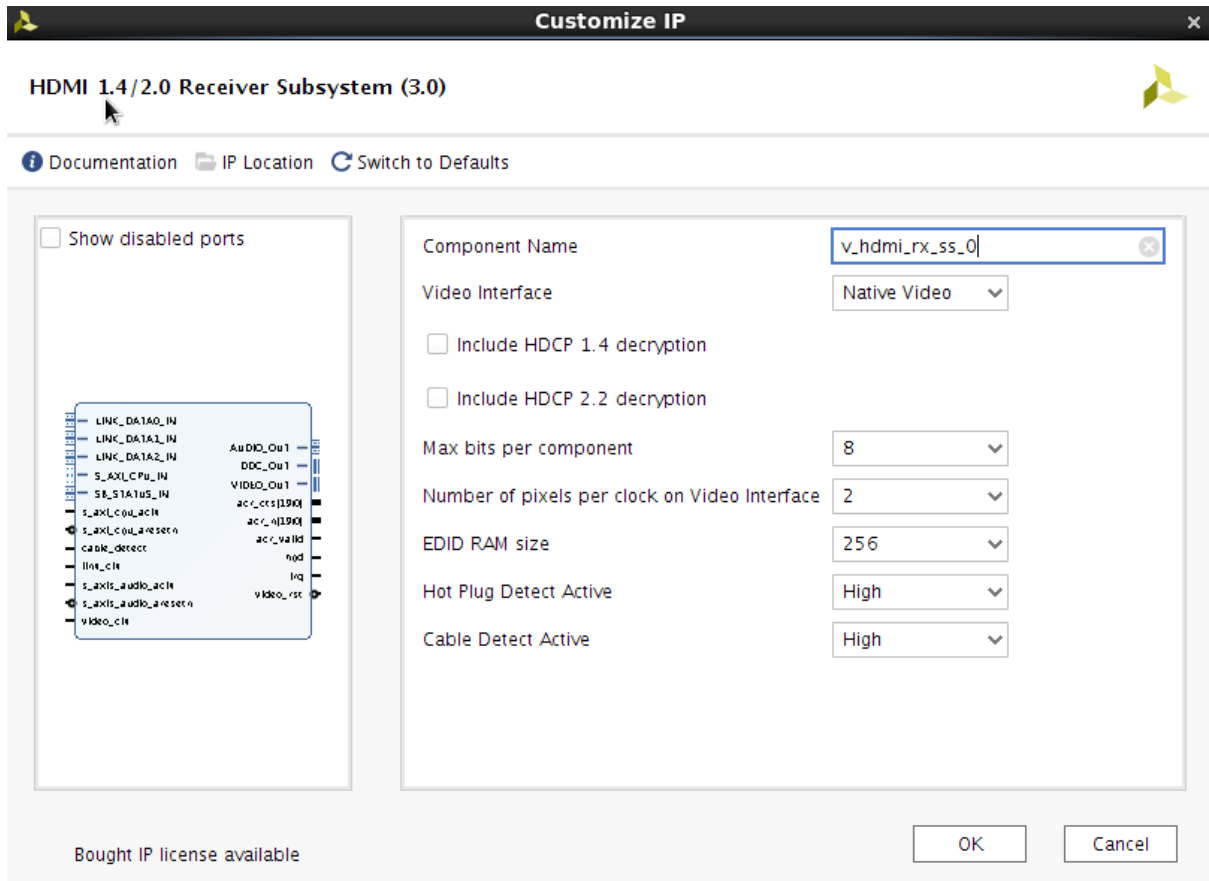


Figure 4-4: Native Video Interface Option

Include HDCP 1.4 Decryption: This option enables HDCP 1.4 decryption.

Include HDCP 2.2 Decryption: This option enables HDCP 2.2 decryption.

Note: HDCP 1.4 and 2.2 Decryption options are only configurable if you have a HDCP license, else it is disabled.



IMPORTANT: The Open Example Design is not supported for Native Video Interface. Therefore, the Example Design Tab is not available when Native Video is selected.

User Parameters

Table 4-1 shows the relationship between the fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl Console).

Table 4-1: Vivado IDE Parameter to User Parameter Relationship

Vivado IDE Parameter/Value	User Parameter/Value	Default Value
Toplevel		
Video Interface	C_VID_INTERFACE	AXI4-Stream
AXI4-Stream	0	
Native Video	1	
Include HDCP 1.4 Decryption	C_INCLUDE_HDCP_1_4	Exclude
Exclude (Untick)	FALSE	
Include (Tick)	TRUE	
Include HDCP 2.2 Decryption	C_INCLUDE_HDCP_2_2	Exclude
Exclude (Untick)	FALSE	
Include (Tick)	TRUE	
Video over AXIS compliant NTSC/PAL Support	C_INCLUDE_LOW_RESO_VID	Exclude
Exclude (Untick)	FALSE	
Include (Tick)	TRUE	
Video over AXIS compliant YUV420 Support	C_INCLUDE_YUV420_SUP	Exclude
Exclude (Untick)	FALSE	
Include (Tick)	TRUE	
Max bits per component	C_MAX_BITS_PER_COMPONENT	8
8	8	
10	10	
12	12	
16	16	
Number of pixels per clock on Video Interface	C_INPUT_PIXELS_PER_CLOCK	2
2	2	
4	4	
Hot Plug Detect Active	C_HPD_INVERT	High
High	High	
Low	Low	
Cable Detect Active	C_CD_INVERT	High
High	High	

Table 4-1: Vivado IDE Parameter to User Parameter Relationship (Cont'd)

Vivado IDE Parameter/Value	User Parameter/Value	Default Value
Low	Low	
EDID RAM Size	C_EDID_RAM_SIZE	256
256	256	
512	512	
1024	1024	
4096	4096	
Video Bridge		
FIFO Depth	C_ADDR_WIDTH	1024
32	32	
1024	1024	
2048	2048	
4096	4096	
8192	8192	
Example Design		
Design Topology	C_EXDES_TOPOLOGY	0
Pass-Through	0	
Rx Only	2	
TX PLL Type	C_EXDES_TX_PLL_SELECTION	0 (GTXE2) 6 (GTHE3/4)
CPLL	0	
QPLL(GTXE2)	3	
QPLL01(GTHE3/4)	6	
RX PLL Type	C_EXDES_RX_PLL_SELECTION	3 (GTXE2) 0 (GTHE3/4)
CPLL	0	
QPLL(GTXE2)	3	
QPLL01(GTHE3/4)	6	
Include NIDRU	C_EXDES_NIDRU	true
Include (Tick)	true	
Exclude (Untick)	false	

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 16].

Constraining the Subsystem

This section contains information about constraining the subsystem in the Vivado Design Suite.

Required Constraints

There are clock frequency constraints for the `s_axi_cpu_aclk`, `s_axis_video_aclk`, `s_axis_audio_aclk`, `link_clk`, and `video_clk`. For example,

```
create_clock -name s_axi_cpu_aclk -period 10.0 [get_ports s_axi_cpu_aclk]
create_clock -name s_axis_audio_aclk -period 10.0 [get_ports s_axis_audio_aclk]
create_clock -name link_clk -period 13.468 [get_ports link_clk]
create_clock -name video_clk -period 6.734 [get_ports video_clk]
create_clock -name s_axis_video_aclk -period 5.0 [get_ports s_axis_video_aclk]
```

When using this subsystem in the Vivado® Design Suite flow with Video PHY Controller modules, `link_clk` and `video_clk` are generated from the Video PHY Controller. Therefore, the clock constraints are set to the Video PHY Controller constraints instead of these generated clocks. See *Clocking* in the *Video PHY Controller LogiCORE™ IP Product Guide* (PG230) [Ref 23] for more information.

`s_axi_cpu_aclk`, `s_axis_video_aclk`, and `s_axis_audio_aclk` constraints are generated at system-level, for example by using a clock wizard.

Device, Package, and Speed Grade Selections

For more information on the device constraint/dependency, see the *Video PHY Controller LogiCORE IP Product Guide (PG230)* [Ref 23].

Table 4-2 shows the device and speed grade selections for HDMI 1.4/2.0 Receiver Subsystem.

Table 4-2: Device and Speed Grade Selections

Device Family	PPC	2				4			
	BPC	8	10	12	16	8	10	12	16
	Speed Grade								
Zynq-7000 AP SoC	-1	HDMI 1.4 ⁽²⁾				HDMI 1.4 ⁽¹⁾			
	-2	HDMI 2.0 ⁽¹⁾				HDMI 2.0 ⁽²⁾			
Zynq UltraScale+ MPSoC	-1	HDMI 2.0 ⁽²⁾				HDMI 2.0 ⁽²⁾			
	-2								
Artix-7	-1	HDMI 1.4 ⁽¹⁾				HDMI 1.4 ⁽¹⁾			
	-2	HDMI 1.4 ⁽¹⁾				HDMI 1.4 ⁽¹⁾			
Kintex-7	-1	HDMI 1.4 ⁽²⁾				HDMI 1.4 ⁽¹⁾			
	-2	HDMI 2.0 ⁽¹⁾				HDMI 2.0 ⁽²⁾			
Kintex UltraScale	-1	HDMI 2.0 ⁽²⁾				HDMI 2.0 ⁽²⁾			
	-2								
Virtex-7	-1	HDMI 1.4 ⁽²⁾				HDMI 2.0 ⁽²⁾	HDMI 1.4 ⁽¹⁾		
	-2	HDMI 2.0 ⁽¹⁾				HDMI 2.0 ⁽²⁾			
Virtex UltraScale	-1	HDMI 2.0 ⁽²⁾				HDMI 2.0 ⁽²⁾			
	-2								

Notes:

1. All HDMI 1.4 resolutions can be supported.
2. Full HDMI 2.0 resolutions support up to 4096 x 2160 @ 60fps.

Clock Frequencies

See [Clocking in Chapter 3](#) for more information.

Clock Management

This section is not applicable for this IP subsystem.

Clock Placement

This section is not applicable for this IP subsystem.

Banking

This section is not applicable for this IP subsystem.

Transceiver Placement

This section is not applicable for this IP subsystem.

I/O Standard and Placement

This section is not applicable for this IP subsystem.

Simulation

Simulation of the subsystem is not supported.

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 16].

Example Design

This chapter contains step-by-step instructions for generating an HDMI Example Design from the HDMI 1.4/2.0 Receiver Subsystem by using Vivado® Flow.

Summary

HDMI 1.4/2.0 Receiver Subsystem allows users to customize the example design based on their system requirements. It offers the full flexibility with the following system parameters:

Topology:

- RX-Only
- Pass-through

VPHY Configuration:

- NI-DRU Enable/Disable
- TXPLL Selection
- RXPLL Selection

Board:

- KC705
- KCU105
- ZC706
- ZCU102

Processor:

- MicroBlaze™
- A9
- A53
- R5

This chapter covers the design considerations of a High-Definition Multimedia Interface (HDMI™) 2.0 implementation using the performance features of these Xilinx® LogiCORE™ IPs:

- HDMI 1.4/2.0 with HDCP 1.4/2.2 Receiver Subsystem
- HDMI 1.4/2.0 with HDCP 1.4/2.2 Transmitter Subsystem (For Pass-through topology Only)
- Video PHY Controller

The design features the receive-only and the pass-through operation modes for the HDMI solution. In the pass-through mode, an external HDMI source is used to send video data over the HDMI design. In the receive-only mode, an external HDMI source is used to send video data, and the HDMI Example design receives and detects the video. You may check the video information from the UART menu. However, in receive-only mode, there won't be video available for visual check. The example design demonstrates the use of the High-bandwidth Digital Content Protection System (HDCP) Revision 1.4/2.2 capability of the HDMI solution. HDCP is used to securely send audiovisual data from an HDCP protected transmitter to HDCP protected downstream receivers. Typically, HDCP 2.2 is used to encrypt content at Ultra High Definition (UHD) while HDCP 1.4 is used as a legacy encryption scheme for lower resolutions.

The inrevium TB-FMCH-HDMI4K FMC daughter card is required for example designs targeting the following boards:

- Kintex®-7 FPGA Evaluation Kit (KC705)
- Kintex® UltraScale™ FPGA Evaluation Kit (KCU105)
- Zynq®-7000 All Programmable SoC evaluation board (ZC706)

And it is not required while targeting the following boards, instead the on-board HDMI 2.0 circuitry is used.

- ZCU102 Evaluation Board

Hardware

The example design is built around the HDMI 1.4/2.0 Transmitter Subsystem (HDMI_TX_SS) (Optional), HDMI 1.4/2.0 Receiver Subsystem (HDMI_RX_SS), Video PHY (VPHY) Controller core and leverages existing Xilinx IP cores to form the complete system. [Figure 5-1](#) and [Figure 5-2](#) are illustrations of Overall HDMI Example Design block diagram while targeting various Xilinx Evaluation Kits.

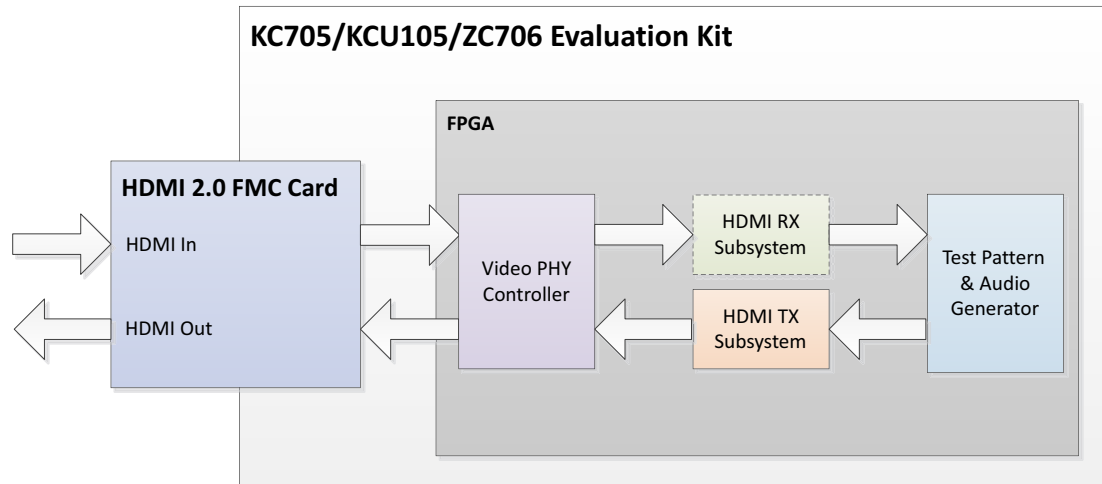


Figure 5-1: KC705/KCU105/ZC706 HDMI Example Design Block Diagram

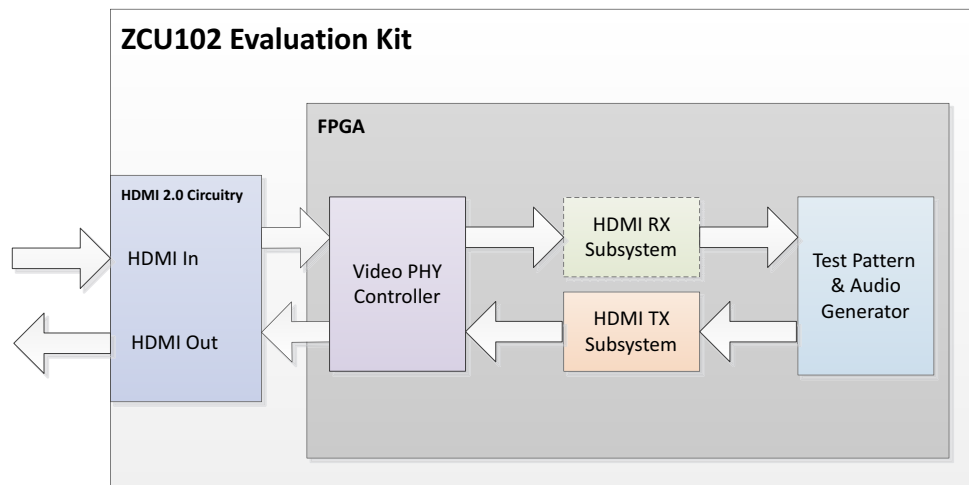


Figure 5-2: ZCU102/106 HDMI Example Design Block Diagram

Note: When an unpowered HDMI source is connected to the HDMI Receiver in a pass-through system, the HDMI Example Design UART may get flooded with Starting Colorbar message because of a limitation to the ZCU102 board design.

The VPHY Controller core has been configured for the HDMI application that allows transmission and reception (optional) of HDMI video/audio to and from the HDMI 2.0 daughter card or on-board HDMI 2.0 circuitry.

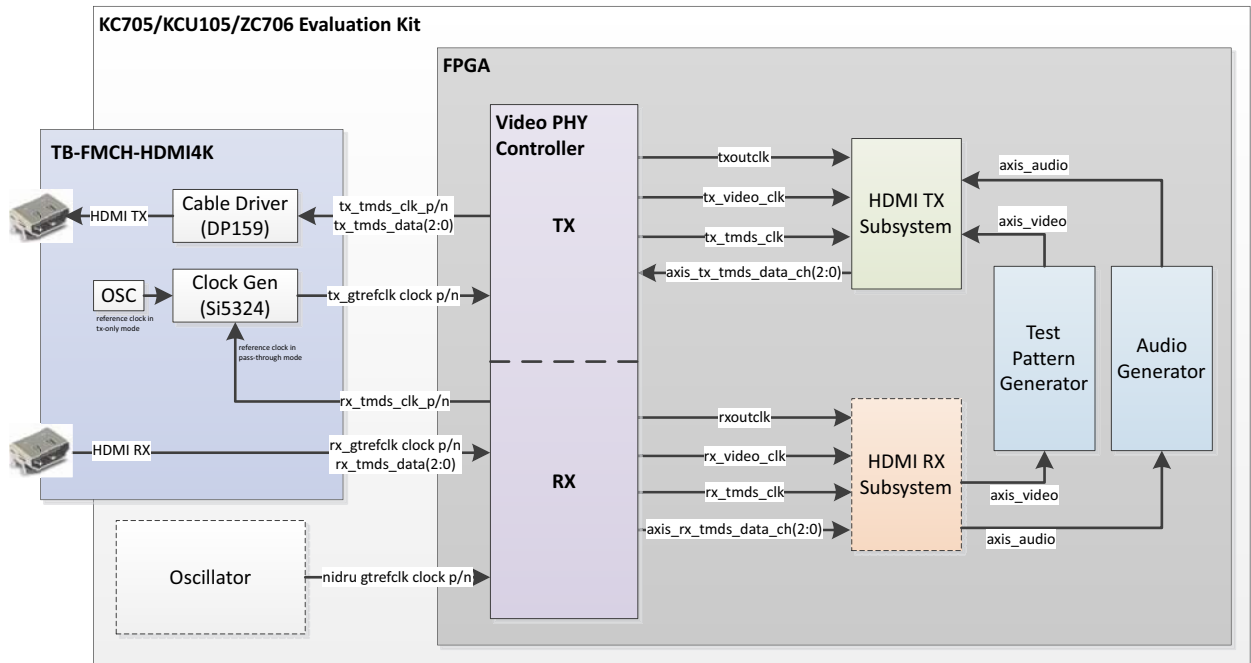


Figure 5-3: KC705/KCU105/ZC706 HDMI Reference Design Clock and Datapath Diagram

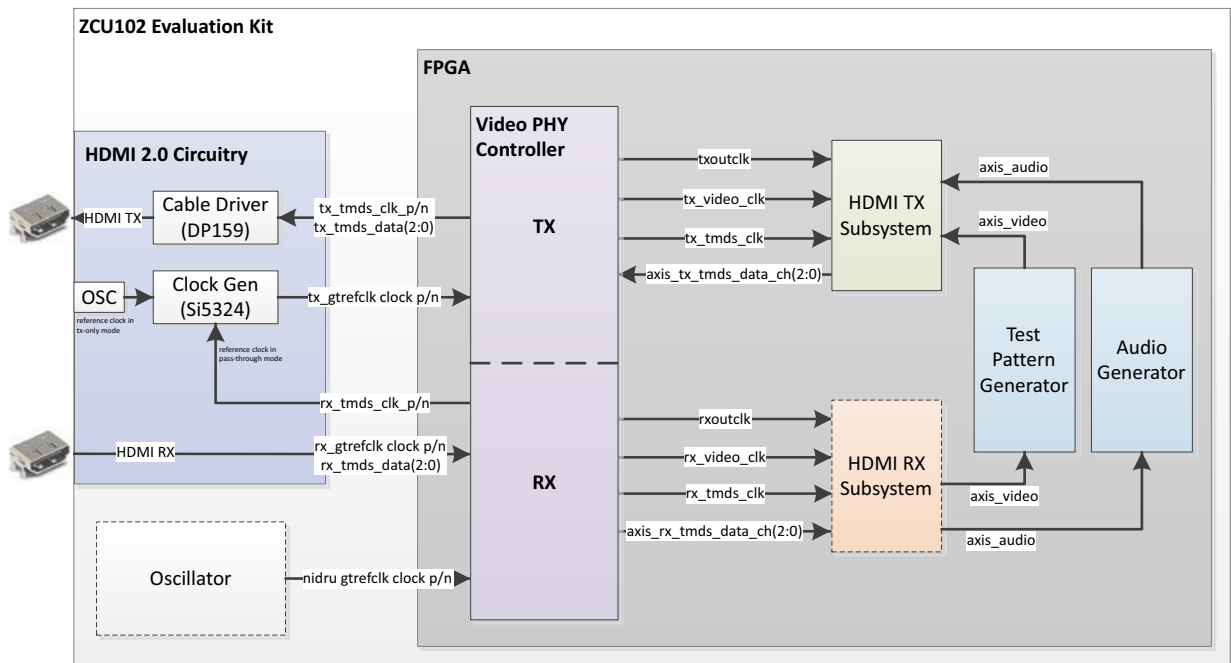


Figure 5-4: ZCU102 HDMI Reference Design Clock and Datapath Diagram

In pass-through mode, the VPHY Controller core recovers the high-speed serial video stream, converts it to parallel data streams, forwards it to the HDMI_RX_SS core, which extracts the video and audio streams from the HDMI stream and converts it to separate AXI video and audio streams. The AXI video goes through the TPG core and the AXI audio goes

through a customized audio generation block. The two AXI streams eventually reach the HDMI_TX_SS core, which converts the AXI video and audio streams back to an HDMI stream before being transmitted by the VPHY Controller core as a high-speed serial data stream. The transition minimized differential signaling (TMDS) clock from the HDMI In interface is forwarded to the HDMI TX transceiver via the SI53xx clock generator in the HDMI 2.0 FMC card or on-board HDMI 2.0 circuitry.

In the receive-only mode, an external HDMI source is used to send video data, and the HDMI Example design receives and detect the video. You can check the video information from the UART menu.

High-level control of the system is provided by a simplified embedded processor subsystem containing I/O peripherals and processor support IP. A clock generator block and a processor system reset block supply clock and reset signals for the system, respectively. See Figure 5-5 and Figure 5-6 for a block diagrams of the three types of processor subsystems supported by HDMI Example Design flow.

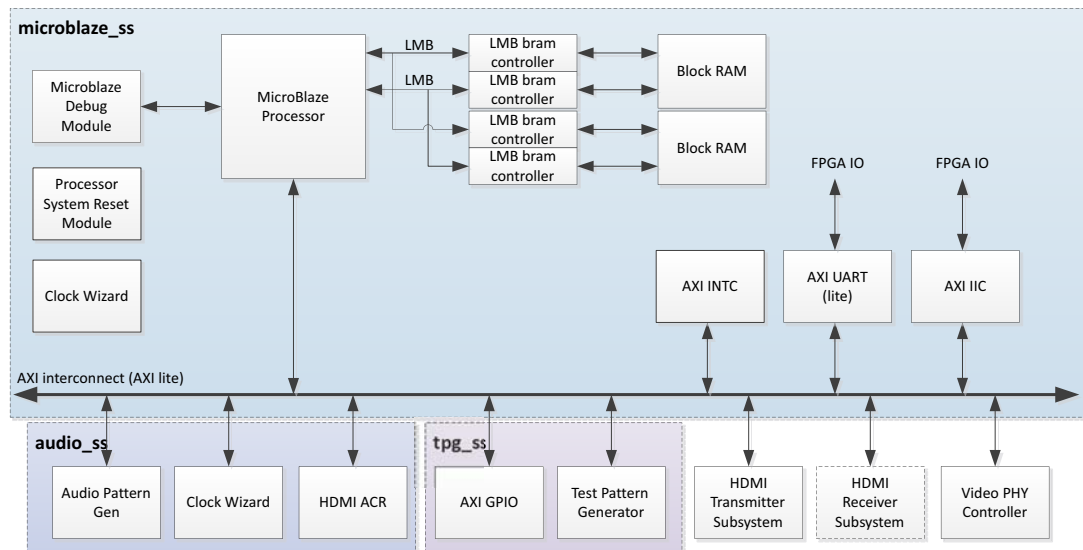


Figure 5-5: HDMI Reference Design Block Diagram (MicroBlaze)

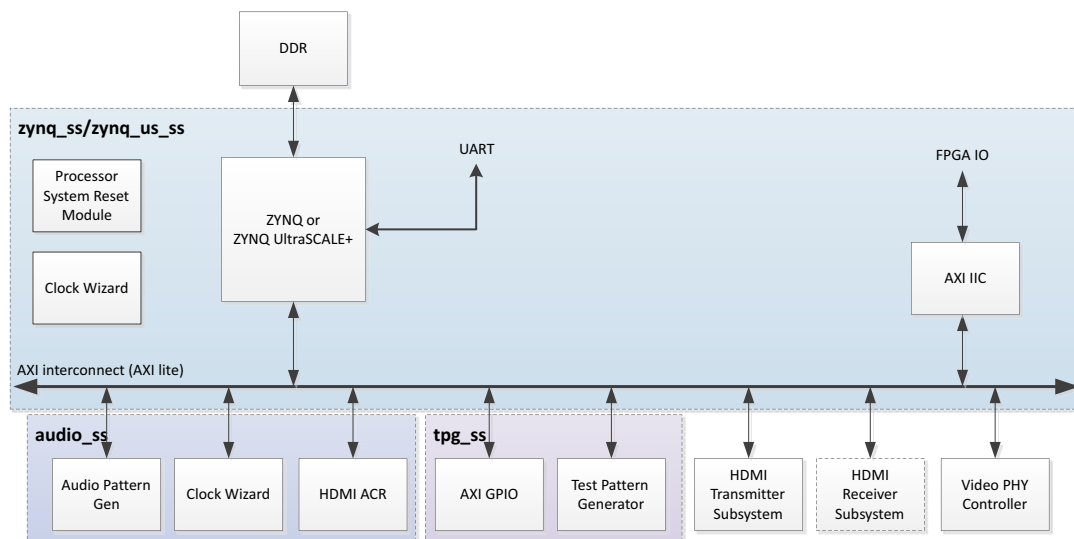


Figure 5-6: HDMI Reference Design Block Diagram (Zynq-7000 AP SoC or Zynq UltraScale+ MPSoC)

Example Design Specifics

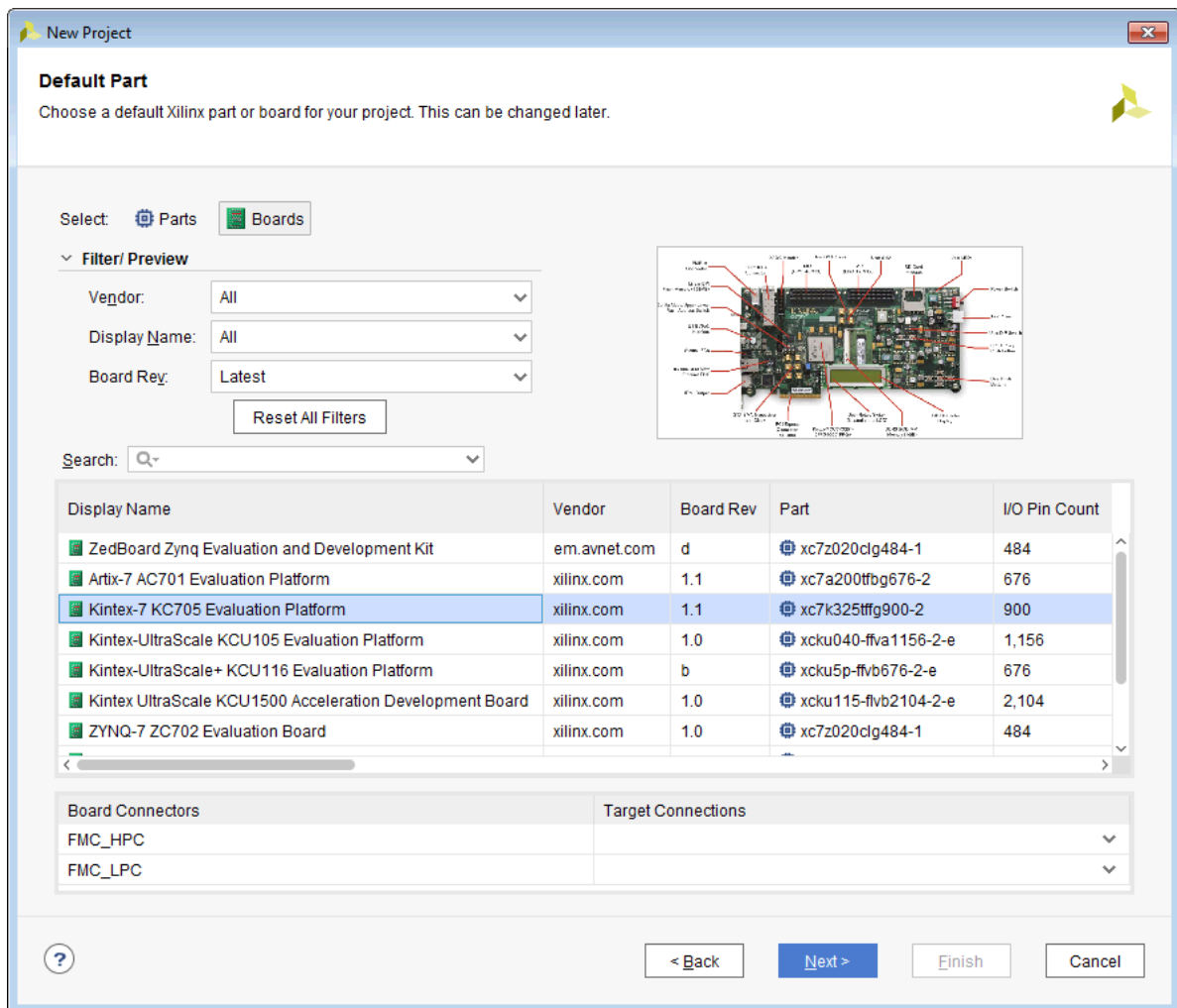
In addition to the Video PHY Controller, HDMI Transmitter Subsystem and HDMI Receiver Subsystem core, the complete example design includes the following cores:

- MicroBlaze or Zynq-7000 AP SoC or Zynq UltraScale+ MPSoC
- MicroBlaze Debug Module (Only for MicroBlaze based processor subsystem)
- AXI Interconnect
- Local Memory Bus (Only for MicroBlaze based processor subsystem)
- LMB BRAM Controller (Only for MicroBlaze based processor subsystem)
- Block Memory Generator (Only for MicroBlaze based processor subsystem)
- Clocking Wizard
- Processor System Reset
- AXI UARTLite (Only for MicroBlaze based processor subsystem)
- AXI Interrupt Controller (Only for MicroBlaze based processor subsystem)
- AXI IIC
- AXI GPIO
- Video Test Pattern Generator
- AXI4-Stream Register Slice
- Utility Buffer
- Utility Vector Logic

- AUD_PAT_GEN (Custom IP)
- HDMI_ACR_CTRL (Custom IP)

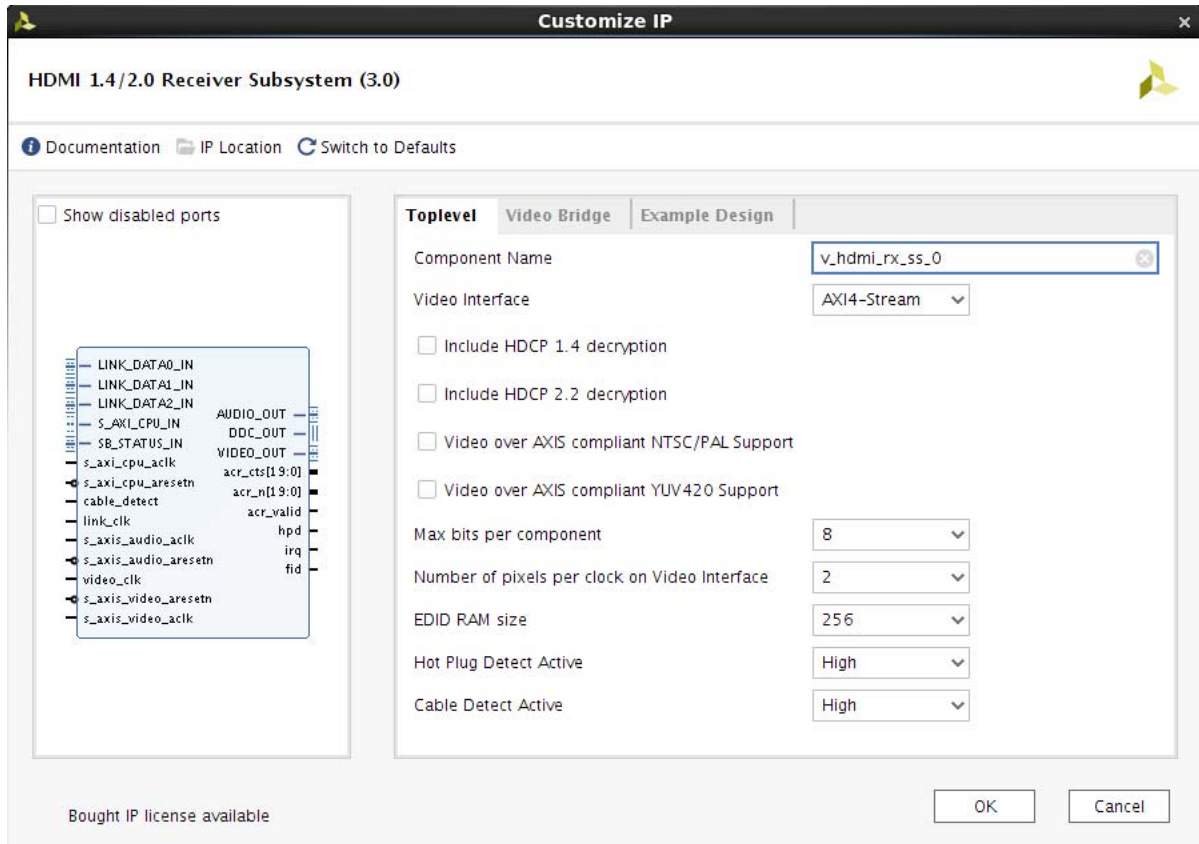
Running the Example Design

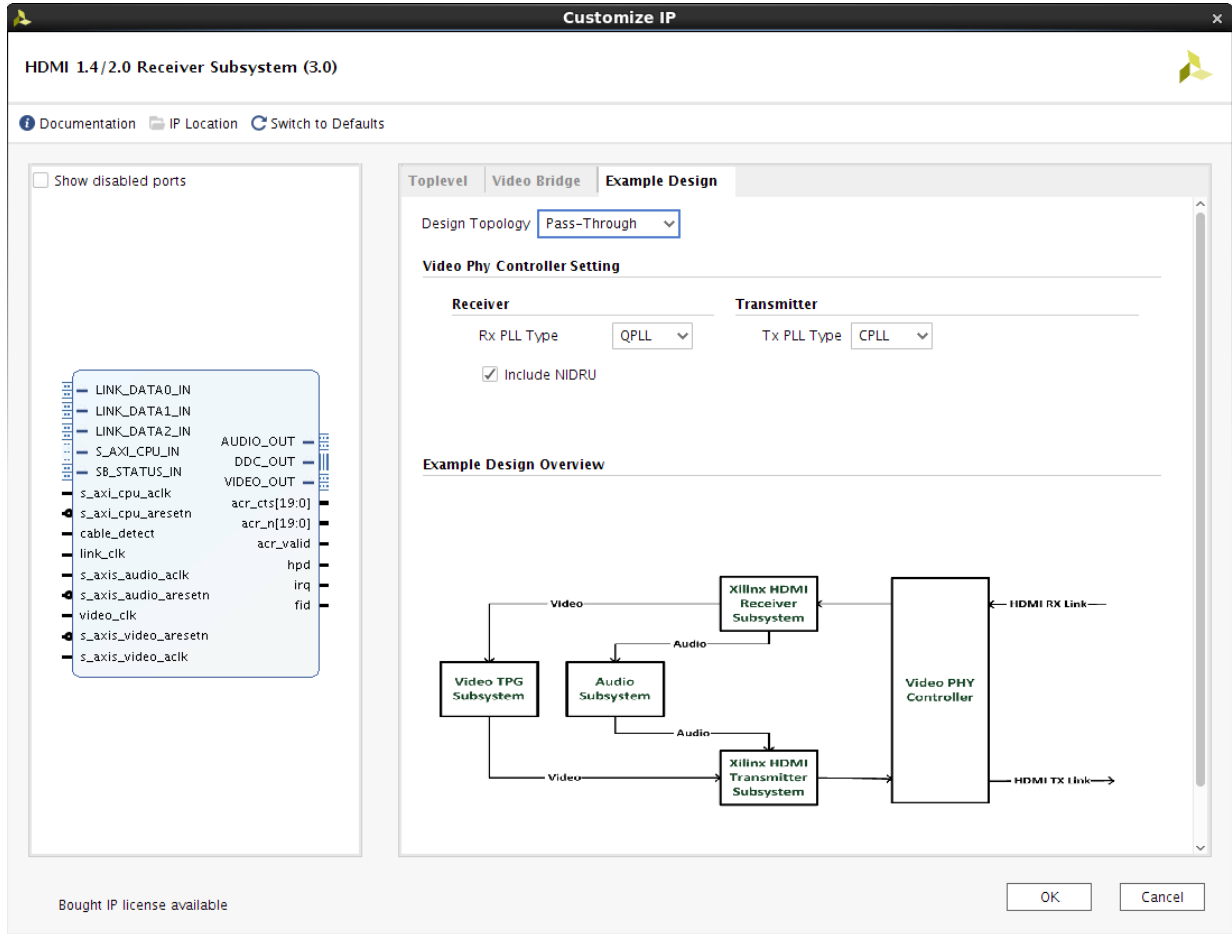
1. Open the Vivado Design Suite and create a new project.
2. In the pop-up window, press **Next** until you get to the page to select Xilinx® part or board for the project.



3. Select the Board. (KC705, KCU105, ZC706, and ZCU102 are supported.)
4. Click **Finish**.
5. Click **IP Catalog** and select HDMI 1.4/2.0 Receiver Subsystem under Video Connectivity, then double click on it.
 - For the Example Design flow, Native Video Interface is not supported.

- You can rename the IP component name, which is used as example design project name.
6. Configure HDMI 1.4/2.0 Receiver Subsystem, then click **OK**.





The **Generate Output Products** dialog box appears.

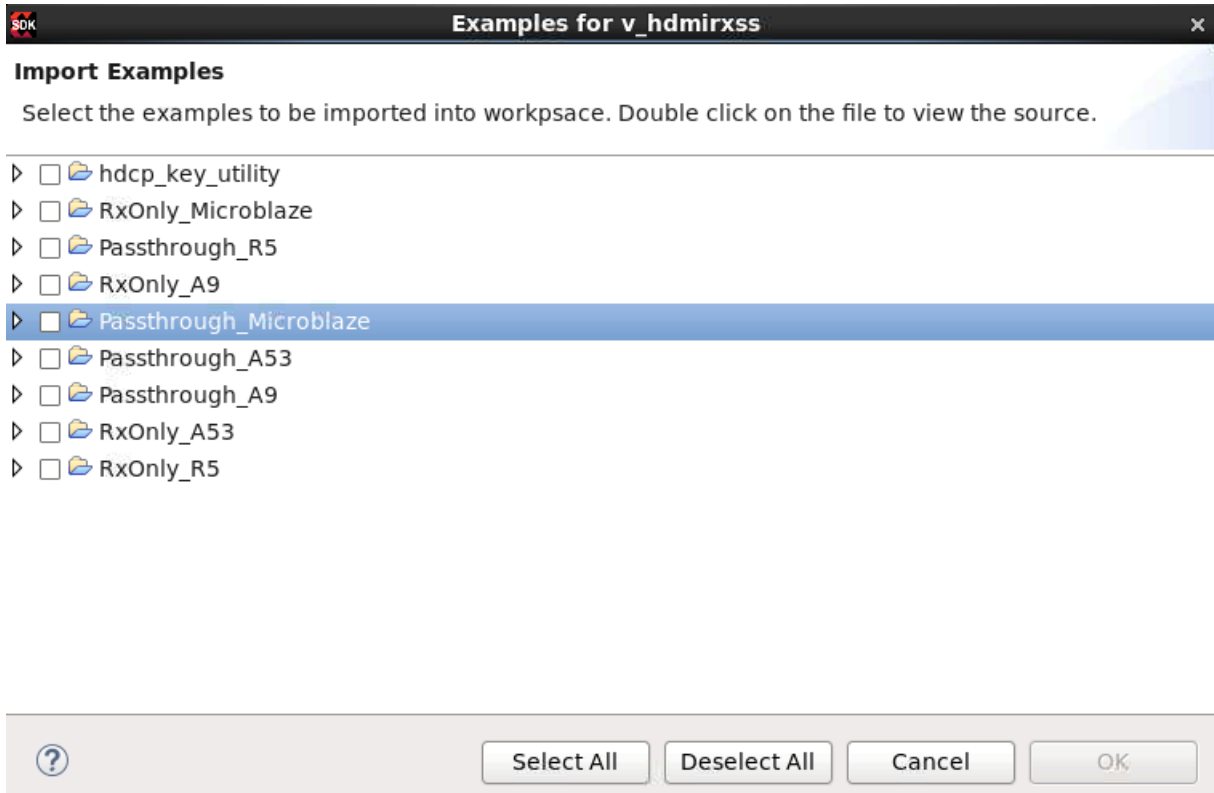
7. Click on **Generate**.
 - a. You may optionally click **Skip** if you just want to generate the example design.
8. Right click on the HDMI 1.4/2.0 Receiver Subsystem component under Design source, and click **Open IP Example Design**.
9. Choose the target project location, then click **OK**.

The IPI Design is then generated. You may choose to Run Synthesis, Implementation, or Generate Bitstream.

A tab to your system.mss opens.

- From system.mss, find the HDMI 1.4/2.0 Receiver Subsystem and click on **Import Examples**.

A window pops up with a list of HDMI application examples.



Refer to [Table 5-1](#) to select the respective application.

Table 5-1: Applications for Example Design

Board	Processor	Topology	Import Example Selection
KC705/KCU105	MicroBlaze	Pass-through	Passthrough_MicroBlaze
KC705/KCU105	MicroBlaze	Rx Only	RxOnly_MicroBlaze
ZC706	A9	Pass-through	Passthrough_A9
ZC706	A9	Rx Only	RxOnly_A9
ZCU102	A53	Pass-through	Passthrough_A53
ZCU102	A53	Rx Only	RxOnly_A53
ZCU102	R5	Pass-through	Passthrough_R5
ZCU102	R5	Rx Only	RxOnly_R5

The example application is built successfully. The .elf is ready to use.

HDCP Key Utility

An optional `hdcp_key_utility` application software is available for using the same hardware to program your own HDCP encryption keys into the EEPROM (FMC or on-board).

To `hdcp_key_utility` application:

1. Import Example from SDK and choose `hdcp_key_utility`.
2. Open `hdcp_key_utility.c` from the SDK project.
3. The arrays `Hdcp22Lc128`, `Hdcp22Key`, `Hdcp14Key1`, and `Hdcp14Key2` hold the HDCP keys and are empty. Fill these arrays with the acquired HDCP keys. The arrays are defined in big endian byte order.
4. Save the file and compile the design.
5. Run the design.

The terminal displays the following output:

```
HDCP Key EEPROM v1.0
This tool encrypts and stores the HDCP 2.2 certificate and HDCP 1.4 keys into the
EEPROM on the HDMI FMC board
Enter Password ->
```

The HDCP keys are encrypted using this password. The same password is used in the reference design to decrypt the HDCP keys.

The application is terminated after completing the programming of HDCP keys.

Note: The keys only need to be programmed into the EEPROM once.

Formatting HDCP Keys for HDCP 1.x

The `hdcp_key_utility.c` has two (empty) HDCP 1.x key arrays.

- The `Hdcp14Key1` array
This array holds the HDCP 1.x RX KSV and Keys.
- The `Hdcp14Key2` array
This array holds the HDCP 1.x RX KSV and Keys.

The arrays have a size of 328 bytes and contain the Key Selection Vector (KSV) (5 bytes padded with zeros to 8 bytes) and key set (320 bytes), where each key is 7 bytes padded with zeros to 8 bytes.

To format the HDCP 1.x keys for the `key_utility`, follow the steps below:

1. Discard the 20 byte SHA-1.

2. Pad each key on the right with one byte of 0s (KSV is already padded).

You should now have 1 x 8 byte KSV + 40 x 8 byte Keys.

3. Byte swap each 8 byte set to reverse their order (convert from Little-endian to Big-endian).

Note: The facsimile keys given in HDCP 1.4 spec are already in little-endian format, so byte swap is not needed when using them for test purpose.

The final result should be a 328 byte HDCP 1.4 keyset.

Formatting HDCP Keys for HDCP 2.2

The `hdcp_key_utility.c` has two (empty) HDCP 2.2 key arrays.

- The `hdcp22_lc128` array

The global secret constant for the HDCP 2.2 TX. The size is 16 bytes and the license constant from the HDCP 2.2 TX certificate is placed into the array (position 4-19)

- The `Hdcp22RxPrivateKey` array

This array holds the HDCP 2.2 RX certificate. The array has a size of 902 bytes. The contents are the header (4), license constant (36 bytes) and key set (862), so the total is 902 bytes.

Running the Reference Design (KC705)

Use the following steps to execute the system using generated bitstream and software elf from the example design

1. Launch the Xilinx System Debugger by selecting **Start > All Programs > Xilinx Design Tools > Vivado 2017.4 > Vivado 2017.4 Tcl Shell**.
2. In the Xilinx command shell window, change to the Example Design Project directory:

```
Vivado% cd ./v_hdmi_rx_ss_0_ex
```

3. Invoke Xilinx System Debugger (`xsdb`).

```
Vivado% xsdb
```

4. Establish connections to debug targets.

```
xsdb% connect
```

5. Download the bitstream to the FPGA.:

```
xsdb% fpga -file ./v_hdmi_rx_ss_0_ex.runs/impl_1/
exdes_wrapper.bit
```

6. Set the target processor.

```
xsdb% target -set 3
```

7. Download the software .elf to the FPGA.

```
xsdb% dow ./v_hdmi_rx_ss_0_ex.sdk/<name of bsp>_xhdmi_example_1/
Debug/<name of bsp>_xhdmi_example_1.elf
```

8. Run the software.

```
xsdb% stop
xsdb% rst
xsdb% con
```

9. Exit the XSDB command prompt.

```
xsdb% exit
```



IMPORTANT: When using the TB-FMCH-HDMI4K example design with the KCU105 board, you must set the FMC VADJ_1V8 Power Rail before programming the FPGA with bitstream generated from Example Design Flow. [KCU105 Board FMCH VADJ Adjustment](#) shows the steps on how to set the VADJ power rail when using KCU105 board. For more details about KCU105 Board, to [KCU105 Board User Guide \[Ref 19\]](#).

KCU105 Board FMCH VADJ Adjustment

The KCU105 board system controller must apply power to the VADJ power rail for the HDMI 2.0 FMC card (TB-FMCH-HDMI4K). Most new boards are per-programmed and should be detected. The VADJ is powered when the DS19 LED (located near the power switch on the KCU105 board) is ON.

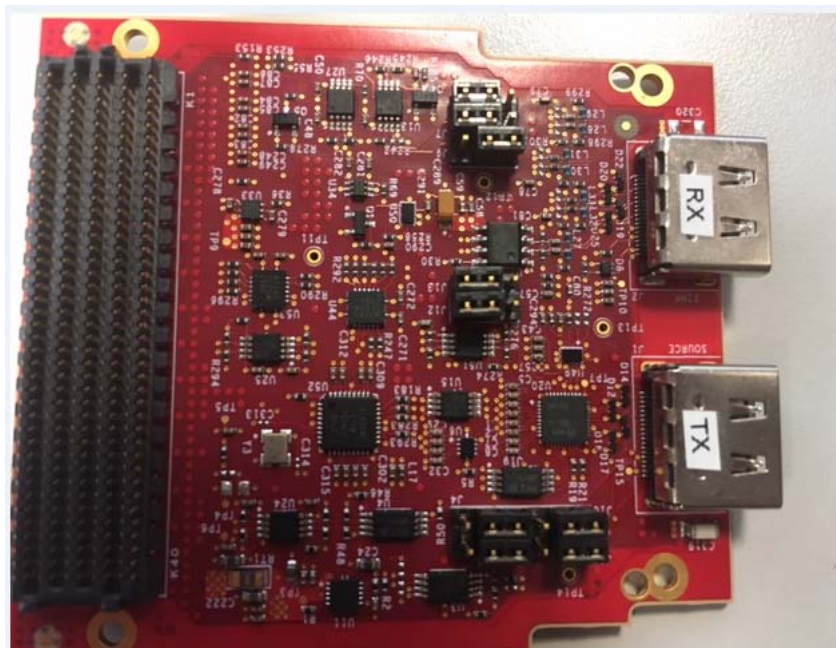
If an older version KCU105 board is used, or the board is not properly programmed upon receiving, you must manually set the VADJ power rail to 1.8V for the HDMI 2.0 FMC card prior to bitstream configuration.

Perform these steps to set the VADJ power rail through the UART terminal are:

1. Connect a USB cable between the USB UART connector of the KCU105 board and a PC running Windows.
2. Use the Windows Device Manager to determine which virtual COM port is assigned to the UART for the Zynq-7000 AP SoC system controller and which is assigned to the UART for the UltraScale FPGA. In the list of COM ports in the Device Manager window, the enhanced COM port associated with the CP210x, is the one connected to the KCU105

board system controller and the standard COM port is the one connected to the FPGA UART.

3. Open a terminal window (115200, 8, N, 1) and set the COM port to the one communicating with the KCU105 board system controller.
4. After the UART terminal is connected, power cycle the KCU105 board to refresh the system controller menu in the UART terminal. Select this option in the system controller menu:
 - a. Adjust FPGA Mezzanine Card (FMC) Settings.
5. In the next menu, select:
 - a. Set FMC VADJ to 1.8V.



IMPORTANT: Ensure that the jumpers are set correctly on their HDMI 2.0 FMC daughter card.

Migration Notes

When migrating from version 2016.3 or earlier, make note of the following:

- Hot Plug Detect Active has been added to HDMI 1.4/2.0 Transmitter Subsystem GUI. Choose High in the Example Design (according to board design).
- Hot Plug Detect Active has been added to HDMI 1.4/2.0 Receiver Subsystem GUI. Choose Low in Example Design (according to board design).
- Cable Detect Active has been added to HDMI 1.4/2.0 Receiver Subsystem GUI.

Choose Low in Example Design (according to board design).

- HDCP 1.4/2.2 is enabled by default in Example Design application software.

Removed UART option to Enable HDCP 1.4 or HDCP 2.2.

- Auto switching has been added to the Example Design Application software.

You do not need to choose HDCP 1.4 or HDCP 2.2 from UART. A corresponding HDCP is selected according to the capability of connected source/sink. If the device support both HDCP 1.4 and HDCP 2.2, the priority is given to HDCP 2.2.

- HDCP repeater feature has been added.

You can enabled/disable it by selecting "h" from UART menu.

- System log is moved from direct UART printout to event log.

You can display the event log by selecting "z" from UART menu.

Verification, Compliance, and Interoperability

Compliance

HDCP compliance has been performed with the following DCP certified test equipment:

- SisplayLabs SL8800
 - HDCP 1.4: 1A, 1B, 2C
 - HDCP 2.2: 1A, 1B, 2C
- Quantum Data QD980
 - HDCP 2.2: 1A, 1B, 2C

Interoperability

Interoperability tests for the HDMI 1.4/2.0 Receiver Subsystem have been conducted with the following hardware setup.

Hardware Testing

The HDMI 1.4/2.0 Receiver Subsystem has been validated using

- Kintex®-7 FPGA Evaluation Kit (KC705)
- Kintex® UltraScale™ FPGA Evaluation Kit (KCU105)
- Inrevium Artix-7 FPGA ACDC A7 Evaluation Board
- Zynq®-7000 All Programmable SoC evaluation board (ZC706)
- ZCU102 Evaluation Board

This release is tested with the following source devices:

- Quantum Data 980B
- Quantum Data 780B
- Apple TV (Gen 2/3/4)
- Android M8 media player
- Apple MacBook Pro
- Google Chromecast
- Open Hour media box
- Dell Latitude laptop (E7240)
- Intel HD Graphics 4000
- Nvidia GTX970 graphics card
- UGOOS media box
- LG 27mu67
- LG BP736
- Philips BDP2180K
- Sony BDP-S3500
- Sony BDP-S6500
- Samsung BD-J5900
- Murideo video generator / SIX-G
- Nvidia shield
- Roku 4
- Nvidia GTX980

Video Resolutions

Figure A-1 shows the hardware setup for AXI4-Stream Video Interface. An HDMI source connects to Video PHY Controller, which converts the HDMI Video into LINK DATA and sends to the HDMI RX Subsystem. Then, the HDMI RX Subsystem translates the LINK DATA into AXI4-Stream Video and sends to the Test Pattern Generator. By setting the Test Pattern Generator to pass-through mode, the AXI4-Stream Video from the HDMI RX Subsystem is passed to HDMI TX Subsystem where it gets translated to LINK DATA again and sends back to the Video PHY Controller. The Video PHY Controller then converts it back to HDMI Video and sends to HDMI Sink.

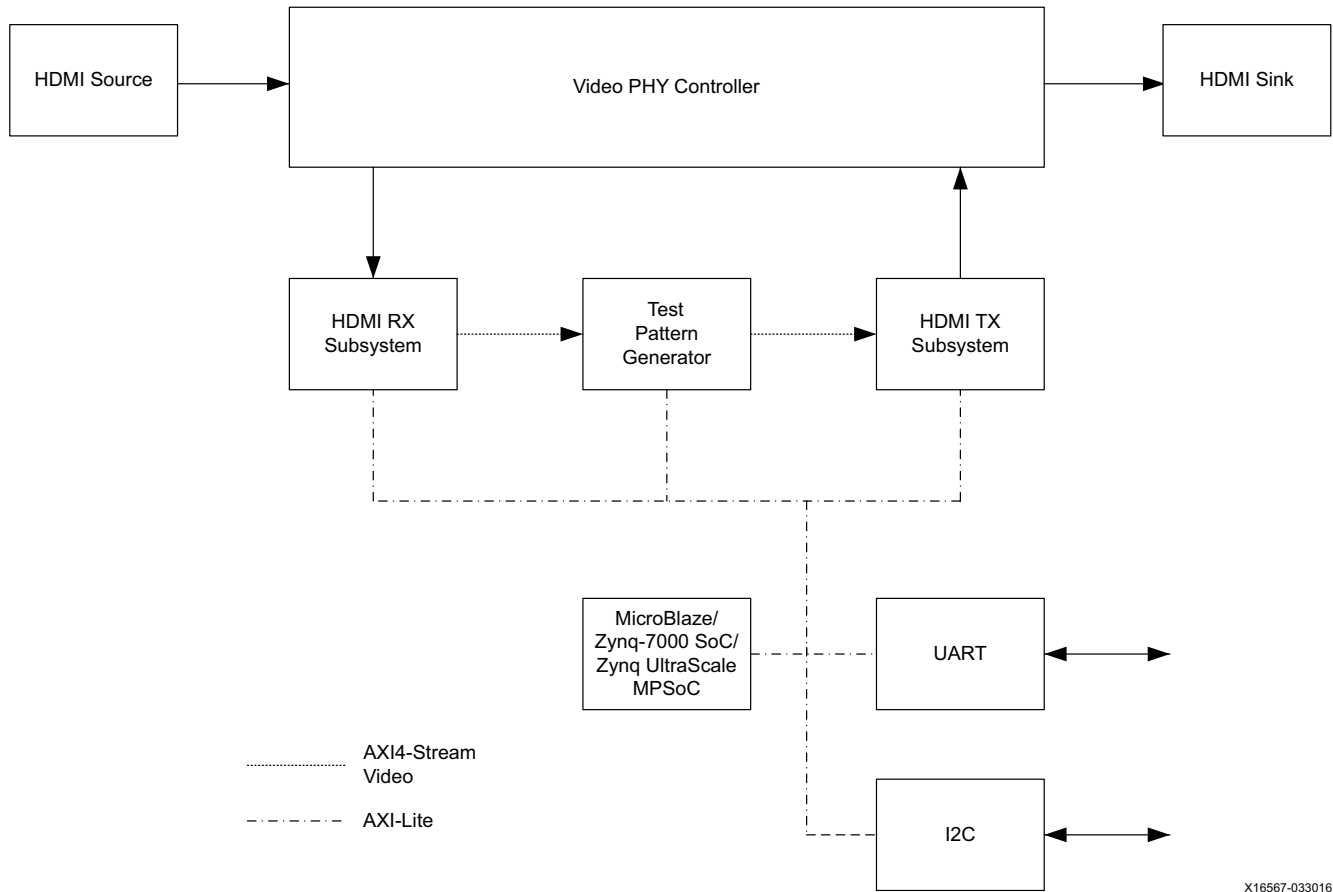


Figure A-1: Test Setup for AXI4-Stream Video Interface

For Video PHY Controller settings and PLL selections, see the *Video PHY Controller LogiCORE IP Product Guide (PG230)* [Ref 23].

Similarly, [Figure A-2](#) shows the hardware setup for Native Video Interface. The only difference is that two Video Bridge modules are added in between the HDMI RX Subsystem and the Test Pattern Generator, and between the Test Pattern Generator to the HDMI TX Subsystem.

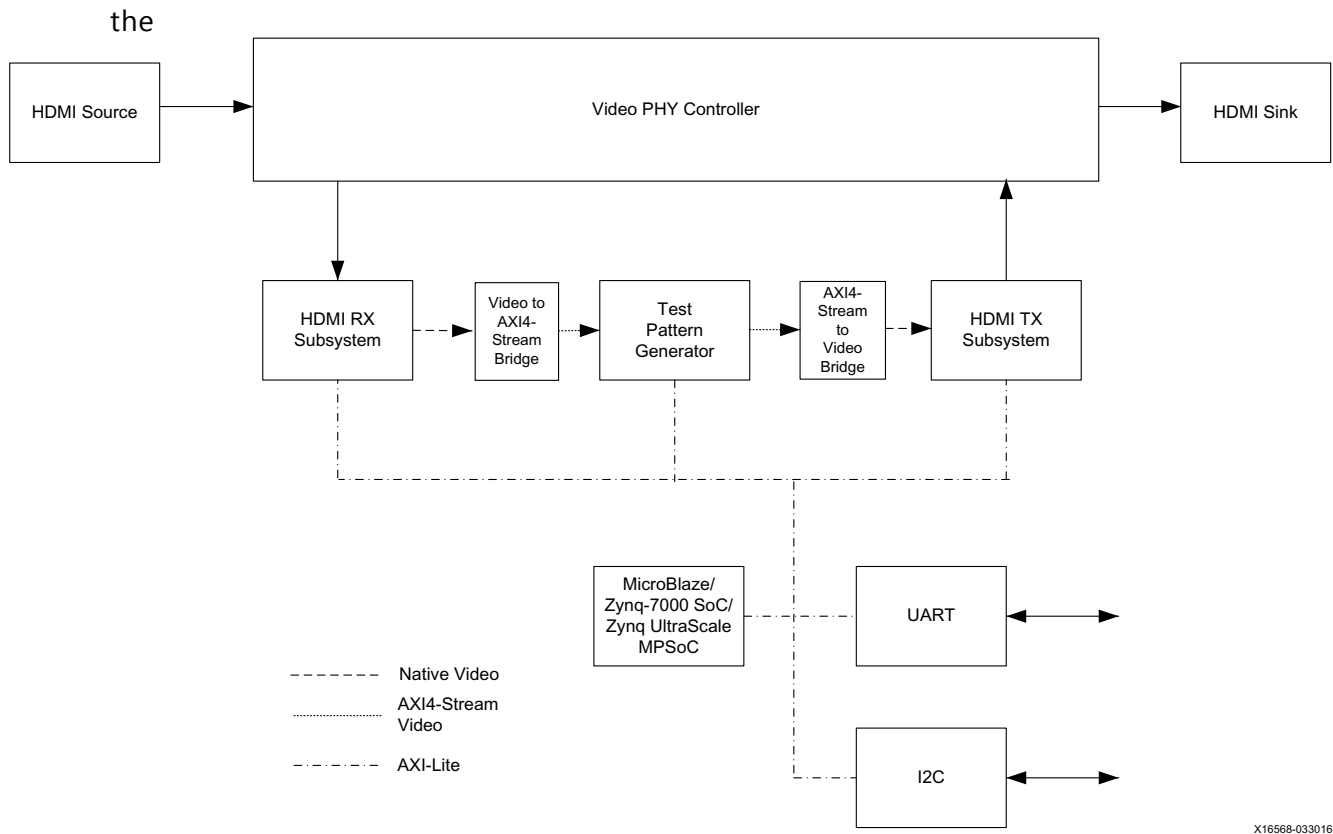


Figure A-2: Test Setup for Native Video Interface

Table A-1, Table A-2, and Table A-3 show the video resolutions that were tested as part of the release for different video formats.

Table A-1: Tested Video Resolutions for RGB 4:4:4 and YCbCr 4:4:4

Resolution	Horizontal		Vertical		Frame Rate (Hz)
	Total	Active	Total	Active	
480i60	858	720	525	480	60
576i50	864	720	625	576	50
1080i50	2640	1920	1125	1080	50
1080i60	2200	1920	1125	1080	60
480p60	858	720	525	480	60
576p50	864	720	625	576	50
720p50	1980	1280	750	720	50
720p60	1650	1280	750	720	60
1080p24	2750	1920	1125	1080	24
1080p25	2640	1920	1125	1080	25
1080p30	2200	1920	1125	1080	30
1080p50	2640	1920	1125	1080	50

Table A-1: Tested Video Resolutions for RGB 4:4:4 and YCbCr 4:4:4 (Cont'd)

Resolution	Horizontal		Vertical		Frame Rate (Hz)
	Total	Active	Total	Active	
1080p60	2200	1920	1125	1080	60
1080p120	2200	1920	1125	1080	120
2160p24	5500	3840	2250	2160	24
2160p25	5280	3840	2250	2160	25
2160p30	4400	3840	2250	2160	30
2160p60 ⁽³⁾	4400	3840	2250	2160	60
4096x2160p60 ⁽³⁾	4400	4096	2250	2160	60
vgap60	800	640	525	480	60
svgap60	1056	800	628	600	60
xgap60	1344	1024	806	768	60
sxgap60	1688	1280	1066	1024	60
wxgap60	1440	1280	790	768	60
wxga+p60	1792	1366	798	768	60
uxgap60	2160	1600	1250	1200	60
wuxgap60	2592	1920	1245	1200	60
wsxgap60	2240	1680	1089	1050	60

Notes:

1. Not all resolutions can be supported due to VPHY limitation. For details, refer to *Video PHY Controller LogiCORE IP Product Guide* (PG230) [Ref 23].
2. In this release, UXGA 60 Hz is supported in the HDMI 1.4/2.0 Receiver Subsystem for 8, 10, and 12 bits per component only.
3. For 4kp60 YUV444/RGB video, only 8bits is supported as defined by HDMI 2.0 spec due to bandwidth limitation.

Table A-2: Tested Video Resolutions for YCbCr 4:2:2 at 12 Bits/component

Resolution	Horizontal		Vertical		Frame Rate (Hz)
	Total	Active	Total	Active	
1080i50	2640	1920	1125	1080	50
1080i60	2200	1920	1125	1080	60
480p60	858	720	525	480	60
576p50	864	720	625	576	50
720p50	1980	1280	750	720	50
720p60	1650	1280	750	720	60
1080p24	2750	1920	1125	1080	24
1080p25	2640	1920	1125	1080	25
1080p30	2200	1920	1125	1080	30

Table A-2: Tested Video Resolutions for YCbCr 4:2:2 at 12 Bits/component

Resolution	Horizontal		Vertical		Frame Rate (Hz)
	Total	Active	Total	Active	
1080p50	2640	1920	1125	1080	50
1080p60	2200	1920	1125	1080	60
2160p24	5500	3840	2250	2160	24
2160p25	5280	3840	2250	2160	25
2160p30	4400	3840	2250	2160	30
vgap60	800	640	525	480	60
svgap60	1056	800	628	600	60
wxgap60	1440	1280	790	768	60
wxga+p60	1792	1366	798	768	60
uxgap60	2160	1600	1250	1200	60
wuxgap60	2592	1920	1245	1200	60
wsxgap60	2240	1680	1089	1050	60

Table A-3: Tested Video Resolutions for YCbCr 4:2:0 at 8, 10, 12, 16 Bits/Component

Resolution	Horizontal		Vertical		Frame Rate (Hz)
	Total	Active	Total	Active	
2160p60	4400	3840	2250	2160	60

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.



TIP: *If the IP generation halts with an error, there might be a license issue. See [License Checkers in Chapter 1](#) for more details.*

Finding Help on Xilinx.com

To help in the design and debug process when using the HDMI 1.4/2.0 Receiver Subsystem, the [Xilinx Support web page](#) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the HDMI 1.4/2.0 Receiver Subsystem. This guide, along with documentation related to all products that aid in the design process, can be found on the [Xilinx Support web page](#) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the [Downloads page](#). For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this subsystem can be located by using the Search Support box on the main [Xilinx support web page](#). To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the HDMI 1.4/2.0 Receiver Subsystem

AR: [54546](#)

Technical Support

Xilinx provides technical support at the [Xilinx Support web page](#) for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the [Xilinx Support web page](#).

Debug Tools

Tools are available to address HDMI 1.4/2.0 Receiver Subsystem design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [[Ref 20](#)].

Reference Boards

Various Xilinx development boards support the HDMI 1.4/2.0 Receiver Subsystem. These boards can be used to prototype designs and establish that the subsystem can communicate with the system.

- 7 series FPGA evaluation board
 - KC705
- UltraScale FPGA evaluation board
 - KCU105
- Zynq-7000 All Programmable SoC evaluation board
 - ZC706
- UltraScale+ FPGA evaluation board
 - ZCU102

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado debug feature is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the debug feature for debugging the specific problems.

General Checks

- Ensure that all the timing constraints and all other constraints were met during implementation.
- Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the `locked` port.
- If your outputs go to 0, check your licensing.
 - User LEDs (KC705/KCU105/ZC706/ZCU102)
 - LED0 - HDMI TX subsystem lock (when HDMI Pass-Through Example Design is used)
- The system flow/state information from the event logs by UART option **z**.

Table B-1: System Flow and State Information

At System Start-up	While Changing Video Stream from Source Device
VPHY log ----- GT init start GT init done RX frequency event RX timer event RX DRU disable QPLL reconfig done GT RX reconfig start GT RX reconfig done QPLL lock RX reset done RX MMCM reconfig done HDMI RX log ----- Initializing HDMI RX core.... Initializing AXI Timer core.... Reset HDMI RX Subsystem.... RX cable is connected.... RX TMDS reference clock change RX Stream Init RX mode changed to HDMI RX Stream Start RX Stream is Up	VPHY log ----- QPLL lost lock RX frequency event RX frequency event RX timer event RX DRU enable QPLL reconfig done GT RX reconfig start GT RX reconfig done QPLL lock RX reset done RX frequency event QPLL lost lock RX frequency event RX timer event RX DRU disable QPLL reconfig done GT RX reconfig start GT RX reconfig done QPLL lock RX reset done RX MMCM reconfig done HDMI RX log ----- RX Stream is Down RX Stream is Down RX mode changed to DVI RX TMDS reference clock change RX Stream Init RX Stream Start RX TMDS reference clock change RX Stream Init RX mode changed to HDMI RX Stream Start RX Stream is Up
Notes: 1. Initializing AXI Timer Core flow is only logged when HDCP option is enabled.	

Interface Debug

AXI4-Lite Interfaces

Read from a register that does not have all 0s as a default to verify that the interface is functional. Output `s_axi_arready` asserts when the read address is valid, and output `s_axi_rvalid` asserts when the read data/response is valid. If the interface is unresponsive, ensure that the following conditions are met:

- The `s_axi_aclk` and `aclk` inputs are connected and toggling.
- The interface is not being held in reset, and `s_axi_areset` is an active-Low reset.
- The interface is enabled, and `s_axi_aclken` is active-High (if used).
- The main subsystem clocks are toggling and that the enables are also asserted.

AXI4-Stream Interfaces

If data is not being transmitted or received, check the following conditions:

- If transmit `<interface_name>_tready` is stuck Low following the `<interface_name>_tvalid` input being asserted, the subsystem cannot send data.
- If the receive `<interface_name>_tvalid` is stuck Low, the subsystem is not receiving data.
- Check that the `aclk` inputs are connected and toggling.
- Check that the AXI4-Stream waveforms are being followed.
- Check subsystem configuration.

Application Software Development

Device Drivers

The HDMI 1.4/2.0 Receiver Subsystem driver abstracts the included supporting elements and provides you with an API for control. The API can be easily integrated into your application thereby providing an out-of-the-box solution.

The subsystem driver is a bare-metal driver, which provides an abstracted view of the feature set provided by each sub-core. It dynamically manages the data and control flow through the processing elements, based on the input/output stream configuration set at run time. Internally, it relies on sub-core drivers to configure the sub-core IP blocks.

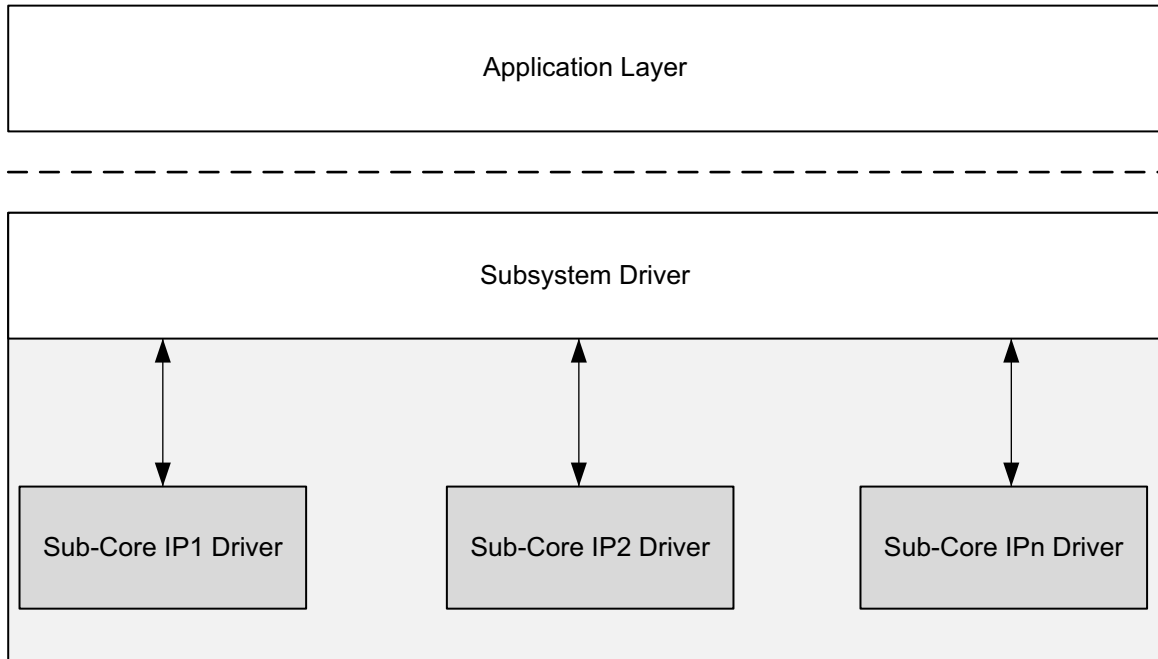
Architecture

The subsystem driver provides an easy-to-use, well-defined API to help integrate the subsystem in an application without having to understand the underlying complexity of configuring each and every sub-core.

The subsystem driver consists of the following:

- **Subsystem layer:** Queries exported hardware to determine the subsystem hardware configuration and pull-in sub-core drivers, at build time. It abstracts sub-core drivers, which interface with hardware at register level, into a set of functional APIs. The subsystem driver uses these APIs to dynamically manage the data flow through processing elements.
- **Sub-core drivers:** Every included sub-core has a driver associated with it that provides APIs to interface with the core hardware.

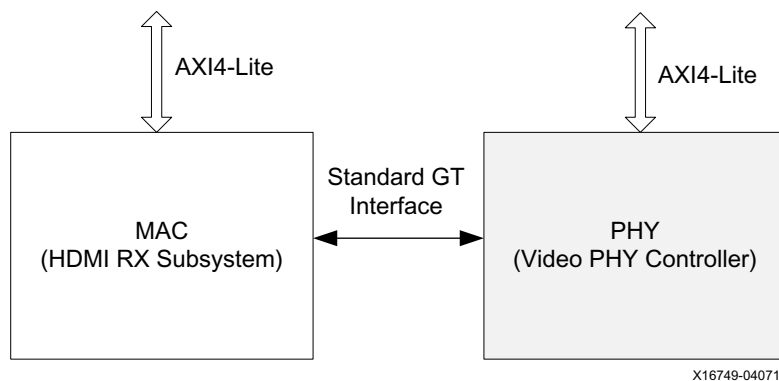
Figure C-1 shows the HDMI 1.4/2.0 Receiver Subsystem architecture.



X16747-040716

Figure C-1: Subsystem Driver Architecture

The HDMI 1.4/2.0 Receiver Subsystem is a MAC subsystem which works with a Video PHY Controller (PHY) to create a video connectivity system. The HDMI 1.4/2.0 Receiver Subsystem is tightly coupled with the Xilinx Video PHY Controller, which itself is independent and offer flexible architecture with multiple-protocol support. Both MAC and PHY are dynamically programmable through the AXI4-Lite interface.



X16749-040716

Figure C-2: MAC Interfaces with PHY

Usage

The HDMI 1.4/2.0 Receiver Subsystem provides a set of API functions for application code to use. On top of that, when HDMI 1.4/2.0 Receiver Subsystem hardware interrupts are generated, the subsystem driver is invoked to configure the system accordingly. HDMI 1.4/2.0 Receiver Subsystem provides callback structure to hook up your own callback functions.

Application Integration

Figure C-4 shows an example code on how an HDMI 1.4/2.0 Receiver Subsystem can be used in your application.

```

1927     XV_HdmiRxSs HdmiRxSs;          /* HDMI RX SS structure */
1928     XV_HdmiRxSs_Config *XV_HdmiRxSs_ConfigPtr;
1929
1930     // Initialize HDMI RX Subsystem
1931     /* Get User Edid Info */
1932     XV_HdmiRxSs_SetEdidParam(&HdmiRxSs, (u8*)&Edid, sizeof(Edid));
1933     XV_HdmiRxSs_ConfigPtr =
1934         XV_HdmiRxSs_LookupConfig(XPAR_V_HDMI_RX_SS_0_V_HDMI_RX_DEVICE_ID);
1935
1936     if(XV_HdmiRxSs_ConfigPtr == NULL)
1937     {
1938         HdmiRxSs.IsReady = 0;
1939         return (XST_DEVICE_NOT_FOUND);
1940     }
1941
1942     //Initialize top level and all included sub-cores
1943     Status = XV_HdmiRxSs_CfgInitialize(&HdmiRxSs, XV_HdmiRxSs_ConfigPtr,
1944         XV_HdmiRxSs_ConfigPtr->BaseAddress);
1945     if(Status != XST_SUCCESS)
1946     {
1947         xil_printf("ERR:: HDMI RX Subsystem Initialization failed %d\r\n", Status);
1948         return(XST_FAILURE);
1949     }
1950
1951     //Register HDMI RX SS Interrupt Handler with Interrupt Controller
1952     Status |= XIntc_Connect(&Intc,
1953         XPAR_MICROBLAZE_SS_AXI_INTC_0_V_HDMI_RX_SS_0_IRQ_INTR,
1954         (XInterruptHandler)XV_HdmiRxSS_HdmiRxIntrHandler,
1955         (void *)&HdmiRxSs);
1956
1957     if (Status == XST_SUCCESS){
1958         XIntc_Enable(&Intc,
1959             XPAR_MICROBLAZE_SS_AXI_INTC_0_V_HDMI_RX_SS_0_IRQ_INTR);
1960     }
    
```

Figure C-4: Application Example Code

To integrate and use the HDMI 1.4/2.0 Receiver Subsystem driver in your application, the following steps must be followed:

1. Include the subsystem header file `xv_hdmiRxSs.h` that defines the subsystem object.
2. Provide the storage for a subsystem driver instance in your application code. For example:

```
XV_HdmiRxSs HdmiRxSs;
```

3. In the subsystem driver instance, there is a metadata structure to store the subsystem hardware configuration. Declare a pointer variable in the application code to point to the instance:

```
XV_HdmiRxSs_Config *XV_HdmiRxSs_ConfigPtr;
```

4. Set EDID parameter for HDMI 1.4/2.0 Receiver Subsystem Subsystem.

```
void XV_HdmiRxSs_SetEdidParam(XV_HdmiRxSs *InstancePtr,
                             u8 *EdidDataPtr,
                             u16 Length);
```

5. For each subsystem instance, the data structures declared in steps 2 and 3 need to be initialized based on its hardware configuration, which is passed through metadata structure from `xparameters.h` uniquely identified by device ID.

To initialize the subsystem, call the following two API functions:

```
XV_HdmiRxSs_Config* XV_HdmiRxSs_LookupConfig(u32 DeviceId);
int XV_HdmiRxSs_CfgInitialize(XV_HdmiRxSs *InstancePtr,
                             XV_HdmiRxSs_Config *CfgPtr,
                             u32 EffectiveAddr);
```

The Device ID can be found in `xparameters.h`:

```
XPAR_[HDMI RX Subsystem Instance Name in IPI]_DEVICE_ID
```

6. Each interrupt source has an associated ISR defined in the subsystem. Register the ISR with the system interrupt controller and enable the interrupt.

```
int XIntc_Connect(XIntc          *InstancePtr,
                 u8             Id,
                 XInterruptHandler Handler,
                 void           *CallBackRef);
void XIntc_Enable(XIntc          *InstancePtr,
                 u8             Id);
```

Where ID can be found in `xparameters.h`.

Note:

1. Prepare the 256 bytes of EDID data and store in an array before calling the mentioned API function.
2. The EDID data is loaded into the HDMI 1.4/2.0 Receiver Subsystem during initialization. This is handled by the subsystem driver, no user intervention is needed.

HDCP RX Overview

The HDMI 1.4/2.0 Receiver Subsystem driver is responsible for combining HDCP 1.4 and HDCP 2.2 drivers APIs into a single common API for use by the user level application. The common HDCP driver API is able to handle the following HDCP configurations: HDCP 1.4 only, HDCP 2.2 only, and both. When both protocols are enabled, the common HDCP driver ensures that only one is active at any given time.

HDCP RX Driver Integration

This section describes the steps required to initialize and run the HDCP RX. The application should call the functions roughly in the order specified to ensure that the driver operates properly. When only a single HDCP protocol is enabled, either 1.4 or 2.2, a subset of the function calls might be needed.

1. Load the HDCP production keys into the HDMI subsystem. This function needs to be called for each key that is loaded. If HDCP 1.4 and 2.2 are enabled all the keys must be loaded, otherwise a subset of the keys are loaded. Note that the byte arrays used to store the key octet strings for HDCP are defined in big endian byte order.
 - `XV_HdmiRxSs_HdcpSetKey`
 - `XV_HDMIRXSS_KEY_HDCP14`
 - `XV_HDMIRXSS_KEY_HDCP22_LC128` (128-bit DCP Licensed Constant)
 - `XV_HDMIRXSS_KEY_HDCP22_PRIVATE` (902-byte DCP Receiver Device Key Set)

Position in Bytes	Size in Bytes	Description
0–39	40	Reserved
40–561	522	Device Public Certificate
562–901	340	Device Private Key ⁽¹⁾

Notes:

1. The actual Private Key size is 320 bytes. The additional 20 bytes is for a hash code that can be used by the software application to verify the keys before loading them. These additional bytes are not used by the HDCP driver.
2. Initialize the HDMI 1.4/2.0 Receiver Subsystem driver after the HDCP keys have been loaded. Initializing the subsystem begins the HDCP 1.4/2.2 drivers internally.
3. Connect the HDCP interrupt handlers to the interrupt controller interrupt ID:
 - `XV_HdmiRxSS_HdcpIntrHandler`
 - `XV_HdmiRxSS_HdcpTimerIntrHandler`
4. Set the HDCP user callback functions. These callbacks are optional and can be used as a hook to take action during various parts of the HDCP protocol. If there is no use for a callback at the application level, they can be left undefined.
 - `XV_HdmiRxSs_SetCallback`
 - `XV_HDMIRXSS_HANDLER_HDCP_AUTHENTICATED`
 - `XV_HDMIRXSS_HANDLER_HDCP_UNAUTHENTICATED`
 - `XV_HDMIRXSS_HANDLER_HDCP_AUTHENTICATION_REQUEST`
 - `XV_HDMIRXSS_HANDLER_HDCP_STREAM_MANAGE_REQUEST`
 - `XV_HDMIRXSS_HANDLER_HDCP_TOPOLOGY_UPDATE`

- XV_HDMIRXSS_HANDLER_HDCP_ENCRYPTION_UPDATE
5. Execute the poll function to run the HDCP state machine. This function checks to see which HDCP protocol is enabled, and then execute only the active protocol. The call to this function can be inserted in the main loop of the user application and should execute continuously. Because the HDCP RX state machine is run using this poll function, it is important to ensure that this function is given adequate CPU runtime, especially during authentication attempts.
 - XV_HdmiRxSs_HdcpPoll
 6. Set the HDCP protocol capability to notify the upstream transmitter which protocols are supported. Setting the HDCP protocol capability is optional and is used to override the default capability of the receiver. The default capability is set to both protocols. There are only two valid capability options: both and none. Setting the capability to none disables the HDCP DDC slave device. Note that setting the protocol capability does not enable the protocol. Protocol enablement is automatically handled by the subsystem, thus the legacy XV_HdmiRxSs_HdcpSetProtocol API is deprecated. Anytime the capability has changed, HPD should be immediately toggled to get the attention of the upstream transmitter.
 - XV_HdmiRxSs_HdcpSetCapability
 - XV_HDMIRXSS_HDCP_NONE
 - XV_HDMIRXSS_HDCP_BOTH
 - XV_HDMIRXSS_HDCP_22
 7. Check the status of authentication.
 - XV_HdmiRxSs_HdcpIsAuthenticated
 8. Check the status of the cipher encryption. This is the instantaneous encryption status of the cipher and can change between subsequent frames.
 - XV_HdmiRxSs_HdcpIsEncrypted
 9. Check the overall HDCP protocol status and log data. You can also set the level of detail for log information reported.
 - XV_HdmiRxSs_HdcpInfo
 - XV_HdmiRxSs_SetInfoDetail

Integrate Video PHY Controller Driver for HDMI RX Subsystem Usage

Because the HDMI 1.4/2.0 Receiver Subsystem is closely coupled with the Video PHY Controller, the following example code demonstrates how a Video PHY Controller can be used in your application.

```

2039     XVphy Vphy;                               /* VPHY structure */
2040     XVphy_Config *XVphyCfgPtr;
2041     // Initialize Video PHY
2042     XVphyCfgPtr = XVphy_LookupConfig(XPAR_VID_PHY_CONTROLLER_0_DEVICE_ID);
2043     if (XVphyCfgPtr == NULL) {
2044         print("Video PHY device not found\n\r\r");
2045         return XST_FAILURE;
2046     }
2047
2048     /* Initialize HDMI VPHY */
2049     Status = XVphy_HdmiInitialize(&Vphy, 0,
2050         XVphyCfgPtr, XPAR_CPU_CORE_CLOCK_FREQ_HZ);
2051     if (Status != XST_SUCCESS) {
2052         print("HDMI VPHY initialization error\n\r\r");
2053         return XST_FAILURE;
2054     }
2055
2056     /* Register VPHY Interrupt Handler */
2057     Status = XIntc_Connect(&Intc,
2058         XPAR_MICROBLAZE_SS_AXI_INTC_0_VID_PHY_CONTROLLER_0_IRQ_INTR,
2059         (XInterruptHandler)XVphy_InterruptHandler,
2060         (void *)&Vphy);
2061
2062     if (Status != XST_SUCCESS) {
2063         print("HDMI VPHY Interrupt Vec ID not found!\n\r\r");
2064         return XST_FAILURE;
2065     }
2066
2067     /* Enable VPHY Interrupt */
2068     XIntc_Enable(&Intc,
2069         XPAR_MICROBLAZE_SS_AXI_INTC_0_VID_PHY_CONTROLLER_0_IRQ_INTR);
    
```

Figure C-5: Application Example Code

To integrate and use the Video PHY Controller for HDMI 1.4/2.0 Receiver Subsystem in the application code, the following steps must be followed:

1. Include the subsystem header file `xvphy.h` that defines the subsystem object.
2. Declare and allocate space for a Video PHY Controller instance in your application code.

Example:

```
XVphy Vphy;
```

3. In the Video PHY Controller instance, there is a metadata structure to store its hardware configuration. Declare a pointer variable in the application code to point to the instance:

```
XVphy_Config *XVphyCfgPtr;
```

4. For each Video PHY Controller instance, the above data structure needs to be initialized based on its hardware configuration, which is passed through meta-structure from `xparameters.h` uniquely identified by device ID.

To initialize the Video PHY Controller, call the following two API functions:

```
XVphy_Config *XVphy_LookupConfig(u16 DeviceId);
u32 XVphy_HdmiInitialize(XVphy *InstancePtr,
                        u8 QuadId,
                        XVphy_Config *CfgPtr,
                        u32 SystemFrequency);
```

The Device ID can be found in `xparameters.h`:

```
XPAR_[Video PHY Controller Instance Name in IPI]_DEVICE_ID
```

Similarly, `SystemFrequency` is the system frequency, which can also be found in `xparameters.h`

Note:

- Xilinx recommends initializing the Video PHY controller after the HDMI 1.4/2.0 Receiver Subsystem initialization is completed.
- Registering the Video PHY Controller interrupts are part of system application integration. Steps are shown in the previous section and not repeated here.

Interrupts

All interrupts generated by the HDMI 1.4/2.0 Receiver Subsystem are listed here:

1. **HPD** – Peripheral I/O to detect HDMI cable 5.0V signal
 - a. **Rising edge** – Cable connected
 - b. **Falling edge** – Cable disconnected
2. **Link Ready** – Every time when Video PHY Controller is reconfigured, the `link_clk` is regenerated. An HDMI RX sub-core register bit (link status bit) reflects the change of `link_clk` status. When stable `link_clk` is detected, it is set to 1. When `link_clk` becomes unstable, it is set to 0. The Link Ready is an interrupt to detect the change of the link status bit.
 - a. **Rising edge** – Link is up
 - b. **Falling edge** – Link is down
3. **Video Ready** – This interrupt is generated by HDMI RX sub-core to reflect the status of received video stream.
 - a. **Rising edge** – Video Stream is stable (StreamUp)
 - b. **Falling edge** – Video Stream is not stable (StreamDown)

4. **HDMI Receiver Auxiliary Infoframe Interrupt** – This interrupt is generated when an Auxiliary Infoframe is received.
5. **HDMI Receiver Audio Infoframe Interrupt** – This interrupt is generated when an Audio Infoframe is received.
6. HDCP 1.4 Interrupt (only available when HDCP 1.4 is enabled in hardware)
7. HDCP 1.4 Timer Interrupt (only available when HDCP 1.4 is enabled in hardware)

Table C-1: Mapping between Interrupt Sources and Application Callback Functions

Interrupts	Callback
HPD	XV_HDMIRXSS_HANDLER_CONNECT
Link Ready	
Video Ready Note: It is edge triggered.	XV_HDMIRXSS_HANDLER_STREAM_UP XV_HDMIRXSS_HANDLER_STREAM_DOWN Video Ready rising edge: Stream Up Video Ready falling edge: Stream Down
	XV_HDMIRXSS_HANDLER_STREAM_INIT Note: This callback function is not directly mapped to any interrupt source. Instead it is executed when stream is detected and Video PHY Controller is stabilized for HDMI RX Subsystem to start stream locking.
HDMI Receiver Auxiliary Infoframe Interrupt	XV_HDMIRXSS_HANDLER_AUX
HDMI Receiver Audio Infoframe Interrupt	XV_HDMIRXSS_HANDLER_AUD
HDCP 1.4 Interrupt	
HDCP 1.4 Timer Interrupt	
HDCP 2.2 Timer Interrupt (only available when HDCP 2.2 is enabled in hardware)	
	XV_HDMIRXSS_HANDLER_HDCP_AUTHENTICATE Note: This callback function is not directly mapped to any interrupt source. Instead it is executed when the HDCP authentication state machine has reached the authenticated state.

Application Callback Functions

Subsystem driver provides a mechanism for the application to register a user-defined function that gets called within an interrupt context.

Callback functions defined in the application code must be registered with provided handlers, using the following defined API:

```
int XV_HdmiRxSs_SetCallback(XV_HdmiRxSs *InstancePtr,
```

```
u32 HandlerType,
void *CallbackFuncPtr,
void *CallbackRef);
```

Available handlers are defined in `xv_hdmirxss.h`:

- [XV_HDMIRXSS_HANDLER_CONNECT](#)
- [XV_HDMIRXSS_HANDLER_AUX](#)
- [XV_HDMIRXSS_HANDLER_AUD](#)
- [XV_HDMIRXSS_HANDLER_STREAM_UP](#)
- [XV_HDMIRXSS_HANDLER_STREAM_DOWN](#)
- [XV_HDMIRXSS_HANDLER_STREAM_INIT](#)
- [XV_HDMIRXSS_HANDLER_HDCP_AUTHENTICATE](#)

XV_HDMIRXSS_HANDLER_CONNECT

This interrupt is triggered every time when an HDMI RX cable connection or disconnection (HPD level transition) occurs.

The callback function needs to perform the following:

1. Enable or disable the differential input clock buffer depending on if cable connection or disconnection occurs, respectively.

```
void XVphy_IBufDsEnable(XVphy *InstancePtr,
                        u8 QuadId,
                        XVphy_DirectionType Dir,
                        u8 Enable);
```

2. Clear Video PHY RX TMDs Clock ratio when cable is disconnected:

```
Vphy.HdmiRxTmdsClockRatio = 0;
```

XV_HDMIRXSS_HANDLER_AUX

This interrupt is triggered every time when an Auxiliary InfoFrame packet is received.

The callback function needs to retrieve the InfoFrame packet data for system application to use.

XV_HDMIRXSS_HANDLER_AUD

This interrupt is triggered every time when an active audio stream is detected or the number of active audio channels changes.

The callback function can update the audio information to the application software.

XV_HDMIRXSS_HANDLER_STREAM_UP

This interrupt is triggered every time when an HDMI video stream becomes locked.

The callback function can update stream up information to the application software.

XV_HDMIRXSS_HANDLER_STREAM_DOWN

This interrupt is triggered when an HDMI video stream turns unlocked.

The callback function can update stream down information to the application software. The application software might start a timer and put the system into standby mode if the HDMI 1.4/2.0 Receiver Subsystem remains unlocked for a certain time.

XV_HDMIRXSS_HANDLER_STREAM_INIT

This interrupt is triggered every time a stream is detected and the Video PHY Controller is stabilized for the HDMI 1.4/2.0 Receiver Subsystem to start stream locking.

The callback function needs to perform the following steps:

1. Check the event is for cable connected or cable disconnected.

```
XV_HdmiRxSs *HdmiRxSsPtr = (XV_HdmiRxSs *)CallbackRef;
HdmiRxSsPtr->IsStreamConnected
    1 - Connected
    0 - Disconnected
```

2. Retrieve the video stream information.

```
XVidC_VideoStream *XV_HdmiRxSs_GetVideoStream(
    XV_HdmiRxSs *InstancePtr);
```

3. Calculate HDMI MMCM parameter based on the video stream information received.

```
u32 XVphy_HdmiCfgCalcMmcmParam(XVphy *InstancePtr,
    u8 QuadId,
    XVphy_ChannelId ChId,
    XVphy_DirectionType Dir,
    XVidC_PixelsPerClock Ppc,
    XVidC_ColorDepth Bpc);
```

4. Enable the Video PHY Controller to start MMCM.

```
void XVphy_MmcmStart(XVphy *InstancePtr, u8 QuadId, XVphy_DirectionType Dir);
```

where,

InstancePtr is a pointer to the XVphy core instance.

QuadId is the GT quad ID to operate on.

Dir is an indicator for TX or RX.

Note: QuadId is not used and should be set to 0.

For example:

```
XVphy_MmcmStart(&Vphy, 0, XVPHY_DIR_RX);
```

XV_HDMIRXSS_HANDLER_HDCP_AUTHENTICATE

If HDCP 1.4 or HDCP 2.2 is enabled in the HDMI 1.4/2.0 Receiver Subsystem hardware, this interrupt is triggered when HDCP passes its authentication state.

The callback function can update HDCP authentication status to the application software.

Video PHY Controller Interrupt Handlers for HDMI 1.4/2.0 Receiver Subsystem

There are several interrupt handlers available in the Video PHY Controller driver to hook up with user-defined callback functions to support HDMI 1.4/2.0 Receiver Subsystem functionality. These interrupt handlers are defined in `xvphy.h`:

- XVPHY_HDMI_HANDLER_RXINIT
- XVPHY_HDMI_HANDLER_RXREADY

Callback functions need to be defined in the application code and hooked up with these interrupt handlers.

```
void XVphy_SetHdmiCallback(XVphy *InstancePtr,
                          XVphy_HdmiHandlerType HandlerType,
                          void *CallbackFunc,
                          void *CallbackRef);
```

XVPHY_HDMI_HANDLER_RXINIT

This interrupt is triggered every time the Video PHY Controller detects an HDMI RX reference clock changes.

The callback function needs to perform the following:

1. Initialize a reference clock change process for an HDMI 1.4/2.0 Receiver Subsystem.

```
void XV_HdmiRxSs_RefClockChangeInit(XV_HdmiRxSs *InstancePtr);
```

2. Set Video PHY Controller HDMI RX reference TMDS clock ratio.

```
VphyPtr->HdmiRxTmdsClockRatio = HdmiRxSs.TMDSClockRatio;
```

XVPHY_HDMI_HANDLER_RXREADY

This interrupt is triggered every time the Video PHY Controller RX reset lock is done.

The callback function needs to perform the following:

1. Check the Video PHY Controller PLL Type.

```
XVphy_PllType XVphy_GetPllType(XVphy *InstancePtr,
```

```

u8 QuadId,
XVphy_DirectionType Dir,
XVphy_ChannelId ChId);

```

2. Set the HDMI 1.4/2.0 Receiver Subsystem Video Stream according to the PLL type.

```

XV_HdmiRxSs_SetStream(XV_HdmiRxSs *InstancePtr,
                    u32 Clock,
                    u32 LineRate);

```

Where both Clock and LineRate are from Video PHY Controller data structure.

Follow the steps in [Chapter 5, Example Design](#) to create an example design, which contains all the procedures implemented and can serve as a reference for integrating the HDMI 1.4/2.0 Receiver Subsystem into your system.

Example Use Cases

In this section, some typical use cases are illustrated with how system reacts at run time to certain events and what is expected for you to perform. For actions expected in the callback functions, see [Application Callback Functions](#) for more information.

Use Case 1: Cable Plug In

HPD interrupt is received indicating Cable Connection.

- Callback function registered to [XV_HDMIRXSS_HANDLER_CONNECT](#) Interrupt type is called.

Use Case 2: Cable Plug Out

1. RX Stream Down interrupt is received.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_STREAM_DOWN](#) interrupt type is called.
2. HPD interrupt is received indicating Cable Disconnection.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_CONNECT](#) Interrupt type is called.

Use Case 3: Received Video Stream

1. Video PHY Controller HDMI RX Init interrupt is received.
 - Callback function registered to [XVPHY_HDMI_HANDLER_RXINIT](#) Interrupt type is called.
2. Video PHY Controller HDMI RX Ready interrupt is received.
 - Callback function registered to [XVPHY_HDMI_HANDLER_RXREADY](#) Interrupt type is called.
3. RX Audio Interrupt is received.

- Callback function registered to [XV_HDMIRXSS_HANDLER_AUD](#) Interrupt type is called.
- 4. RX Stream Initialization Interrupt is received.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_STREAM_INIT](#) Interrupt type is called.
- 5. When Video stream is locked, the RX stream up interrupt is received.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_STREAM_UP](#) Interrupt type is called.

Now, the video stream has been detected and you can retrieve the stream information using the provided API:

```
XVidC_VideoStream *XV_HdmiRxSs_GetVideoStream(
    XV_HdmiRxSs *InstancePtr);
```

Use Case 4: Video Stream Change

1. RX Stream Down interrupt is received.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_STREAM_DOWN](#) interrupt type is called.
2. Video PHY Controller HDMI RX Init interrupt is received.
 - Callback function registered to [XVPHY_HDMI_HANDLER_RXINIT](#) Interrupt type is called.
3. Video PHY Controller HDMI RX Ready interrupt is received.
 - Callback function registered to [XVPHY_HDMI_HANDLER_RXREADY](#) Interrupt type is called.
4. RX Audio Interrupt is received.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_AUD](#) Interrupt type is called.
5. RX Stream Initialization Interrupt is received.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_STREAM_INIT](#) Interrupt type is called.
6. When Video stream is locked, the RX stream up interrupt is received.
 - Callback function registered to [XV_HDMIRXSS_HANDLER_STREAM_UP](#) Interrupt type is called.

Now, the video stream has been detected and you can retrieve the stream information using the provided API:

```
XVidC_VideoStream *XV_HdmiRxSs_GetVideoStream(
    XV_HdmiRxSs *InstancePtr);
```

Use Case 5: Receive Infoframe

The Auxiliary InfoFrame received interrupt is received.

Callback function registered to [XV_HDMIRXSS_HANDLER_AUX](#) Interrupt type is called.

Use Case 6: How to Disable Internal EDID

If you do not want to enable the internal EDID support, you can comment out the function `XV_HdmiRx_DdcLoadEdid` in `xv_hdmirxss_coreinit.c`, under function call.

```
int XV_HdmiRxSs_SubcoreInitHdmiRx(XV_HdmiRxSs *HdmiRxSsPtr)
```

Example:

```
// Load EDID  
// XV_HdmiRx_DdcLoadEdid(HdmiRxSsPtr->HdmiRxPtr, HdmiRxSsPtr->EdidPtr,  
// HdmiRxSsPtr->EdidLength);
```

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

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- From the Vivado IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

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- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on Documentation Navigator, see the [Documentation Navigator](#) page on the Xilinx website.

References

These documents provide supplemental material useful with this product guide:

1. *Xilinx Vivado AXI Reference Guide* ([UG1037](#))
2. *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* ([DS892](#))
3. *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* ([DS893](#))
4. *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* ([DS182](#))
5. *Virtex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* ([DS183](#))
6. *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics* ([DS181](#))
7. *Zynq-7000 All Programmable SoC: DC and AC Switching Characteristics* ([DS187](#))
8. *Zynq-7000 All Programmable SoC: DC and AC Switching Characteristics* ([DS191](#))
9. *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* ([DS922](#))
10. *Virtex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* ([DS923](#))
11. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* ([DS925](#))
12. HDMI specifications (www.hdmi.org/manufacturer/specification.aspx)
13. HDCP specifications (www.digital-cp.com/hdcp-specifications)
14. *AXI4-Stream Video IP and System Design Guide* ([UG934](#))
15. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* ([UG994](#))
16. *Vivado Design Suite User Guide: Designing with IP* ([UG896](#))
17. *Vivado Design Suite User Guide: Getting Started* ([UG910](#))
18. *ISE to Vivado Design Suite Migration Guide* ([UG911](#))
19. *KCU105 Board User Guide* ([UG917](#))
20. *Vivado Design Suite User Guide: Programming and Debugging* ([UG908](#))
21. *Vivado Design Suite User Guide: Implementation* ([UG904](#))
22. *AXI Interconnect LogiCORE IP Product Guide* ([PG059](#))
23. *Video PHY Controller LogiCORE IP Product Guide* ([PG230](#))
24. *HDCP v2.2 Product Guide* ([PG249](#))
25. *HDCP v1.4 Product Guide* ([PG224](#))
26. *Video In to AXI4-Stream LogiCORE IP Product Guide* ([PG043](#))

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/20/2017	3.0	<ul style="list-style-type: none"> Updated Example Design steps. Added notes for DP159 Settings. Updated notes for CPU clock requirements.
10/04/2017	3.0	<ul style="list-style-type: none"> Added Example design topology supports (RX-Only, Pass-through). Added Example design VPHY Configuration Support (NI-DRU Enable/Disable, TXPLL selection, RXPLL selection). Added Example design new board supports (ZCU102). Added SDK application supports (RX, Pass-through and HDCP key utility) Added Information for Example design description. Added Software Flow diagram. Added Information if not all audio channels are used. Added Information about Native Video. Added Information about Interlaced Video.
04/05/2017	2.0	<ul style="list-style-type: none"> Removed single pixel per clock support
11/30/2016	2.0	<ul style="list-style-type: none"> Added example design migration notes.
10/05/2016	2.0	<ul style="list-style-type: none"> Added example design flow. Added HPD XGUI option. Added software use cases. Updated Xilinx AUTOMOTIVE APPLICATIONS DISCLAIMER.
06/08/2016	2.0	<ul style="list-style-type: none"> Updated optional video over AXI-Stream support.
04/06/2016	2.0	<ul style="list-style-type: none"> Added Features section in IP Facts. Updated Unsupported Features in Overview chapter. Updated Product Specification chapter. Updated Designing with the Subsystem chapter. Updated Design Flow Steps chapter. Updated Hardware Testing and Video Resolutions sections. Updated Application Software Development appendix.
11/18/2015	1.0	Initial Xilinx release.

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