LogiCORE IP Utility Vector Logic (v2.0)

PB046 (v2.0) April 6, 2016 **Product Brief**

Introduction

The Utility Vector Logic core takes two vector operands and bit-wise applies a logic function to generate a single vector result. This core is intended as glue logic between peripherals. The logical operations supported are AND, OR, XOR and NOT.

Additional Information

See the product page.

Features

- Configurable size of the vectors
- Configurable logical operation on vectors

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™, UltraScale™, Zynq® -7000, Artix®-7, Virtex® -7, Kintex®-7
Supported User Interfaces	N/A
Provided with Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	N/A
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The Utility Vector Logic Core can be configured to perform a logical operation between single bit or vectored signals. The logical operations performed are AND, OR, XOR and NOT.

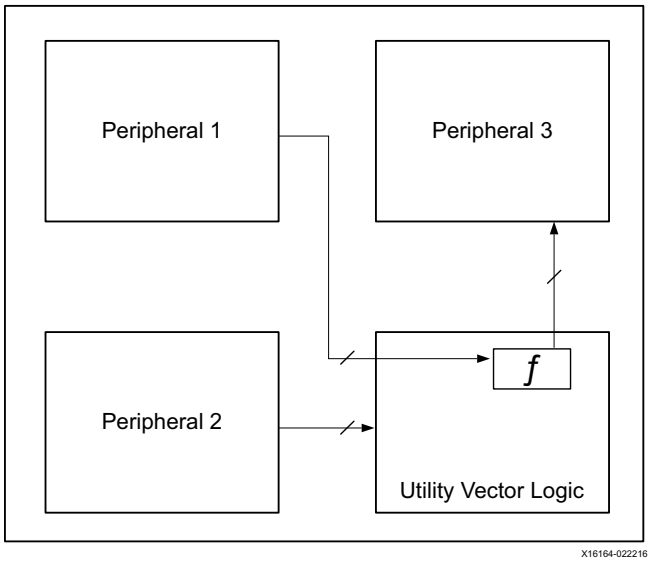

Figure 1: **Utility Vector Logic in a System**

Block Diagram

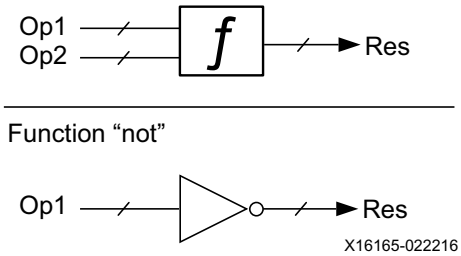

Figure 2: **Utility Vector Logic Block Diagram**

Using Utility Vector Logic in a Block Design

In a block design you instantiate the Utility Vector Logic core by right clicking in the block design canvas and selecting **Add IP** from the context menu.

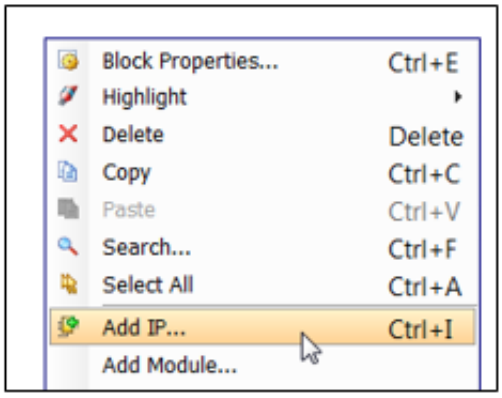

Figure 3: **Adding the Utility Vector Logic in the Block Design Canvas**

In the Search field of the IP Catalog, type **utility,** select the **Utility Vector Logic** core and double-click the core to instantiate it.

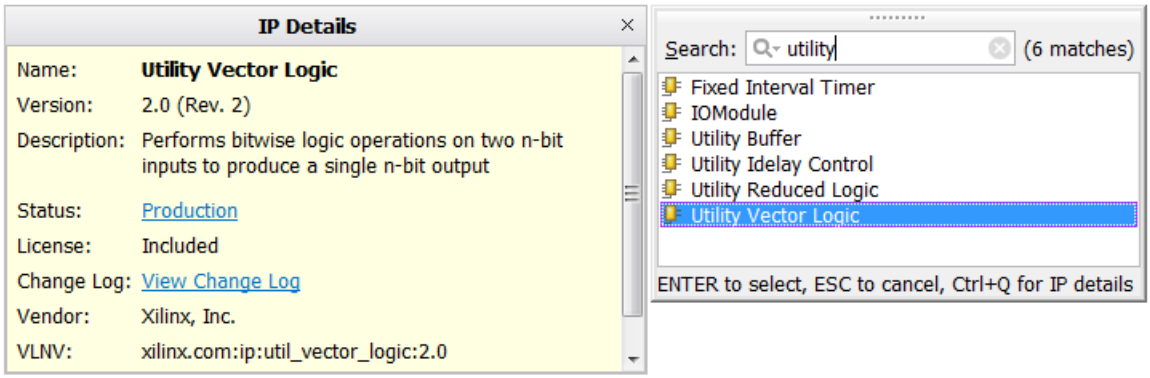

Figure 4: **Search the Utility Vector Logic IP Core in the IP Catalog and Instantiate**

This instantiates the Utility Vector Logic IP core in the design as shown in Figure 5.

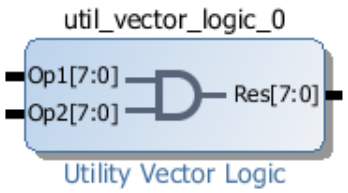

Figure 5: **Utility Vector Logic IP before customization**

Double-click the Utility Vector Logic block to open the Re-customize IP dialog box. When you re-customize the IP and change the operation, the symbol on the block will update accordingly to match the functionality being performed.

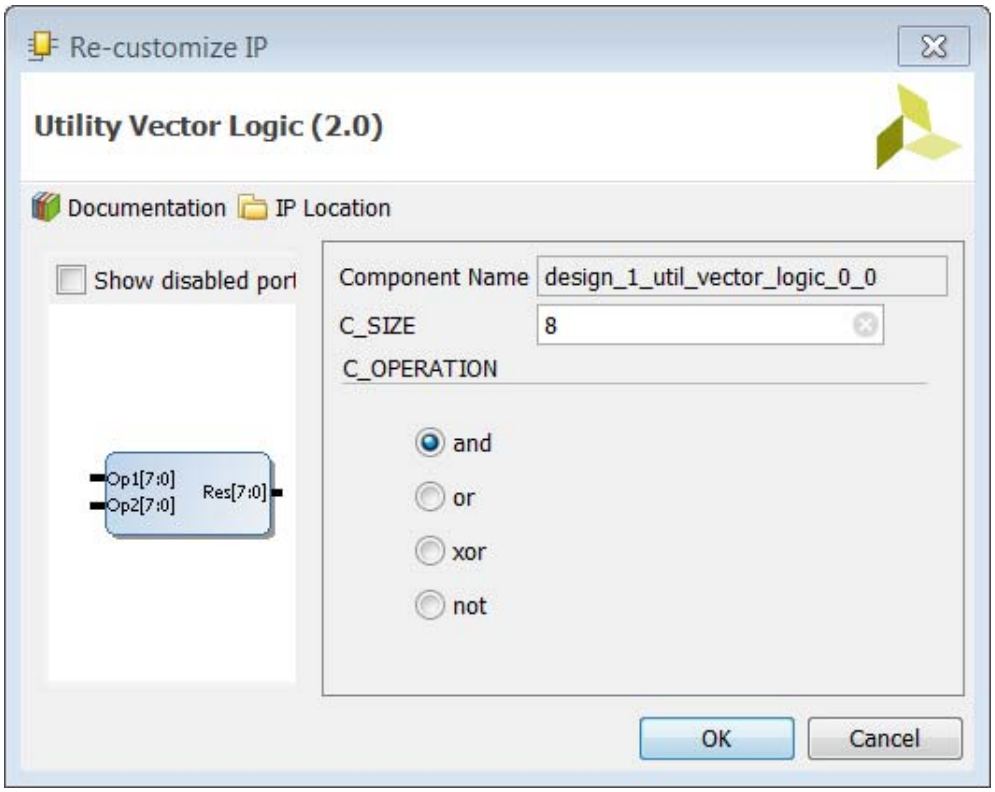

Figure 6: **Re-customize IP Dialog Box**

I/O Signals

Table 1: **Summary of Vector Logic I/O**

Signal	Interface	I/O	Description
Op1	None	I	Operand 1 vector [0: C_SIZE-1]
Op2	None	I	Operand 2 vector [0: C_SIZE-1]. Unused when C_OPERATION ="NOT"
Res	None	O	Result vector [0: C_SIZE-1]

Design Parameters

Table 2: **Utility Vector Logic Parameters**

Parameter	Description	Type
C_OPERATION	The vector operation to perform. The supported operations are: AND, OR, XOR, and NOT.	String
C_SIZE	The size of the vectors. Notice that the width of Op1, Op2 and Res must be equal. The minimum value of this parameter is 1.	Integer

There are no restrictions on allowed parameter combinations for this core.

Parameter-Port Dependencies

Table 3: **Port and Parameter Dependencies**

Name	Affects	Depends	Relationship Description
Design Parameters			
C_SIZE	Op1	0 to C_SIZE-1	Scale width of input bus
C_SIZE	Op2	0 to C_SIZE-1	Scale width of input bus
C_SIZE	Res	0 to C_SIZE-1	Scale width of output bus
Port Signals			
Op1		C_SIZE	Scale width of input bus
Op2		C_SIZE	Scale width of input bus
Res		C_SIZE	Scale width of output bus

Design Implementation

Design Tools

Note: This IP can only be used in the Vivado® IP integrator. It is not designed to be used in an RTL-only design flow within the Vivado Design Suite.

The Utility Vector Logic core is delivered as an HDL file to perform the selected operation.

Target Technology

The target technologies are UltraScale+™, UltraScale™, Zynq®-7000, and 7 series devices.

Device Utilization and Performance Benchmarks

Table 4: **Resource Utilization**

Parameter Value		Device Resources		
C_OPERATION	C_SIZE	Slices	Slice Flip-Flops	Slice LUTs
and	8	5	0	8
or	8	8	0	8
xor	8	5	0	8
not	8	5	0	8

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/06/2016	2.0	Initial Xilinx release of this product brief.

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