Virtex-7 FPGA VC7215 Characterization Kit IBERT

Getting Started Guide

UG970 (Vivado Design Suite v2015.1) April 27, 2015

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/10/2013	1.0	Initial Xilinx release.
10/31/2013	2.0	Updated for Vivado® Design Suite 2013.3. Updated most figures in Chapter 1, VC7215 IBERT Getting Started Guide. Figure 1-30 was renamed *Design Sources File Hierarchy*. Figure 1-31, *Synthesize Out-Of-Context Module* was deleted. The name of the project files ZIP file changed to `rdf0294-vc7215-ibert-2013-3.zip`. Updated Appendix A, Additional Resources and Legal Notices links.
12/18/2013	3.0	Updated for Vivado Design Suite 2013.4. Updated Figure 1-10 through Figure 1-15. Updated Figure 1-19, Figure 1-20, Figure 1-23, Figure 1-27, and Figure 1-28.
04/16/2014	4.0	Updated for Vivado Design Suite 2014.1. Updated most graphics in Chapter 1 from Figure 1-10 on. File lists changed under Extracting the Project Files. The ZIP project file name changed to `rdf0294-vc7215-ibert-2014-1.zip`. The section *Launching Vivado Design Suite* was changed to Setting Up Vivado Design Suite. The section In Case of RX Bit Errors was added.
06/12/2014	5.0	Updated for Vivado Design Suite 2014.2. Updated Figure 1-10, Figure 1-11, Figure 1-19, Figure 1-20, Figure 1-23, Figure 1-27, Figure 1-30, Figure 1-32, Figure 1-33, and Figure 1-35. Updated Viewing GTH Transceiver Operation.
10/08/2014	6.0	Updated for Vivado Design Suite 2014.3. Updated Figure 1-10, Figure 1-11, Figure 1-19, Figure 1-21, Figure 1-23, Figure 1-27, and Figure 1-33. Added device programming information to Starting the SuperClock-2 Module. Updated In Case of RX Bit Errors. C_USER_SCAN_CHAIN* was changed to 3 in Figure 1-33.
11/24/2014	7.0	Updated for Vivado Design Suite 2014.4. The name of the project files ZIP file changed to `rdf0294-vc7215-ibert-2014-4.zip`. Updated Figure 1-10, Figure 1-19, and Figure 1-23.
04/27/2015	2015.1	Updated for Vivado Design Suite 2015.1. The ZIP project file name changed to `rdf0294-vc7215-ibert-2015-1.zip`. Updated Figure 1-4, Figure 1-10, Figure 1-15, Figure 1-17, Figure 1-18, Figure 1-20, Figure 1-23, and Figure 1-27. Version changed to match the software release.

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Chapter 1

VC7215 IBERT Getting Started Guide

Overview

This document provides a procedure for setting up the Virtex®-7 FPGA VC7215 GTH Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration using the Vivado® Design Suite. The designs required to run the IBERT demonstrations are stored in three Secure Digital (SD) memory cards that are provided with the VC7215 board. The demonstration shows the capabilities of the Virtex-7 XC7VX690T FPGA GTH transceiver.

The VC7215 board is described in detail in *VC7215 Virtex-7 FPGA GTH Transceiver Characterization Board User Guide* (UG972) [Ref 1].

The IBERT demonstrations operate one GTH Quad at a time. The procedure consists of:

1. Setting Up the VC7215 Board, page 6
2. Extracting the Project Files, page 7
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4. Configuring the FPGA, page 14
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Requirements

The hardware and software required to run the GTH IBERT demonstrations are:

- VC7215 Virtex-7 FPGA GTH Transceiver Characterization Board. Includes:
  - Three SD cards labeled IBERT #1, IBERT #2, and IBERT#3 containing the IBERT demonstration designs
  - One Samtec BullsEye cable
  - Eight SMA female-to-female (F-F) adapters
  - Six 50Ω SMA terminators
  - Two GTH transceiver power supply modules (installed on board)
  - SuperClock-2 module, Rev 1.0 (installed on board)
  - 12V DC power adapter
  - USB cable, standard-A plug to Micro-B plug
- Host PC with:
  - SD card reader
  - USB ports
- Vivado Design Suite 2015.1

The hardware and software required to rebuild the IBERT demonstration designs are:

- Vivado Design Suite 2015.1
- PC with a version of the Windows operating system supported by Vivado Design Suite

Setting Up the VC7215 Board

This section describes how to set up the VC7215 board.

CAUTION! *The VC7215 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

When the VC7215 board ships from the factory, it is configured for the GTH IBERT demonstrations described in this document. If the board has been re-configured it must be returned to the default setup before running the IBERT demonstrations.

1. Move all jumpers and switches to their default positions. The default jumper and switch positions are listed in *VC7215 Virtex-7 FPGA GTH Transceiver Characterization Board User Guide* (UG972) [Ref 1].
2. Install the two GTH transceiver power modules by plugging them into connectors J66 and J97, and connectors J10 and J72.
3. Install the SuperClock-2 module:
   a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the SUPERCLOCK-2 MODULE interface of the VC7215 board.
   b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the VC7215 board.
   c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18, and place another jumper across Si570 INH header J11.
   d. Screw down a 50Ω SMA terminator onto each of the six unused Si5368 clock output SMA connectors: J7, J8, J12, J15, J16 and J17.

Extracting the Project Files

The Vivado project files required to run the IBERT demonstrations are located in `rdf0294-vc7215-ibert-2015-1.zip` on the SD card provided with the VC7215 board. They are also available online at the Virtex-7 FPGA VC7215 Characterization Kit website.

The ZIP file contains these files:

- BIT files
  - 20 BIT files, one for each of the board's 20 Quads (`vc7215_ibert_qxxx_325.bit`)
- Probe files
  - 20 probe files, one for each of the board's 20 QuadS (`vc7215_qxxx_325.ltx`)
- The complete project files
- TCL scripts
  - `add_scm2.tcl`
  - `setup_scm2_325_00.tcl`

The Tcl scripts are used to help merge the IBERT and SuperClock-2 source code (described in Creating the GTH IBERT Core, page 29) and to set up the SuperClock-2 module to run at 325.00 MHz (described in Setting Up Vivado Design Suite, page 16).

To copy the files from the Secure Digital memory card:

1. Connect the Secure Digital memory card labeled IBERT #1 to the host computer.
2. Locate the file `rdf0294-vc7215-ibert-2015-1.zip` on the Secure Digital memory card.
3. Unzip the files to a working directory on the host computer.

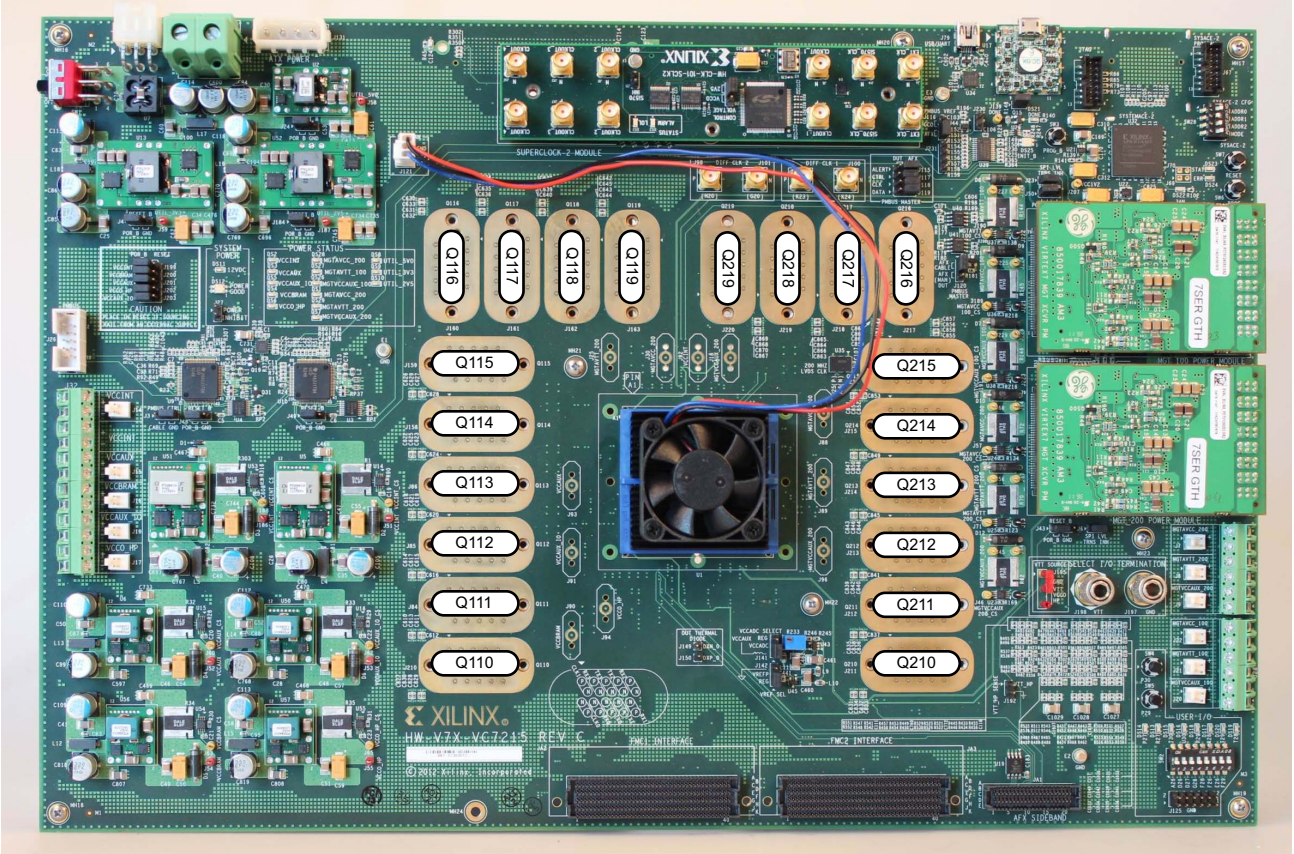
Running the GTH IBERT Demonstration

The GTH IBERT demonstration operates one GTH Quad at a time. This section describes how to test GTH Quad 115. The remaining GTH Quads are tested following a similar series of steps.

Connecting the GTH Transceivers and Reference Clocks

Figure 1-1 shows the locations for all GTH transceiver Quads on the VC7215 board.

Note: Figure 1-1 is for reference only and might not reflect the current revision of the board.



UG970_c1_01_060413

Figure 1-1: **GTH Quad Locations**

All GTH transceiver pins and reference clock pins are routed from the FPGA to a connector pad which interfaces with Samtec BullsEye connectors. Figure 1-2 **A** shows the connector pad. Figure 1-2 **B** shows the connector pinout.

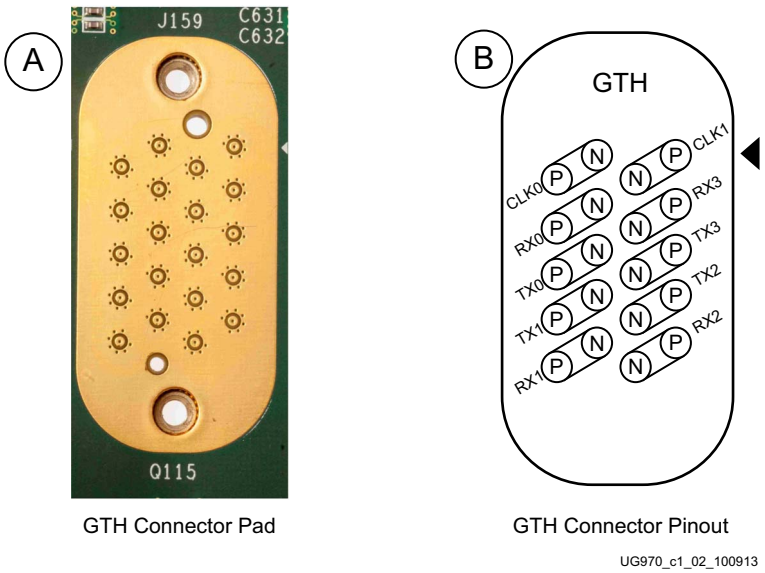


Figure 1-2: **A – GTH Connector Pad. B – GTH Connector Pinout**

The SuperClock-2 module provides LVDS clock outputs for the GTH transceiver reference clocks in the IBERT demonstrations. Figure 1-3 shows the locations of the differential clock SMA connectors on the clock module which can be connected to the reference clock cables.

Note: The image in Figure 1-3 is for reference only and might not reflect the current revision of the board.

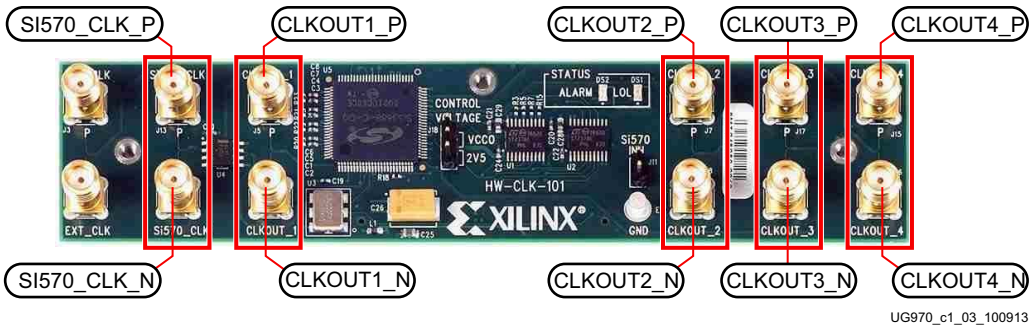


Figure 1-3: **SuperClock-2 Module Output Clock SMA Locations**

The four SMA pairs labeled CLKOUT provide LVDS clock outputs from the Si5368 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled Si570_CLK provides LVDS clock output from the Si570 programmable oscillator on the clock module.

Note: The Si570 oscillator does not support LVDS output on the Rev B and earlier revisions of the SuperClock-2 module.

For the GTH IBERT demonstration, the output clock frequencies are preset to 325.00 MHz. For more information regarding the SuperClock-2 module, refer to *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770) [Ref 2].

Attach the GTH Quad Connector

Before connecting the BullsEye cable assembly to the board, firmly secure the blue elastomer seal provided with the cable assembly to the bottom of the connector housing if it is not already inserted (see Figure 1-4).

Note: Figure 1-4 is for reference only and might not reflect the current version of the connector.

Figure 1-4: **BullsEye Connector with Elastomer Seal**

Attach the Samtec BullsEye connector to GTH Quad 115 (Figure 1-5), aligning the two indexing pins on the bottom of the connector with the guide holes on the board. Hold the connector flush with the board and fasten it by tightening the two captive screws.

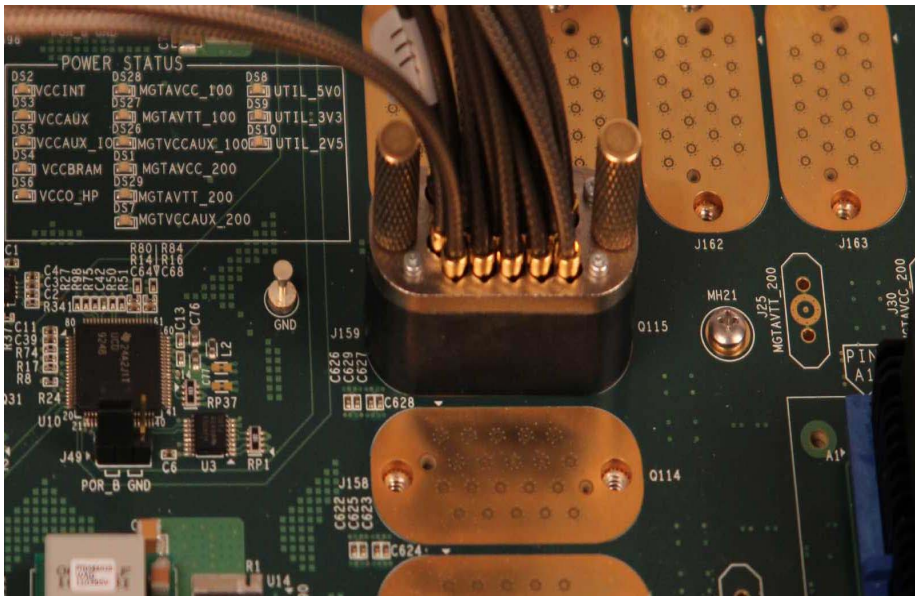


Figure 1-5: **BullsEye Connector Attached to Quad 115**

GTH Transceiver Clock Connections

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the CLK0 reference clock inputs. Connect these cables to the SuperClock-2 module as follows:

- CLK0_P coax cable → SMA connector J5 (CLKOUT1_P) on the SuperClock-2 module
- CLK0_N coax cable → SMA connector J6 (CLKOUT1_N) on the SuperClock-2 module

Note: Any one of the five differential outputs from the SuperClock-2 module can be used to source the GTH reference clock. CLKOUT1_P and CLKOUT1_N are used here as an example.

GTH TX/RX Loopback Connections

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the four receivers (RX0, RX1, RX2 and RX3) and the four transmitters (TX0, TX1, TX2 and TX3). Use eight SMA female-to-female (F-F) adapters (Figure 1-6), to connect the transmit and receive cables as shown in Figure 1-7 and detailed below:

- TX0_P → SMA F-F Adapter → RX0_P
- TX0_N → SMA F-F Adapter → RX0_N
- TX1_P → SMA F-F Adapter → RX1_P
- TX1_N → SMA F-F Adapter → RX1_N
- TX2_P → SMA F-F Adapter → RX2_P
- TX2_N → SMA F-F Adapter → RX2_N
- TX3_P → SMA F-F Adapter → RX3_P
- TX3_N → SMA F-F Adapter → RX3_N

Note: To ensure good connectivity, it is recommended that the adapters be secured with a wrench; however, do not over tighten the SMAs.

Figure 1-6: **SMA F-F Adapter**

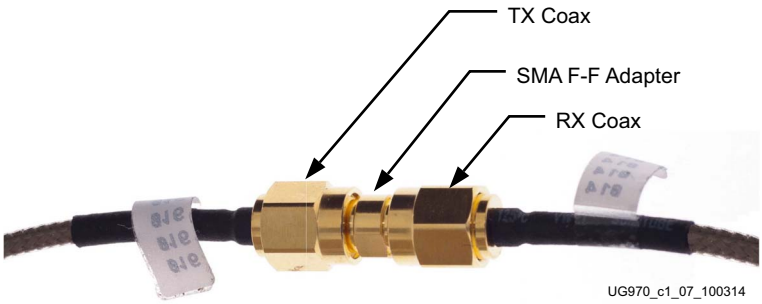


Figure 1-7: **TX-To-RX Loopback Connection Example**

Figure 1-8 shows the VC7215 board with the cable connections required for the Quad 115 GTH IBERT demonstration.

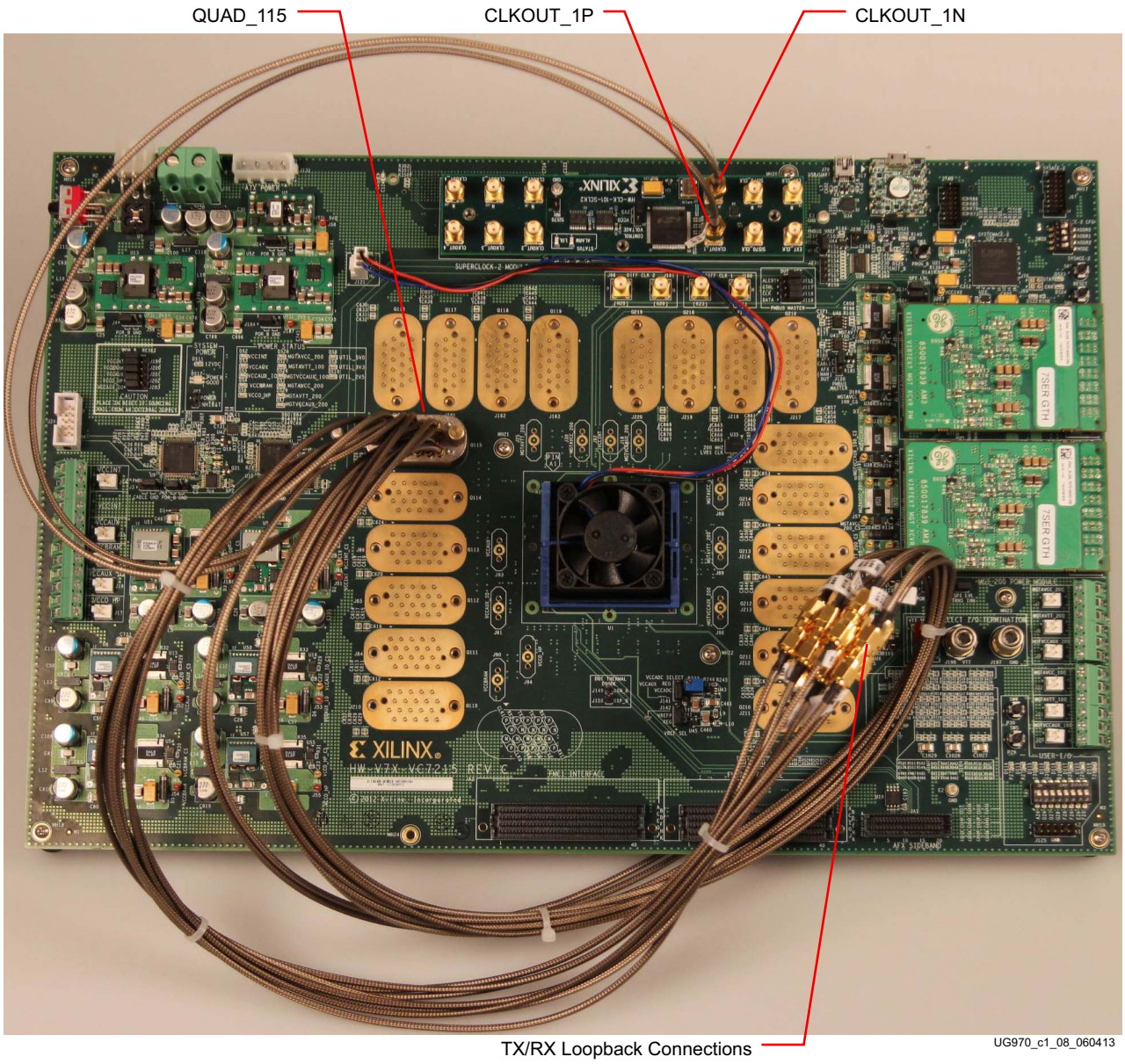


Figure 1-8: **Cable Connections for Quad 115 GTH IBERT Demonstration**

Configuring the FPGA

This section describes how to configure the FPGA using an SD card included with the board. The FPGA can also be configured through Vivado Design Suite using the `.bit` files available on the SC card or online (as collection `rdf0294-vc7215-ibert-2015-1.zip`) at the Virtex-7 FPGA VC7215 Characterization Kit website.

To configure from the SD card:

1. Insert the SD card labeled IBERT #1 provided with the VC7215 board into the SD card reader slot located on the bottom side (upper right corner) of the VC7215 board.
2. Plug the 12V output from the power adapter into connector J2 on the VC7215 board.
3. Connect the host computer to the VC7215 board using a standard-A plug to Micro-B plug USB cable. The standard-A plug connects to a USB port on the host computer and the Micro-B plug connects to U17, the Digilent USB JTAG configuration port on the VC7215 board.
4. Select the GTH IBERT demonstration with the System ACE™ SD controller SYSACE-2 CFG switch, SW28. The setting on this 4-bit DIP switch (Figure 1-9) selects the file used to configure the FPGA. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. For the Quad 115 GTH IBERT demonstration, set ADR2 = ON, ADR1 = OFF, and ADR0 = ON. The MODE bit (switch position 4) is not used and can be set either ON or OFF.

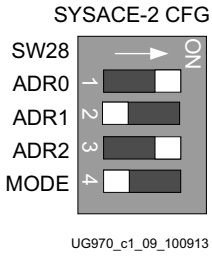


Figure 1-9: **Configuration Address DIP Switch (SW28)**

There is one IBERT demonstration design for each GTH Quad on the VC7215 board, for a total of twenty IBERT designs. An additional design is provided to demonstrate the USB/UART interface (details of this demonstration are described in the `README` file on the SD card). All twenty designs are organized and stored on three SD cards as shown in Table 1-1.

Table 1-1: **SD Card Contents and Configuration Addresses**

SD Card	Demonstration Design	ADR2	ADR1	ADR0
IBERT #1	GTH Quad 110	OFF	OFF	OFF
	GTH Quad 111	OFF	OFF	ON
	GTH Quad 112	OFF	ON	OFF
	GTH Quad 113	OFF	ON	ON
	GTH Quad 114	ON	OFF	OFF
	GTH Quad 115	ON	OFF	ON
	GTH Quad 116	ON	ON	OFF
	GTH Quad 117	ON	ON	ON
IBERT #2	GTH Quad 118	OFF	OFF	OFF
	GTH Quad 119	OFF	OFF	ON
	GTH Quad 210	OFF	ON	OFF
	GTH Quad 211	OFF	ON	ON
	GTH Quad 212	ON	OFF	OFF
	GTH Quad 213	ON	OFF	ON
	GTH Quad 214	ON	ON	OFF
	GTH Quad 215	ON	ON	ON
IBERT #3	GTH Quad 216	OFF	OFF	OFF
	GTH Quad 217	OFF	OFF	ON
	GTH Quad 218	OFF	ON	OFF
	GTH Quad 219	OFF	ON	ON
	USB/UART	ON	OFF	OFF
	LED Scroll	ON	OFF	ON
	Pushbuttons	ON	ON	OFF
	DIP Switches	ON	ON	ON

5. Place the main power switch SW1 to the ON position.

Setting Up Vivado Design Suite

1. Start Vivado Design Suite on the host computer and click **Flow > Open Hardware Manager** (shown in Figure 1-10).

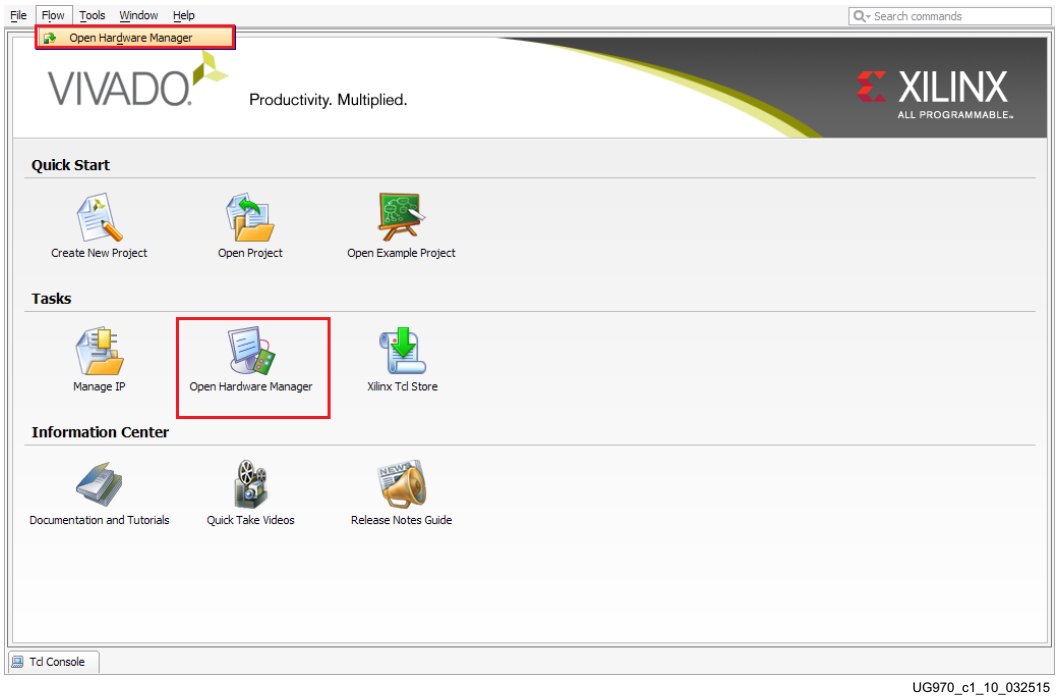


Figure 1-10: **Vivado Design Suite, Open Hardware Manager**

2. In the Hardware Manager window, click **Open New Target** (highlighted in Figure 1-11).

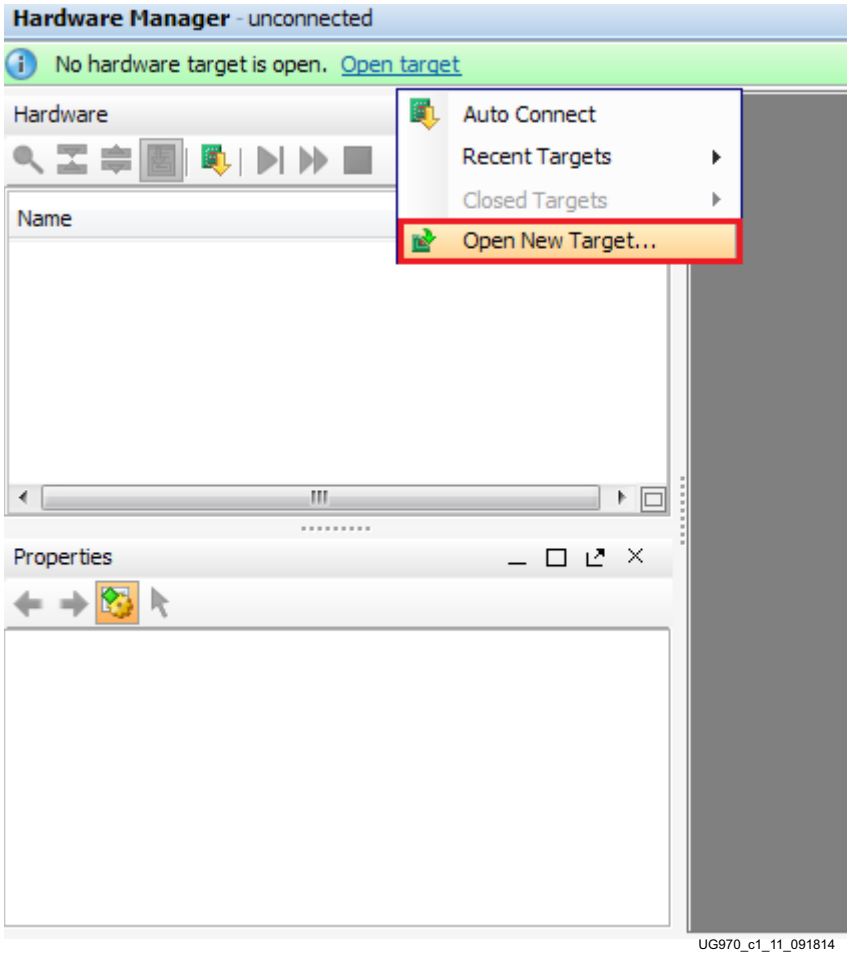


Figure 1-11: **Open a New Hardware Target**

3. An Open Hardware Target wizard pops up. Click **Next** on the first window.
4. In the Hardware Server Settings window, select **Local server (target is on local machine)**. Click **Next** to open the server and connect to the Xilinx TCF JTAG cable.

5. In the Select Hardware Target window, the `xilinx_tcf` cable appears under **Hardware Targets**. The JTAG chain contents of the selected cable appear under the Hardware Devices window (Figure 1-12). Select the **xilinx_tcf** target and keep the JTAG Clock Frequency at the default value (15 MHz). Cick **Next**.

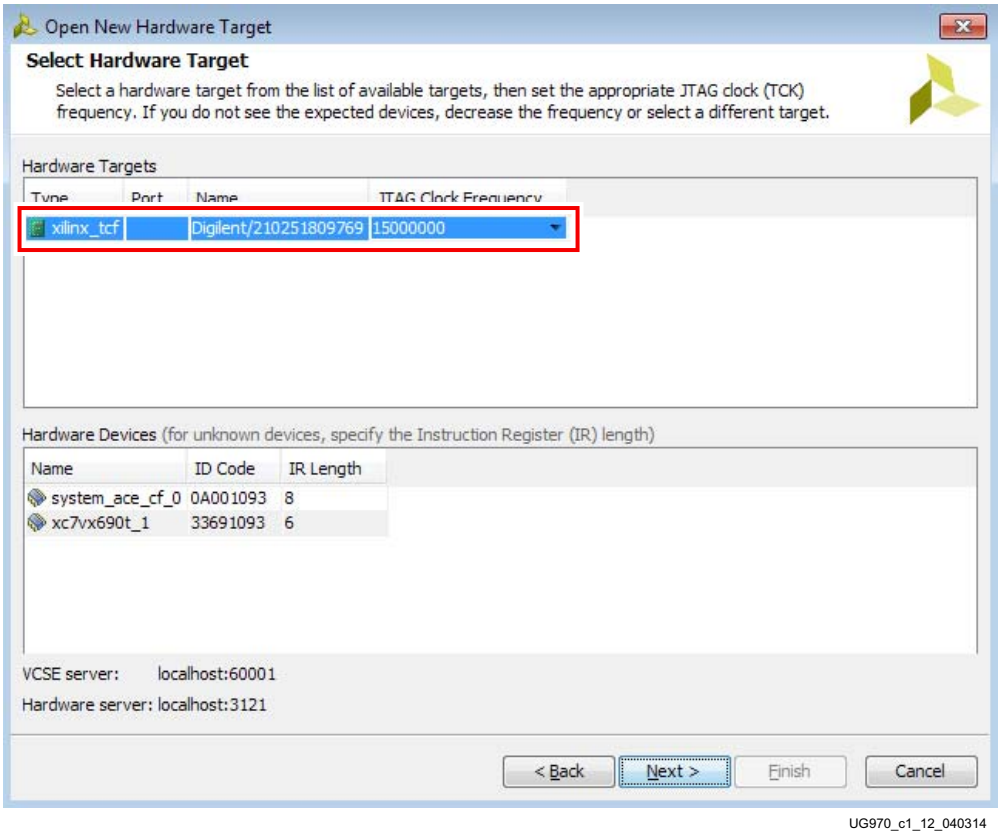


Figure 1-12: **Select Hardware Target**

6. In the Open Hardware Target Summary window, click **Finish**. The wizard closes and the Vivado Design Suite opens the hardware target.

Starting the SuperClock-2 Module

The IBERT demonstration designs use an integrated VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components:

- An always-on Si570 crystal oscillator
- An Si5368 jitter-attenuating clock multiplier.

Outputs from either device can be used to drive the transceiver reference clocks.

To start the SuperClock-2 module:

1. The Vivado Design Suite Hardware Manager window shows the System ACE™ SD Controller and the XC7VX690T device. The XC7VX690T_1 device is reported as programmed. In the Hardware Device Properties window, enter the file path to the Q115 probes file (`vc7215_ibert_q115_debug_nets.ltx`) in the extracted IBERT files from the SD card (Figure 1-13).

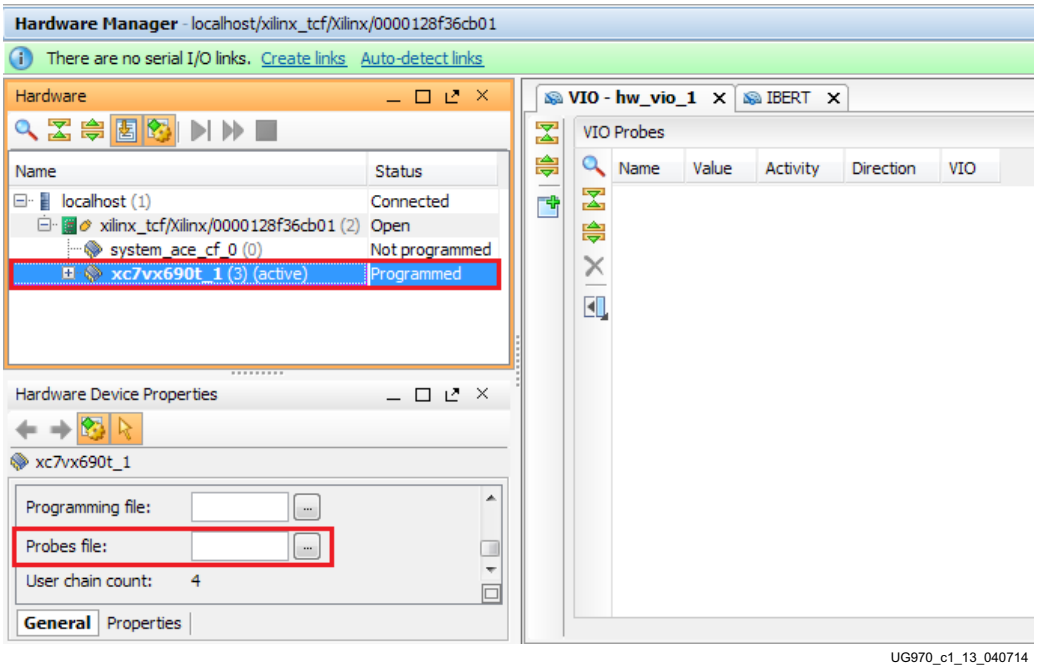


Figure 1-13: **Adding the Probes File**

2. In the Hardware window, right-click **XC7VX690T_1** and select **Refresh Device** (Figure 1-14).

   Note: If the FPGA was not programmed using the SD card, provide both the programming and the probes files, and select **Program Device**.

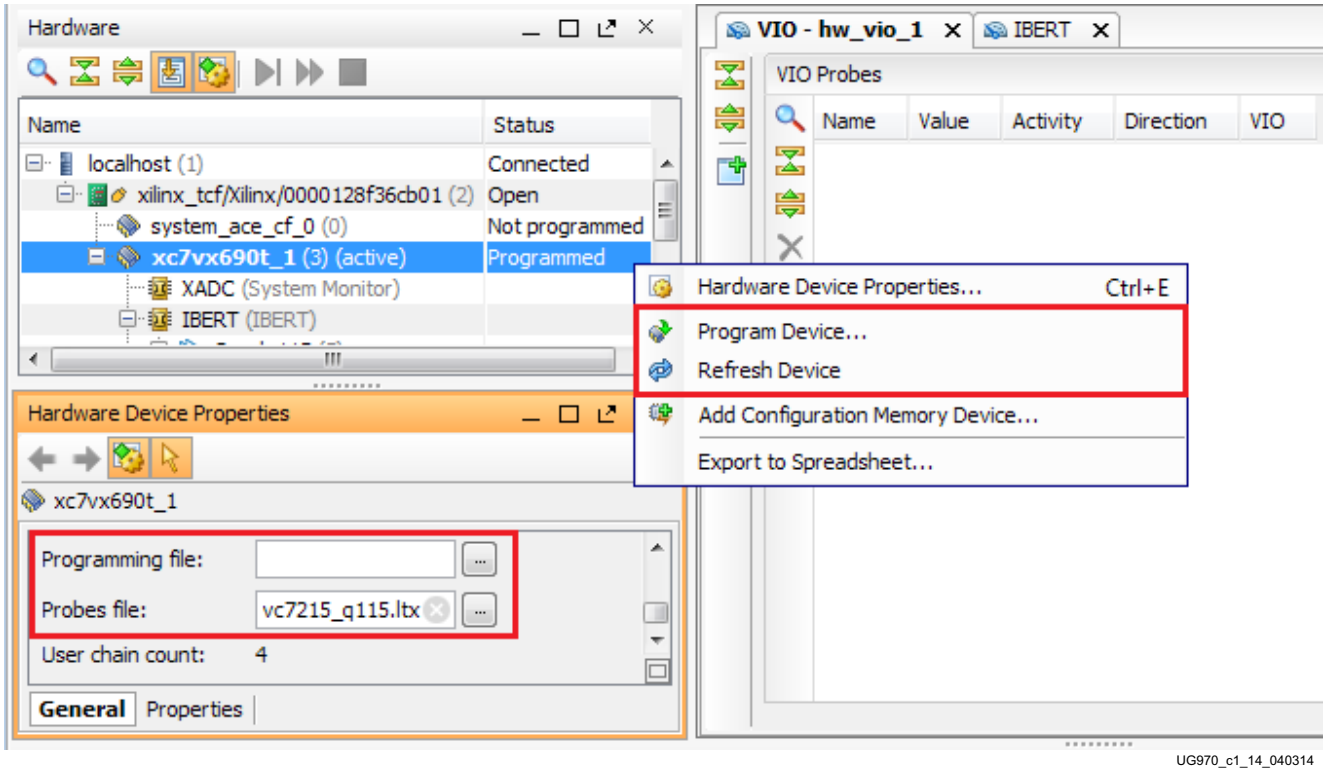


Figure 1-14: **Refresh/Program Device**

3. The Vivado tool reports that the XC7VX690T is programmed and displays the SuperClock-2 VIO core and the IBERT core. To configure the SuperClock-2 module, select **Tools > Run Tcl Script** (Figure 1-15). In the following Run Script window, navigate to the `setup_scm2_325_00.tcl` script in the extracted files and click **OK**.

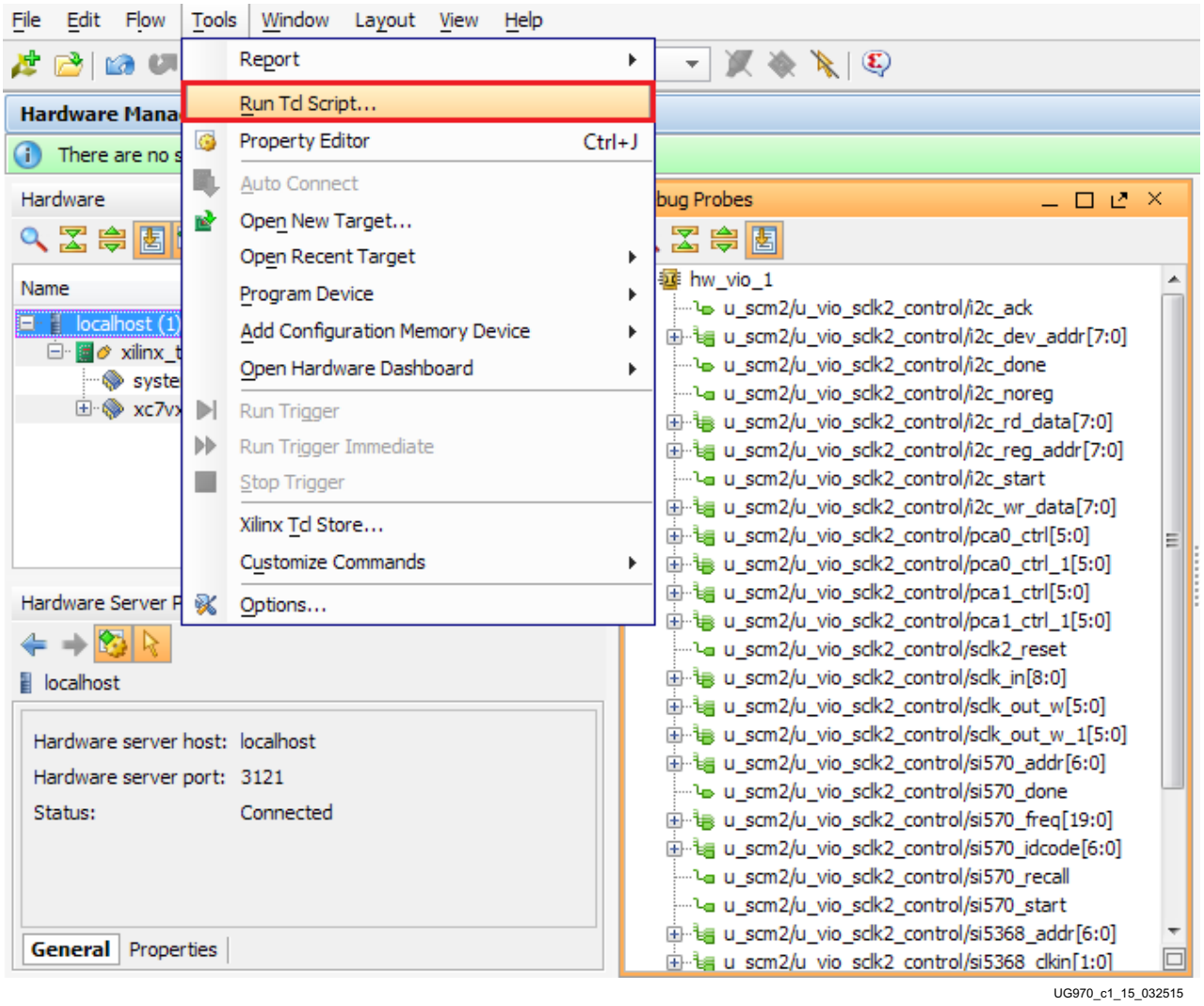


Figure 1-15: **Run Tcl Script**

4. To view the SuperClock-2 settings in the VIO core, select the probe signal from the Debug Probes window and drag it to the VIO-hw_vio_1 window. For example, the frequencies, ROM addresses, and start signals are selected (Figure 1-16).

   Note: The ROM address values for the Si5368 and Si570 devices (that is, si5368_addr[6:0] and si570_addr[6:0]) are preset to 3 to produce an output frequency of 325.00 MHz. Entering a different ROM address changes the reference clock(s) frequency. The complete list of pre-programmed SuperClock-2 frequencies and their associated ROM addresses is provided in Table 1-2.

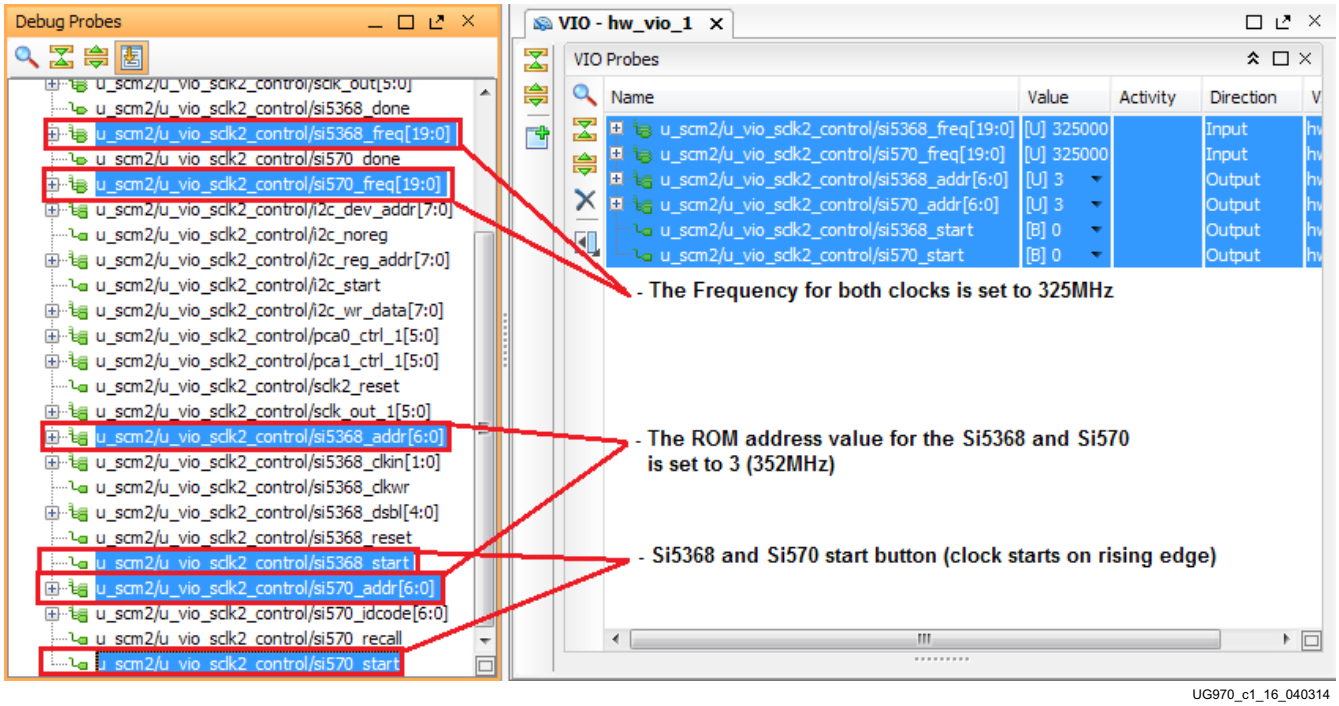


Figure 1-16: **SuperClock-2 Module VIO Core**

5. To view the GTH transceiver operation, click **Layout > Serial I/O Analyzer.** From the top of the Hardware Manager window, select **Auto-Detect Links** to display all available links automatically. Links can also be created manually in the Links window by right-clicking and selecting **Create Links,** or by clicking the **Create Links** button (Figure 1-17).

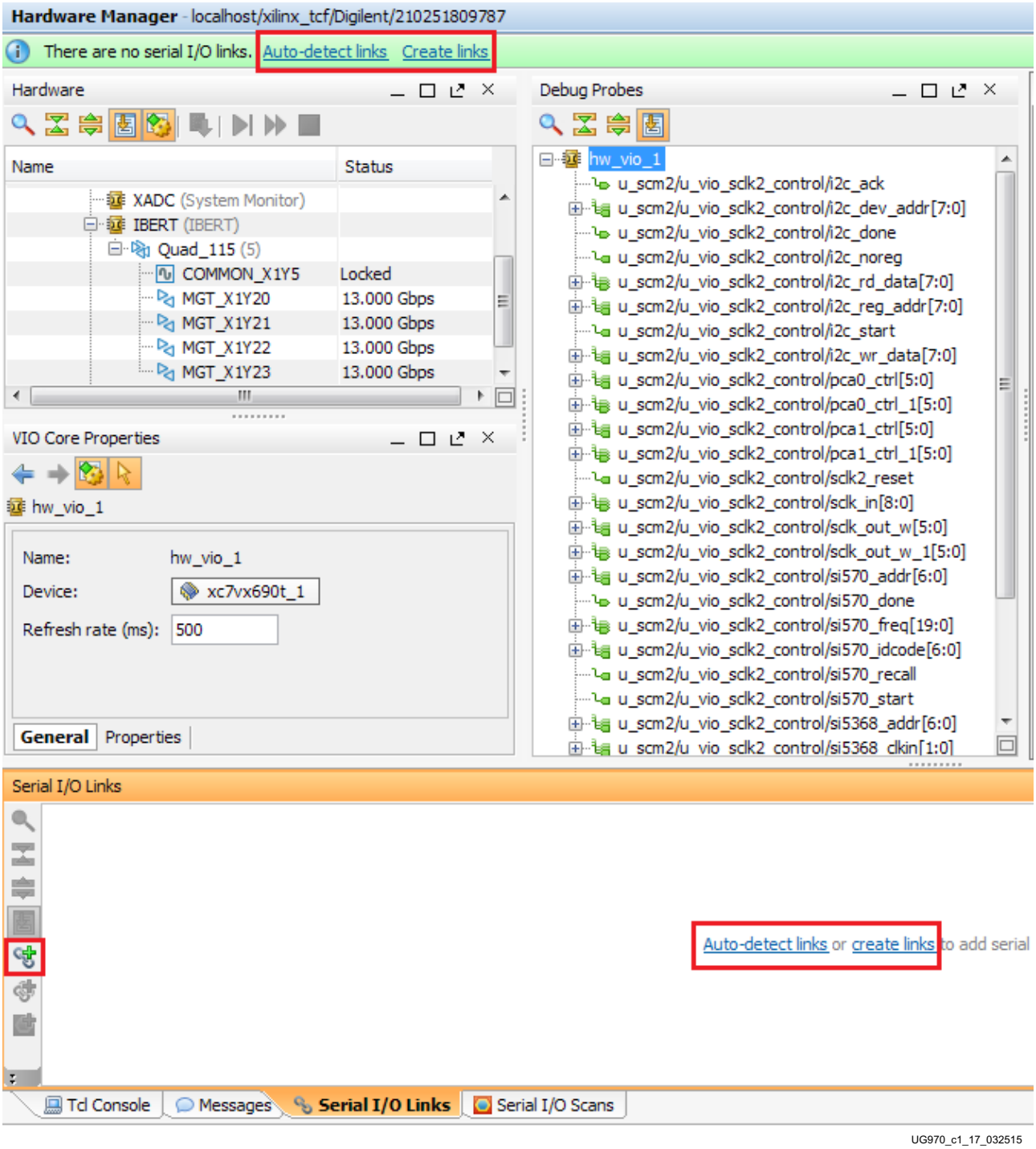


Figure 1-17: **Serial I/O Analyzer - Create Links...**

6. If links are created manually, the Create Links window is displayed. The options in this window are used to link any TX GT to any RX GT. To create links, select the TX GT and RX GT from the two lists. Press the **Add Link** button. For this project, connect the following links:

   MGT_X1Y20/TX to MGT_X1Y20/RX

   MGT_X1Y21/TX to MGT_X1Y21/RX

   MGT_X1Y22/TX to MGT_X1Y22/RX

   MGT_X1Y23/TX to MGT_X1Y23/RX

   This linking is shown in Figure 1-18.

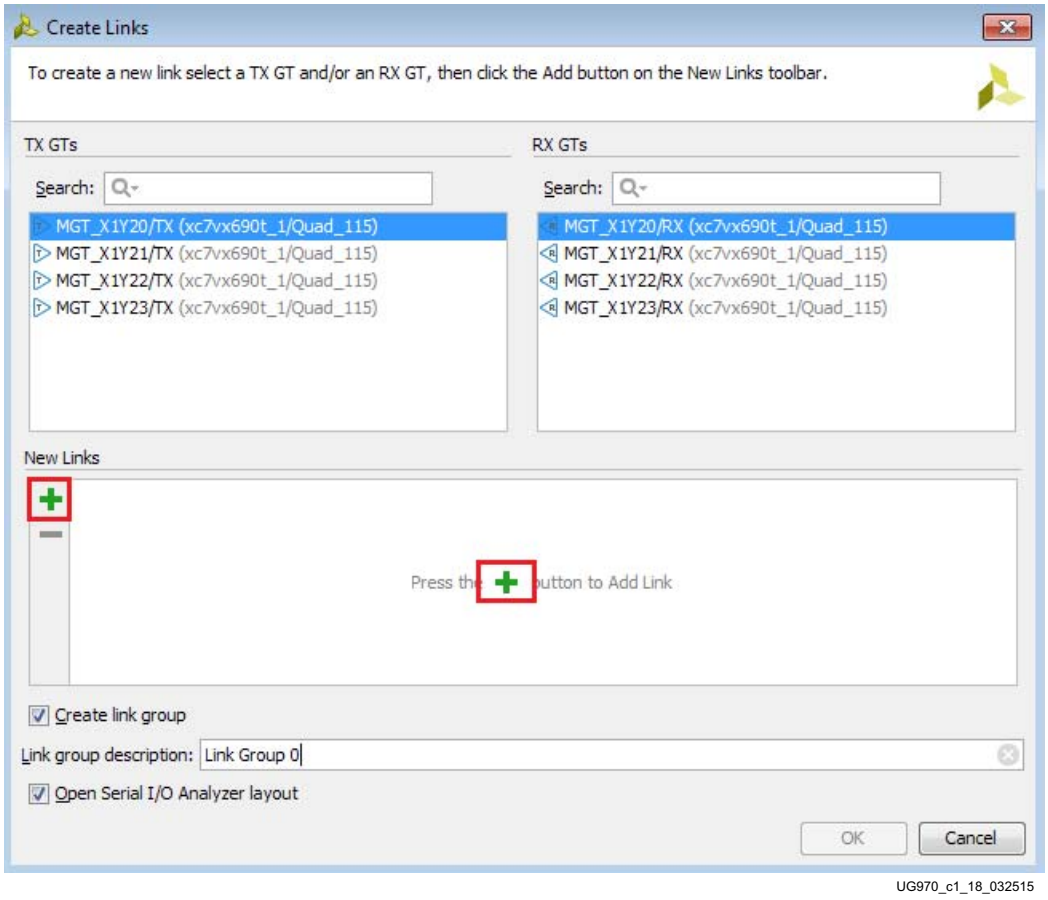


Figure 1-18: **Create Links Window**

Viewing GTH Transceiver Operation

After completing step 6 in Starting the SuperClock-2 Module, the IBERT demonstration is configured and running. The status and test settings are displayed on the Links tab in the Links window shown in Figure 1-19.

Note the line rate and error count:

- The line rate for all four GTH transceivers is 13.0 Gb/s (see Status in Figure 1-19).
- Verify that there are no bit errors.

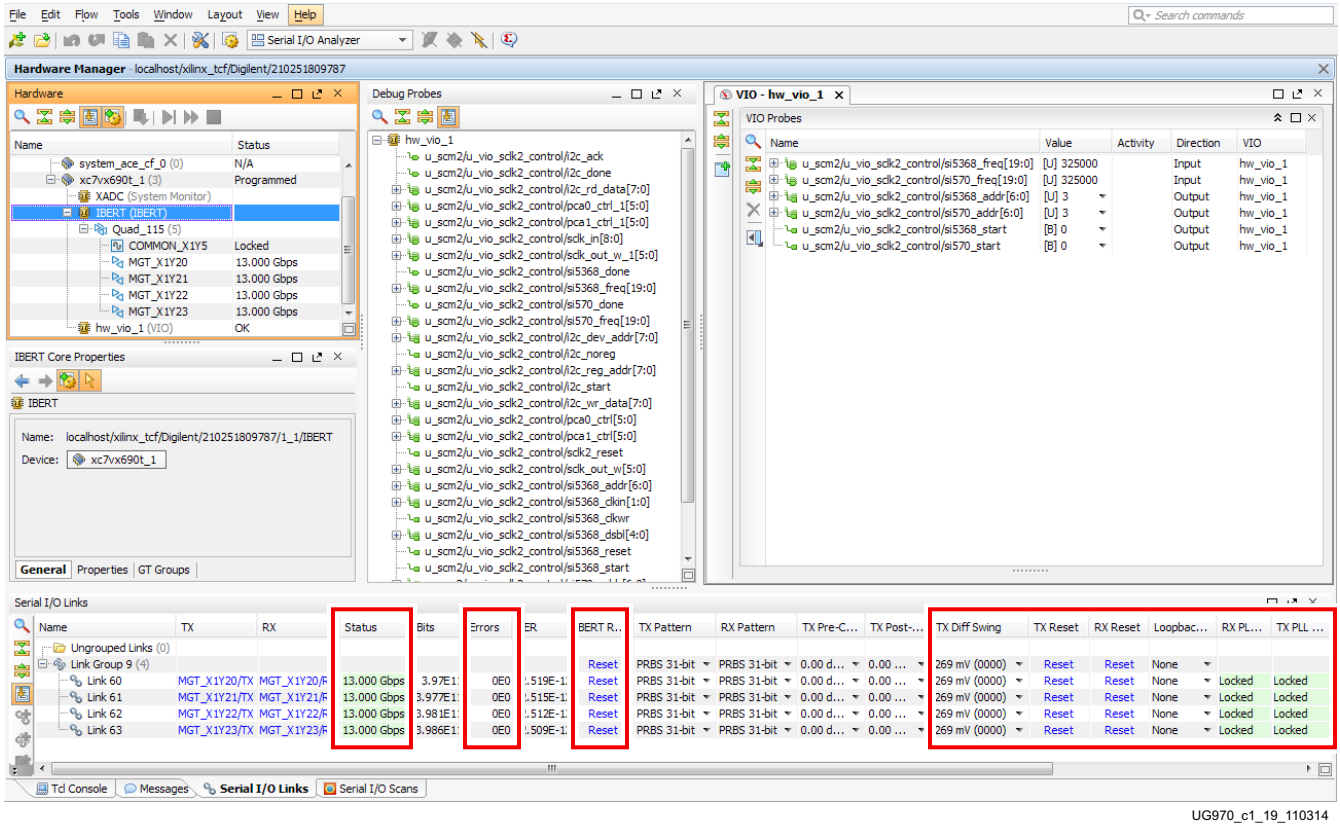


Figure 1-19: **Serial I/O Analyzer Links**

In Case of RX Bit Errors

If there are initial bit errors after linking, or as a result of changing the TX or RX pattern, click the respective **BERT Reset** button to zero the count.

If the MGT Link Status shows No Link for one or more transceivers:

- Make sure the blue elastomer seal is connected to the bottom of the BullsEye cable and the cable is firmly connected and flush on the board.
- Increase the TX differential swing of the transceiver (to compensate for any loss due to PCB process variation).
- Click the respective **TX Reset** button followed by **BERT Reset**.

Additional information on the Vivado Design Suite and IBERT core can be found in *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 3] and *LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTH Transceivers Product Guide for Vivado Design Suite* (PG152) [Ref 4].

Closing the IBERT Demonstration

To stop the IBERT demonstration:

1. Close the Vivado Design Suite application by selecting **File > Exit**.
2. Place the main power switch SW1 in the off position.

SuperClock-2 Frequency Table

Table 1-2 lists the addresses for the frequencies that are programmed into the SuperClock-2 read-only-memory (ROM).

Table 1-2: **Si570 and Si5368 Frequency Table**

Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)
0	100GE/40GE/10GE	161.130	30	OBSAI	307.200	60	XAUI	156.250
1	Aurora	81.250	31	OBSAI	614.400	61	XAUI	312.500
2	Aurora	162.500	32	OC-48	19.440	62	XAUI	625.000
3	Aurora	325.000	33	OC-48	77.760	63	Generic	66.667
4	Aurora	650.000	34	OC-48	155.520	64	Generic	133.333
5	CE111	173.370	35	OC-48	311.040	65	Generic	166.667
6	CPRI	61.440	36	OC-48	622.080	66	Generic	266.667

Table 1-2: **Si570 and Si5368 Frequency Table *(Cont'd)***

Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)
7	CPRI	122.880	37	OTU-1	166.629	67	Generic	333.333
8	CPRI	153.630	38	OTU-1	333.257	68	Generic	533.333
9	CPRI	245.760	39	OTU-1	666.514	69	Generic	644.000
10	CPRI	491.520	40	OTU-1	666.750	70	Generic	666.667
11	Display Port	67.500	41	OTU-2	167.330	71	Generic	205.000
12	Display Port	81.000	42	OTU-2	669.310	72	Generic	210.000
13	Display Port	135.000	43	OTU-3	168.050	73	Generic	215.000
14	Display Port	162.000	44	OTU-4	174.690	74	Generic	220.000
15	Fibrechannel	106.250	45	PCIe	100.000	75	Generic	225.000
16	Fibrechannel	212.500	46	PCIe	125.000	76	Generic	230.000
17	Fibrechannel	425.000	47	PCIe	250.000	77	Generic	235.000
18	GigE	62.500	48	SATA	75.000	78	Generic	240.000
19	GigE	125.000	49	SATA	150.000	79	Generic	245.000
20	GigE	250.000	50	SATA	300.000	80	Generic	250.000
21	GigE	500.000	51	SATA	600.000	81	Generic	255.000
22	GPON	187.500	52	SDI	74.250	82	Generic	260.000
23	Interlaken	132.813	53	SDI	148.500	83	Generic	265.000
24	Interlaken	195.313	54	SDI	297.000	84	Generic	270.000
25	Interlaken	265.625	55	SDI	594.000	85	Generic	275.000
26	Interlaken	390.625	56	SMPTE435M	167.063	86	Generic	280.000
27	Interlaken	531.250	57	SMPTE435M	334.125	87	Generic	285.000
28	OBSAI	76.800	58	SMPTE435M	668.250	88	Generic	290.000
29	OBSAI	153.600	59	XAUI	78.125	89	Generic	295.000
90	Generic	300.000	103	Generic	365.000	116	Generic	430.000
91	Generic	305.000	104	Generic	370.000	117	Generic	435.000
92	Generic	310.000	105	Generic	375.000	118	Generic	440.000
93	Generic	315.000	106	Generic	380.000	119	Generic	445.000
94	Generic	320.000	107	Generic	385.000	120	Generic	450.000
95	Generic	325.000	108	Generic	390.000	121	Generic	455.000
96	Generic	330.000	109	Generic	395.000	122	Generic	460.000
97	Generic	335.000	110	Generic	400.000	123	Generic	465.000

Table 1-2: **Si570 and Si5368 Frequency Table *(Cont'd)***

Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)	Address	Protocol	Frequency (MHz)
98	Generic	340.000	111	Generic	405.000	124	Generic	470.000
99	Generic	345.000	112	Generic	410.000	125	Generic	475.000
100	Generic	350.000	113	Generic	415.000	126	Generic	480.000
101	Generic	355.000	114	Generic	420.000	127	Generic	485.000
102	Generic	360.000	115	Generic	425.000			

Creating the GTH IBERT Core

Vivado Design Suite 2015.1 is required to rebuild the designs shown here.

This section provides a procedure to create a single Quad GTH IBERT core with integrated SuperClock-2 controller. The procedure assumes Quad 115 and 13.0 Gb/s line rate, but cores for any of the GTH Quads with any supported line rate can be created following the same series of steps.

For more details on generating IBERT cores, refer to *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 3].

1. Start the Vivado Design Suite.
2. In the Vivado window, click the **Manage IP** icon highlighted in Figure 1-20, then select **New IP Location**.

Figure 1-20: **Initial Window, Vivado Design Suite**

3. When the Create a New Customized IP Location dialog box opens (not shown), click **Next**.

4. In the Manage IP Settings window, select a part by clicking the **(...)** button next to the **Part** field. A Select Device window pops up. Use the drop-down menu items to narrow the choices. Select the **xc7vx690tffg1927-3** device (Figure 1-21). Click **OK**.

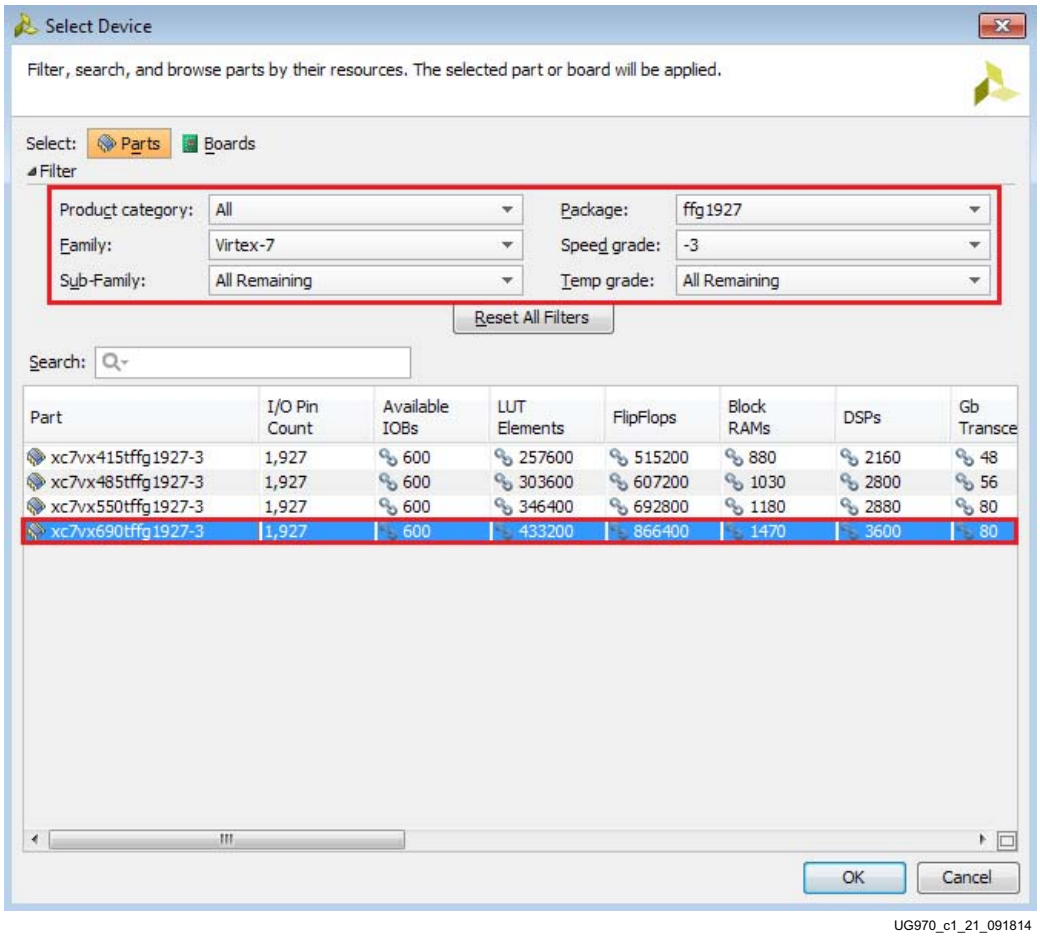


Figure 1-21: **Select Device**

5. Back on the Manage IP Settings window, select **Verilog** for Target language, **Vivado Simulator** for Target simulator, **Mixed** for Simulator language, and a directory to save the customized IP (Figure 1-22). Click **Finish**.

   Note: Make sure the directory name does not include spaces.

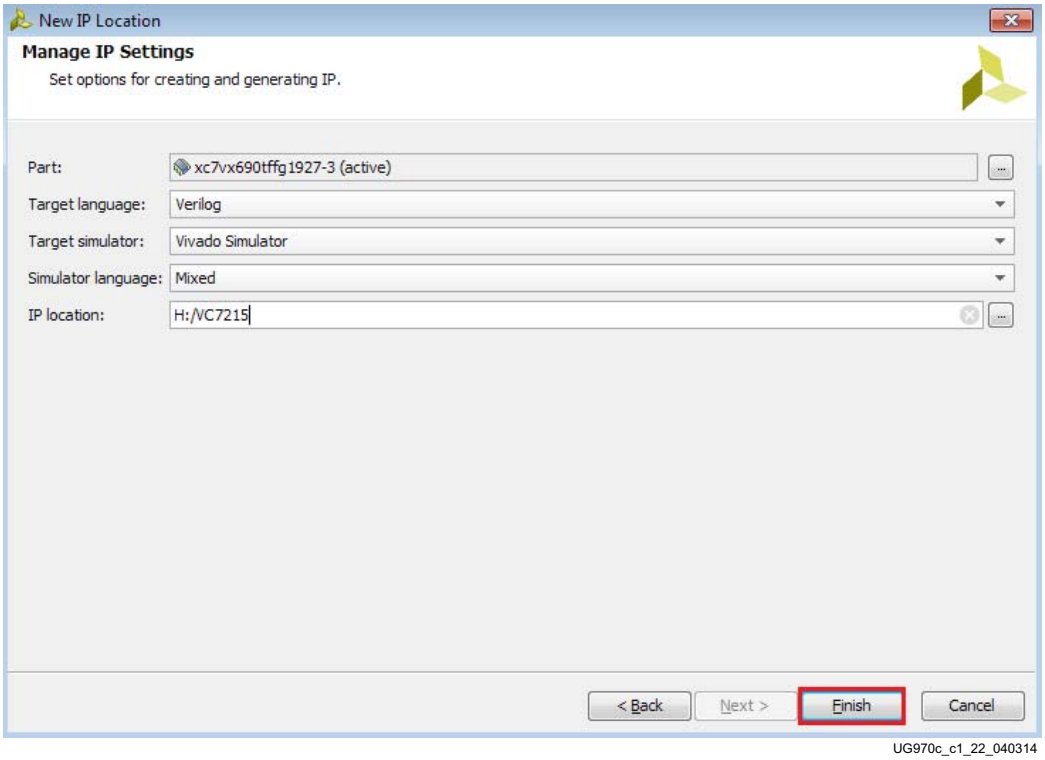


Figure 1-22: **Manage IP Settings**

6. Next, in the IP Catalog window, open the **Debug & Verification** folder, then open the **Debug** folder, and double-click **IBERT 7 Series GTH** (Figure 1-23).

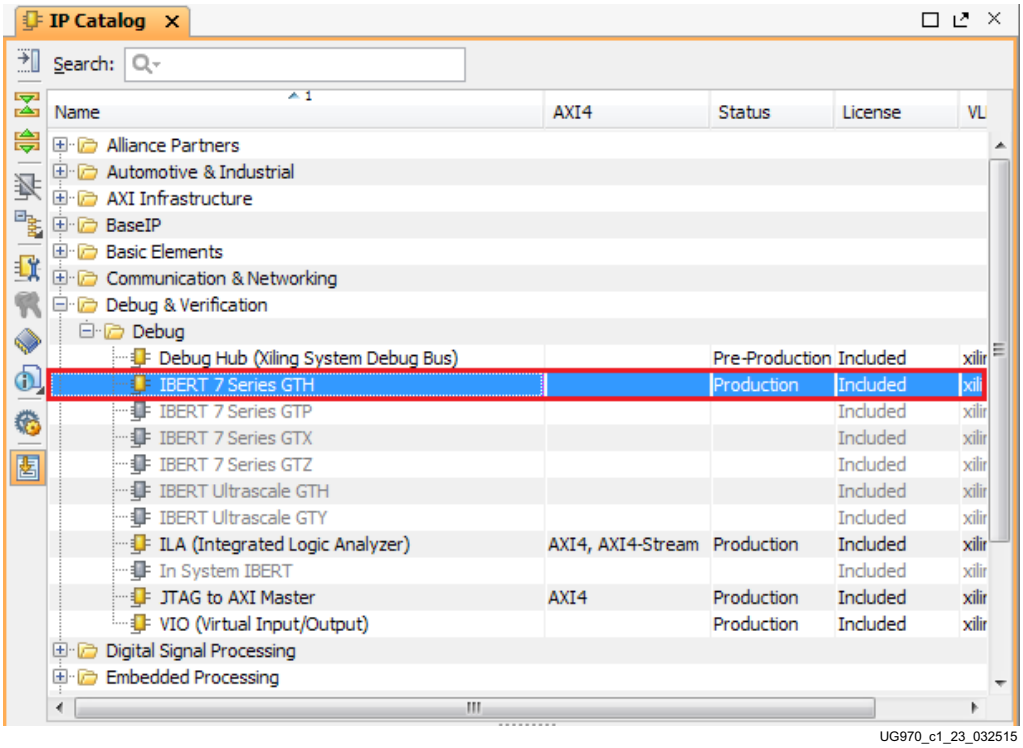


Figure 1-23: **IP Catalog**

7. A Customize IP window opens. In the Protocol Definition tab, change **LineRate (Gbps)** to **13.0**. Then use the drop-down menu to change the **Refclk (MHz)** to **325.00**. Keep the defaults for other fields (Figure 1-24).

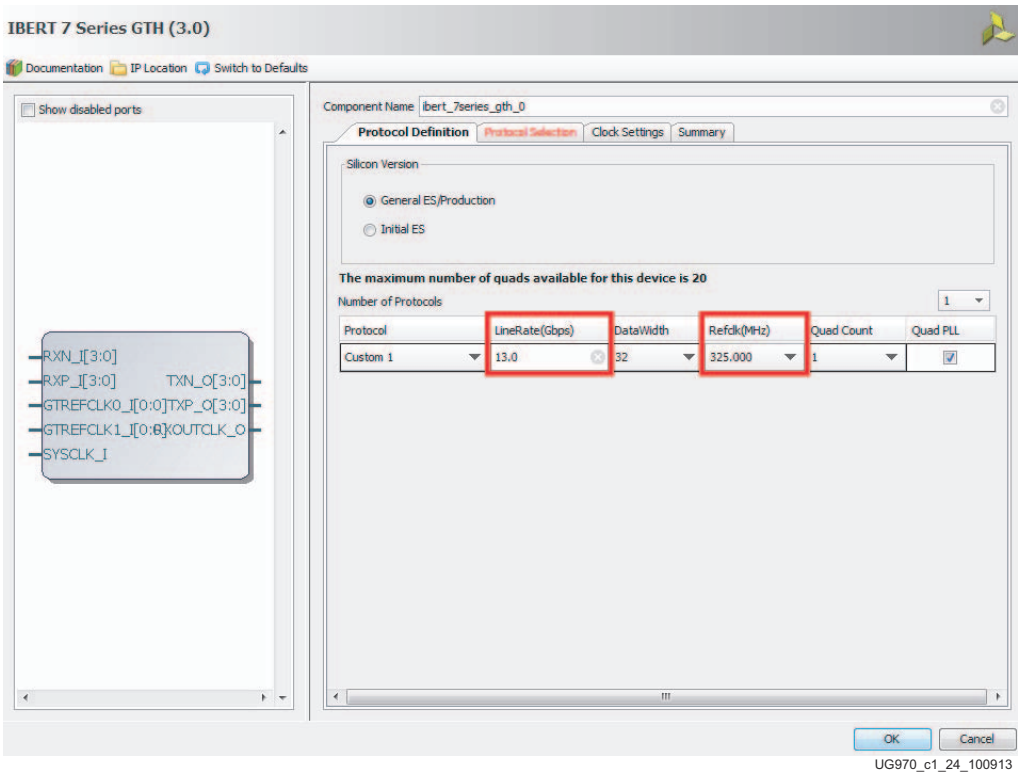


Figure 1-24: **Customize IP - Protocol Definition**

8. In the Protocol Selection tab, use the **Protocol Selected** drop-down menu next to **QUAD_115** to select **Custom 1 / 13.0 Gbps** (Figure 1-25).

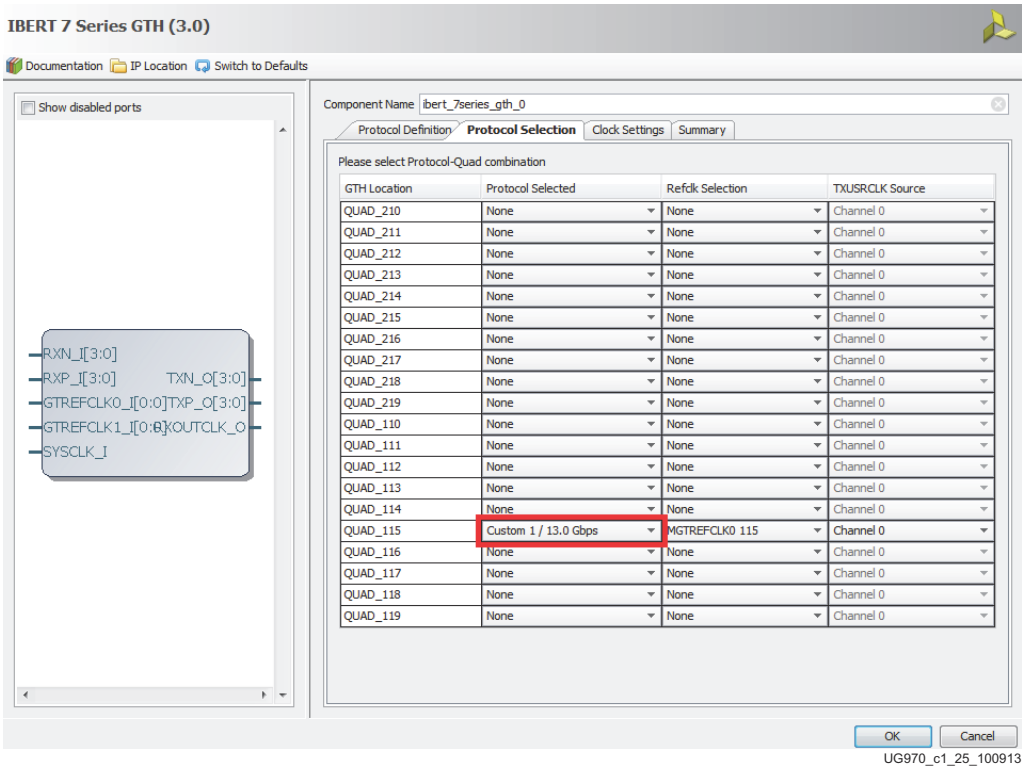


Figure 1-25: **Customize IP - Protocol Selection**

9. In the Clock Settings tab, select **DIFF SSTL15** for the I/O Standard, enter **J25** for P Package Pin and **J26** for N Package Pin (the FPGA pins that the system clock connects to), and ensure the **Frequency** is set to **200.00** (Figure 1-26). Press **OK**.

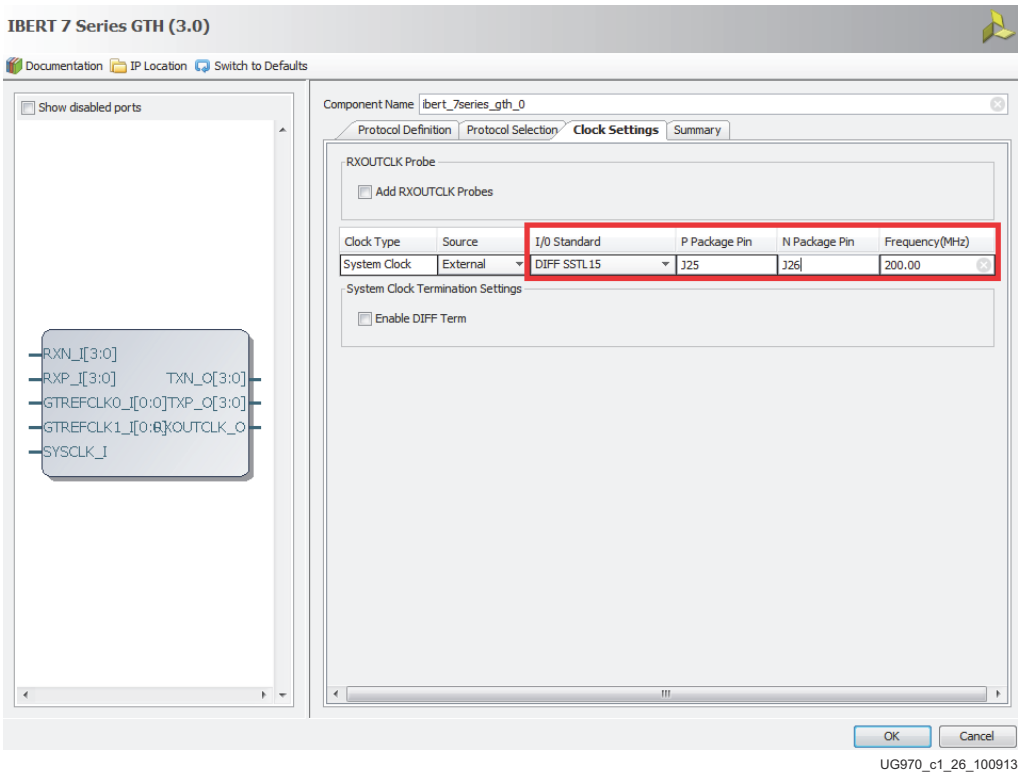


Figure 1-26: **Customize IP - Clock Settings**

10. Back in the Manage IP window (Figure 1-22), in the Sources window, right-click the **IBERT IP** and select **Open IP Example Design** (Figure 1-27). Specify a location to save the design and press **OK**, A Generate Output Products window opens. Leave the defaults unchanged, and press **Generate**. The design opens in a new Vivado window.

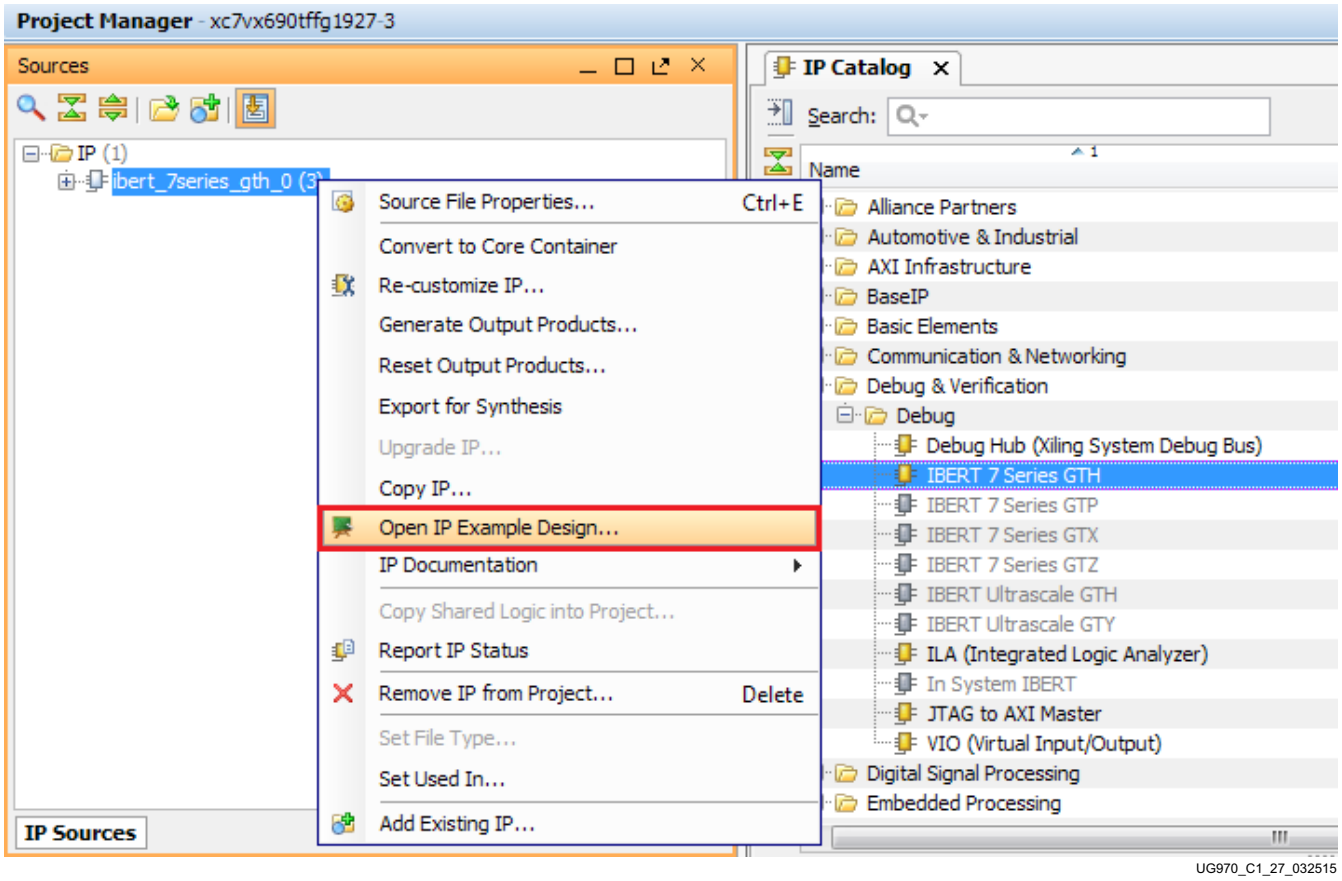


Figure 1-27: **Open IP Example Design**

11. In the new window, select **Tools > Run Tcl Script**. In the **Run Script** window, navigate to **add_scm2.tcl** in the extracted files and press **OK**. The SuperClock-2 Module Design Sources and Constraints are automatically added to the example design (Figure 1-28).

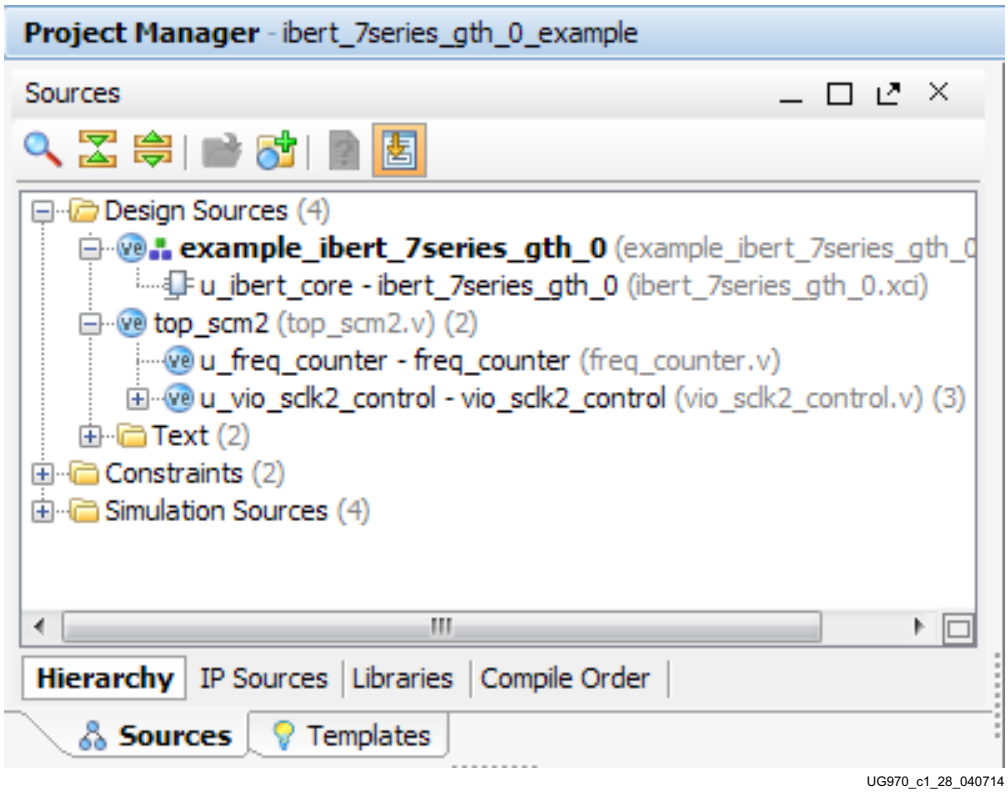


Figure 1-28: **Sources after Running add_scm2.tcl**

12. The SuperClock-2 source code now needs to be added to the example ibert wrapper. In the Sources window, double-click **example_ibert_7series_gth_0** in the Design Sources folder to open the Verilog code. Add the top level ports from `top_scm2.v` to the module declaration, and instantiate the **top_scm2** module in the example ibert wrapper (Figure 1-29). Click **File > Save File**.

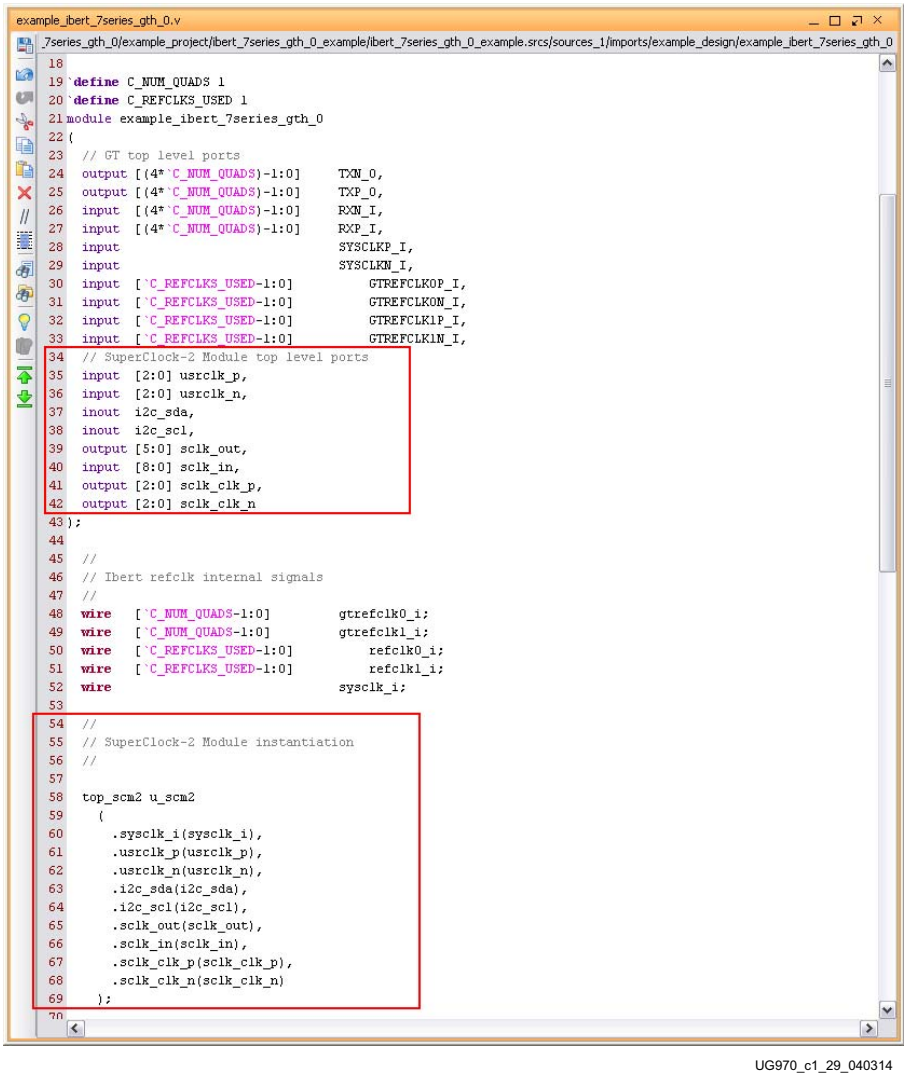


Figure 1-29: **SuperClock-2 in the Example IBERT Wrapper**

13. In the Sources window, Design Sources should now reflect that the SuperClock-2 module is part of the example IBERT design (Figure 1-30).

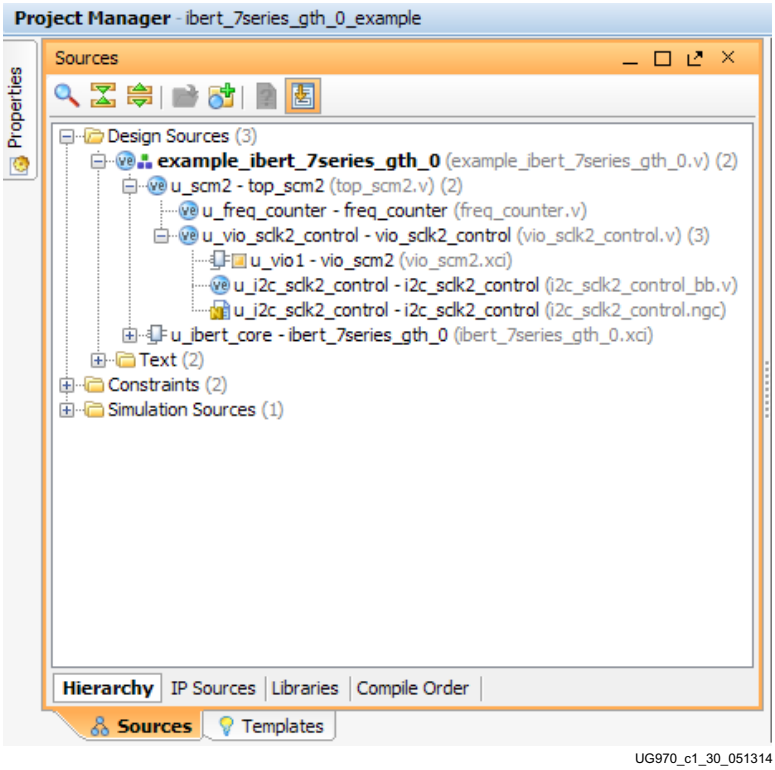


Figure 1-30: **Design Sources File Hierarchy**

14. Click **Run Synthesis in the Flow Navigator** to synthesize the design (Figure 1-31).

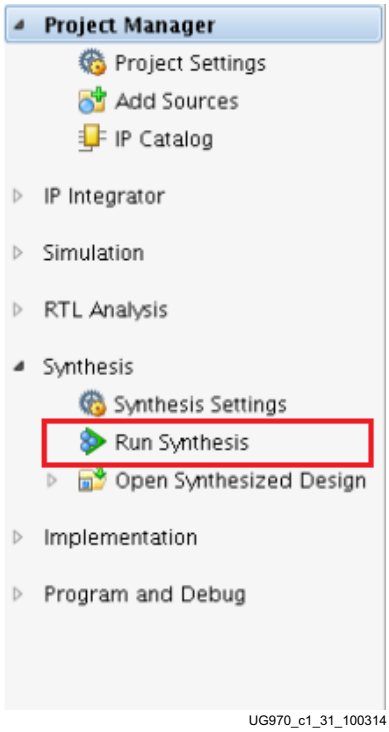


Figure 1-31: **Run Synthesis**

15. When synthesis is done, a Synthesis Complete window pops up. Select **Open Synthesized Design** and click **OK** (Figure 1-32).

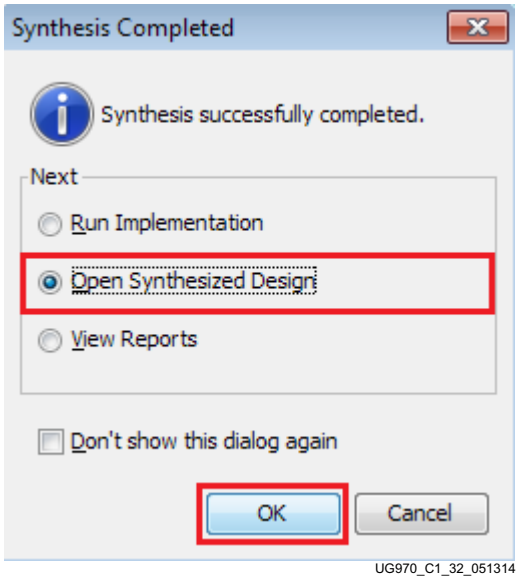


Figure 1-32: **Synthesis Completed**

16. When the Synthesized Design opens, select **dbg_hub** in the Netlist window, then select the **Debug Core Options** tab in the Cell Properties window. Change C_USER_SCAN_CHAIN* to **3** (Figure 1-33). Click **File > Save Constraints**.

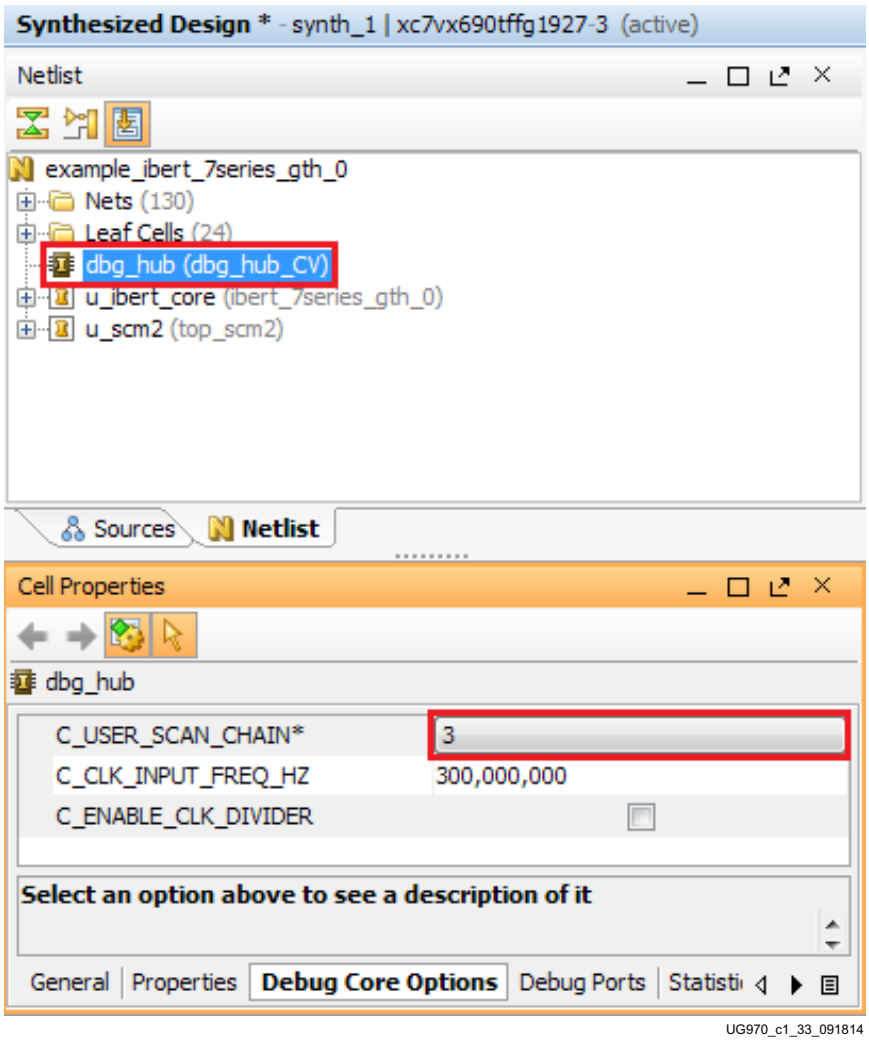


Figure 1-33: **Debug Core Options for dbg_hub**

17. In the Project Manager, under Program and Debug, click **Generate Bitstream** (Figure 1-34). A window pops up asking if it is ok to launch implementation. Click **Yes**.

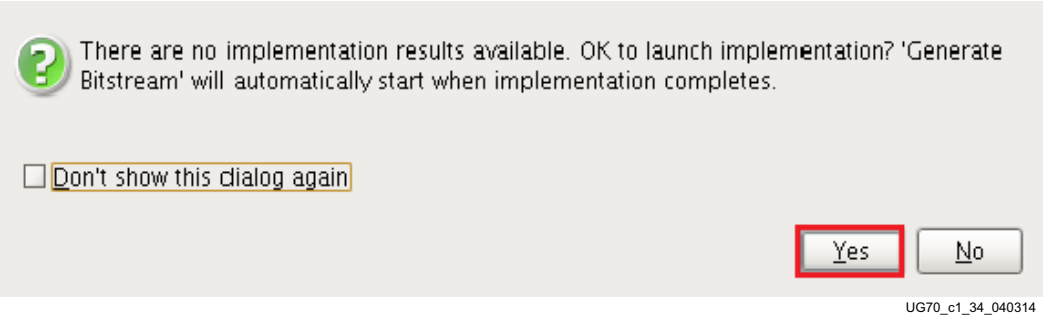


Figure 1-34: **Generate Bitstream**

18. When the Bitstream Generation Completed dialog window appears, click **Cancel** (Figure 1-35).

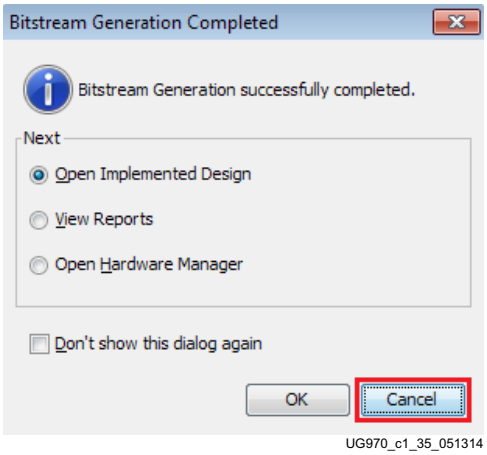


Figure 1-35: **Bitstream Generation Completed**

19. The generated bitstream can be found in the following directory:

```
..\ibert_7series_gth_0\ibert_7series_gth_0_example\ibert_7series
_gth_0_example.runs\impl_1
```

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VC7215 board and its documentation is available on these websites:

Virtex-7 FPGA VC7215 Characterization Kit

Virtex-7 FPGA VC7215 Characterization Kit documentation

Virtex-7 FPGA VC7215 Characterization Kit Master Answer Record (AR 55180)

These Xilinx documents provide supplemental material useful with this guide:

1. *VC7215 Virtex-7 FPGA GTH Transceiver Characterization Board User Guide* (UG972)
2. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770)
3. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
4. *LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTH Transceivers Product Guide for Vivado Design Suite* (PG152)

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