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Hot Swapping with FPGAs

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Summary

Inserting electronics into a live system can be a necessary requirement for an end application. Typically this is called "hot swapping" or "hot plugging", but can also be referred to as "live insertion." A basic understanding of hot swapping is required before inserting an electronic device into a live system fully powered and running without interruption. Depending on the application, these requirements can be more challenging. As an example, the state of the I/O might be required to be maintained during the hot swapping process. With high-performance, high-reliability, and high-speed systems, it can be essential to keep a system live at all times. One such application is a redundant array of independent disks (RAID) storage system that provides high performance for data reliability and is essential to be kept powered and live at all times. Another common example is USB, where you can plug and unplug into a live powered system.

Introduction

Spartan®-7 and newer Xilinx FPGAs have a key balance between performance and functionality. Native hot swap capability is not a feature because this can impact performance, which means that you must take special care when designing for live systems. A live system in this context describes a system that is powered on. As an example with Xilinx FPGAs, there are power sequencing recommendations unique to each FPGA family that still must be followed during a hot swap sequence. In addition to power sequence recommendations, the application might require valid signal integrity levels during a hot swap event. External circuitry might be required to meet I/O requirements for valid signal integrity; so it is important that you understand what rules and restrictions limit the hot swap capabilities of a Xilinx FPGA. If hot swapping is a requirement, the challenge will be greater to design a stable and reliable system. This application note is best used as a checklist for what you need to account for when using a Xilinx FPGA in a hot swap type of application.

Common Guidelines for Hot Swapping Xilinx FPGAs

The hot swap checklist is used as a general rule of thumb for hot swapping Xilinx FPGAs. Note that specific Xilinx FPGA families will have slightly different requirements. Those device-specific requirements are listed in Device-Specific Hot Swap Information. Xilinx FPGAs share the same CMOS I/O structure, but there are some unique older devices that are different. Xilinx high-speed serial transceivers have a different I/O structure than GPIO, but general guidelines still apply for hot swapping. Check the device data sheet for more specific detailed requirements if they exist.

A CMOS I/O structure (symmetrical/complementary type of I/O architecture) in Figure 1 shows the Xilinx FPGA basic I/O structure, which includes clamp diodes seen on most Xilinx FPGAs. A separate diode to V_{CC} and ground are on all SelectIO™ I/O pins for Xilinx FPGA devices.

An easy check for clamp diodes is to look at the absolute maximum V_{IN} specification ratings in the device specific data sheet. If the maximum specification is dependent on V_{CCO} then the device has clamp diodes.

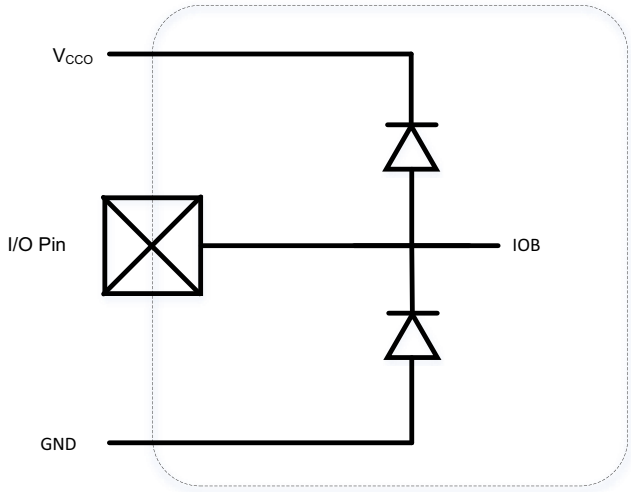

Figure 1: **Xilinx FPGA I/O with Clamp Diodes**

Provided are guidelines to check when using a Xilinx FPGA in a hot swap compliant system.

Hot Swap Checklist

- Follow power sequence recommendations
- Check the I/O state during power sequence and during configuration
- Physically stagger power/ground pin connections.
- External circuitry might be required
- Protect against ESD
- Simulate with IBIS/SPICE

Table 1: **General Xilinx FPGA Hot Swapping Guidelines**

Hot Swap Guidelines	Notes	Additional Info
Follow power sequence recommendations	Certain voltage rails are more critical than others; special care must be taken for power sequencing.	Requirements listed in device-specific data sheets.
Check the I/O state during power sequence and during configuration	Multi-function pins and SSI device specific pins have restrictions during configuration.	I/O status listed in user guides (SelectIO, Configuration). The PUDC_B pin enables pull-up resistors during configuration.
Physically stagger power/ground pin connections	Ground pins are generally physically longer and are connected first, followed by data pin, and then by power pins.	No Xilinx specific guidelines; it depends on the application.
External circuitry might be required	Applications sensitive to the state of the I/O during hot swap might require external circuitry. Pre-charge pins can help protect inrush current. Absolute maximums in data sheets must not be exceeded. Soft-start circuit can manage power supply ramp up. Hot Swap Power Manager ASICs (HSPM) can provide simplified hot swap solutions.	V_{IN} should not exceed the maximum value from the data sheet. I_{IN} (I/O current) also needs monitoring on an individual and bank level. See the device-specific data sheet for more information.
Protect against ESD	Physical PCB design and additional ESD protection circuitry might be needed.	Thin film coating using conducting material can help mitigate ESD effects during hot swapping.
Simulate with IBIS/SPICE	I/O capacitance should be taken into account. Simulation can uncover unwanted I/O effects during hot swap.	Xilinx provides IBIS and SPICE models on Xilinx.com for I/O modeling and simulation.

Device-Specific Hot Swap Information

7 Series (Spartan-7, Artix-7, Virtex-7, Kintex-7 FPGAs) and Zynq®-7000 AP SoC

With Xilinx 28 nm technology, High Range (HR) Select I/O banks have a V_{CCO} power sequencing requirement. This must be taken into account for making the device hot-swap compliant. Note that Spartan-7 and Artix®-7 only have HR banks.

IMPORTANT: *For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0, the voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.*

The voltage levels on the I/O should not exceed the V_{IN} specification found in the specific device data sheets. For example, the Kintex®-7 device has a maximum V_{IN} value of "V_{CCO} + 0.550". If your V_{CCO} is 1.8V, the maximum V_{IN} value your I/O can handle is 1.8V + 0.550 = 2.35V.

For maximum overshoot specifications, look at the "V_{IN} maximum Allowed AC Voltage Overshoot and Undershoot" tables found near the top of the data sheets. The device can handle some overshoot and undershoot above the maximum specifications for a short period of time without any damage occurring. However, Xilinx does not recommend designing to the maximum of the AC overshoot/undershoot if the voltages will be at those extreme levels for extended periods of time.

IMPORTANT: *Clamp diodes are always present on the I/O with the structure from Figure 1. When driving a potentially unpowered bank, the clamp diodes will be forward biased, sinking current into the device. Note that the I_{IN} specification in the data sheet to ensure current on both an I/O and Bank basis are within specification.*

The behavior of the I/O is not guaranteed until the device is powered up.

Example power sequence for a Kintex-7 FPGA:

Power sequence from *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS182) [Ref 3]:

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels, both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ or $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT}$ - $V_{MGTAVCC}$ > 150 mV and $V_{MGTAVCC}$ < 0.7V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT}$ - V_{CCINT} > 150 mV and V_{CCINT} < 0.7V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Virtex-6 FPGAs

Similar to the previously mentioned FPGAs, these Virtex-6 devices can be hot-swap compliant if the power-sequencing requirements are met and current is limited through the I/O.

Virtex-6 FPGAs have clamp diodes to V_{CCO}, similar to Virtex-II Pro, Virtex-4, and Virtex-5 FPGAs, which means that the current through them should be limited in case V_{IN} is applied before V_{CCO}. The maximum current through an I/O is 10 mA, as specified in the data sheet.

The *Hot-Swapping Virtex-II, Virtex-II Pro, Virtex-4, and Virtex-5 Devices Application Note* (XAPP251) [Ref 7] covers hot swapping with older FPGA families, which also applies to Virtex-6 devices. This application note applies to all devices with a clamp diode to V_{CCO}/GND, including Virtex-6 FPGA.

Spartan-6 FPGA

The Spartan-6 can be hot-swap compliant as stated in the *Spartan-6 Family Overview* (DS160) [Ref 2]. These devices do not have clamp diodes to V_{CCO}, one of the only unique devices that does. The Spartan-6 FPGA input voltage is independent of V_{CCO}. See the "Absolute Maximum Ratings" table in *Spartan-6 FPGAs Data Sheet: DC and Switching Characteristics* (DS162) [Ref 1] for details.

In the "Recommended Operating Conditions" table in of *Spartan-6 FPGAs Data Sheet: DC and Switching Characteristics* (DS162) [Ref 1], you can see that you can safely apply a voltage up to 3.95V maximum to the I/O without damage.

Diodes are only available for PCI standards. If using a PCI standard, the diodes are enabled. The hot-swap/hot-plug compatibility then follows the usual rules; the current through the I/Os should be limited and V_{IN} should follow the absolute maximum specifications.

References

1. *Spartan-6 FPGAs Data Sheet: DC and Switching Characteristics* (DS162)
2. *Spartan-6 Family Overview* (DS160)
3. *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS182)
4. *Spartan-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS189)
5. *Virtex-7 T and XT FPGAs Data Sheet: DC and Switching Characteristics* (DS183)
6. *Artix-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS181)
7. *Hot-Swapping Virtex-II, Virtex-II Pro, Virtex-4, and Virtex-5 Devices* (XAPP251)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2018	1.1	Added two sentences about Xilinx high speed serial transceivers to the end of the first paragraph in the Common Guidelines for Hot Swapping Xilinx FPGAs section.
03/31/2017	1.0	Initial Xilinx release.

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