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All Digital VCXO Replacement Using a Gigabit Transceiver Fractional PLL

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Summary

This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within the gigabit transceiver and associated PLLs.

Note: In this application note, *transceiver* refers to these types of transceivers:

Device Family	Transceiver Type
Virtex® UltraScale™ FPGAs	GTY transceiver
Kintex UltraScale+™ and Virtex UltraScale+ FPGAs, and Zynq® UltraScale+ devices	GTH, GTM, and GTY transceivers

A common design requirement is to frequency or phase lock a transceiver output to an input source (known as loop, recovered, or slave timing). Traditionally, an external clock cleaning device or VCXO and PLL components are used to provide a high-quality clock reference for the transceiver, since FPGA logic-based clocks are generally too noisy. While effective, external clock components carry a power and cost penalty that is additive as each individual clock channel is generated. When using many channels or in low-cost systems, the cost can be significant. Additionally, adding many external clock sources provides more opportunity for crosstalk and interference at the board level.

The system described in this application note provides a method to effectively replace these external clock components with the Xilinx transceiver fractional PLL (fPLL) when used in conjunction with a high-performance FPGA based digital PLL (DPLL). Each Quad PLL (QPLL) has the capability to be fractionally frequency controlled using a dedicated interface. The QPLL has an interface that controls a sigma delta modulator (SDM) to enable the fractional feedback capability in the QPLL. The main QPLL feedback is controlled fractionally based on the SDM control word allowing fine frequency control by modulating the ratio of the feedback between N and N+1. The control input can be set statically or controlled dynamically from an FPGA logic-based DPLL system.

The reference design circuit provides a fully integrated DPLL and transceiver fPLL system which can be instantiated for each QPLL used. The QPLL nominal operating rate is set using an external crystal oscillator (XO), and using the fPLL feature the output can be phase- or frequency-locked to an input reference signal. The DPLL enables generation of a synchronous QPLL output with run-time configurable parameters (e.g., gain, cutoff frequency, and clock divider values) to enable you to set up the operation specifically for the end application. This allows the flexibility of the reference input signal and DPLL cleaning bandwidth.

The reference design circuit can lock the QPLL over the full fractional range from N to N+1 of the main fPLL divider setting and programmatically provide jitter cleaning bandwidths in the range from 0.1 Hz to 1 kHz. In the UltraScale FPGAs, the transceiver is capable of operating to over 30 Gb/s[1]. Typical applications for this circuit include video SD/HD, Sync E, IEEE1588, SDH, SONET, and OTN.

This system offers a complimentary feature to the proven phase interpolator controlled crystal oscillator (PICXO) feature available in 7 series and UltraScale devices (refer to *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)* (XAPP589) [Ref 1] and *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs)* (XAPP1241) [Ref 2]). The implementation between the fPLL and PICXO, however, is different. The PICXO manipulates the transceiver clock on a per lane basis at the transceiver output directly based on the input QPLL or CPLL bit rate clock, while the fPLL manipulates the QPLL clock output rate directly. There are therefore differences in the use cases for each method. Specifically, the fPLL can provide two fractionally capable clock outputs from QPLLs 0 and 1 that can be shared among the four transceivers in the Quad group.

The fPLL also offers a lower jitter alternative to the phase interpolation based PICXO techniques. It is better suited to applications in which lowest jitter is critical (e.g., synchronous digital hierarchy (SDH)/Sonet or optical transport network (OTN) systems) as well as applications that require controlled TX latency such as common packet radio interface (CPRI) or IEEE1588. These can be supported with the fractional controlled crystal oscillator (FRACXO).

You can download the reference design files for this application note from the Xilinx® website. For detailed information about the design files, see Reference Design, page 23.

For full details on the fPLL operation of transceivers in Virtex UltraScale FPGAs, refer to the *UltraScale Architecture GTY Transceivers User Guide* (UG578) [Ref 3]. Refer to *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893) [Ref 4] for switching characteristics.

Fractional N PLL theory is not covered in this application note. However, there are many references available on the subject. This application note does provide a ready solution to the Dynamic Frac-N example recommended in *UltraScale Architecture GTY Transceivers User Guide* (UG578). An extract is shown in Figure 1, where a fabric-based PLL provides the control around the GTY Frac-N PLL to provide locking to an external source.

[1] The maximum supported line rate for the transceiver and fPLL varies with device and family. The latest specifications are contained in the user guides and data sheets for the relevant transceivers.

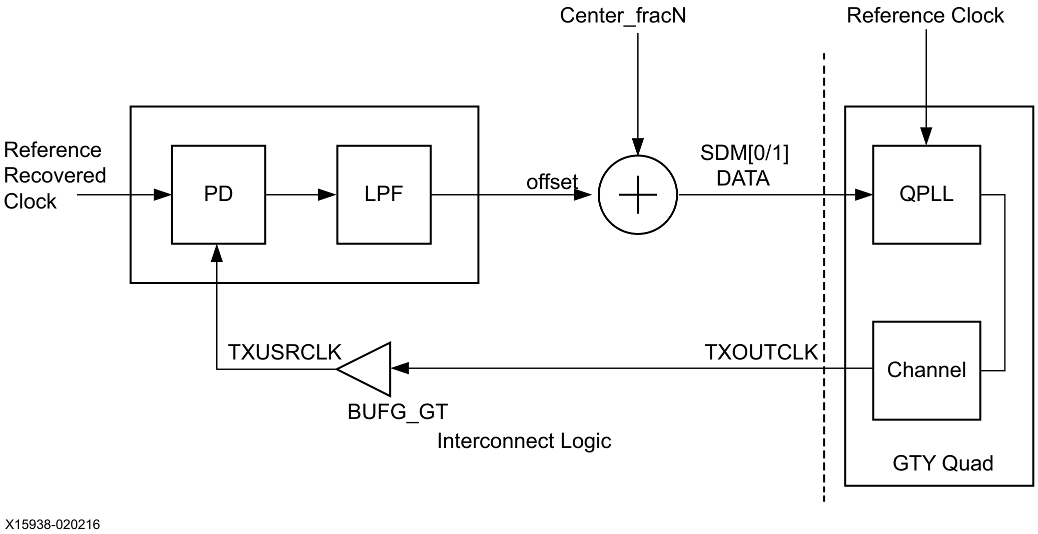


Figure 1: **SDM Application Example**

The fPLL exists in the GTY QPLL in Virtex UltraScale FPGAs and also in all UltraScale+ device QPLLs. The QPLL is self-contained and multiplies the external ref clk in (XO) to the required bit rate using the attributes M and N that can be set by the user. This generates the base bit rate clock for the transceiver.

When the SDM functionality is enabled, the SDM data port and the fractional capability functions are active. The SDM data settings modulate the fractional divider between its base setting N and N+1, allowing with high precision (here 2^{24} bits) a non-integer bit rate to be output from the QPLL.

When the SDM data port is driven from a separate DPLL (here known as the FRACXO DPLL), the main PLL clock can be locked to a separate synchronization reference. This configuration is shown in Figure 2. This DPLL also provides the ability to jitter clean the synchronization reference, and the FRACXO DPLL is intended to be operated with transfer bandwidths < 1 kHz, thus enabling an on-chip way to replace an external VCXO or cleaning PLL system.

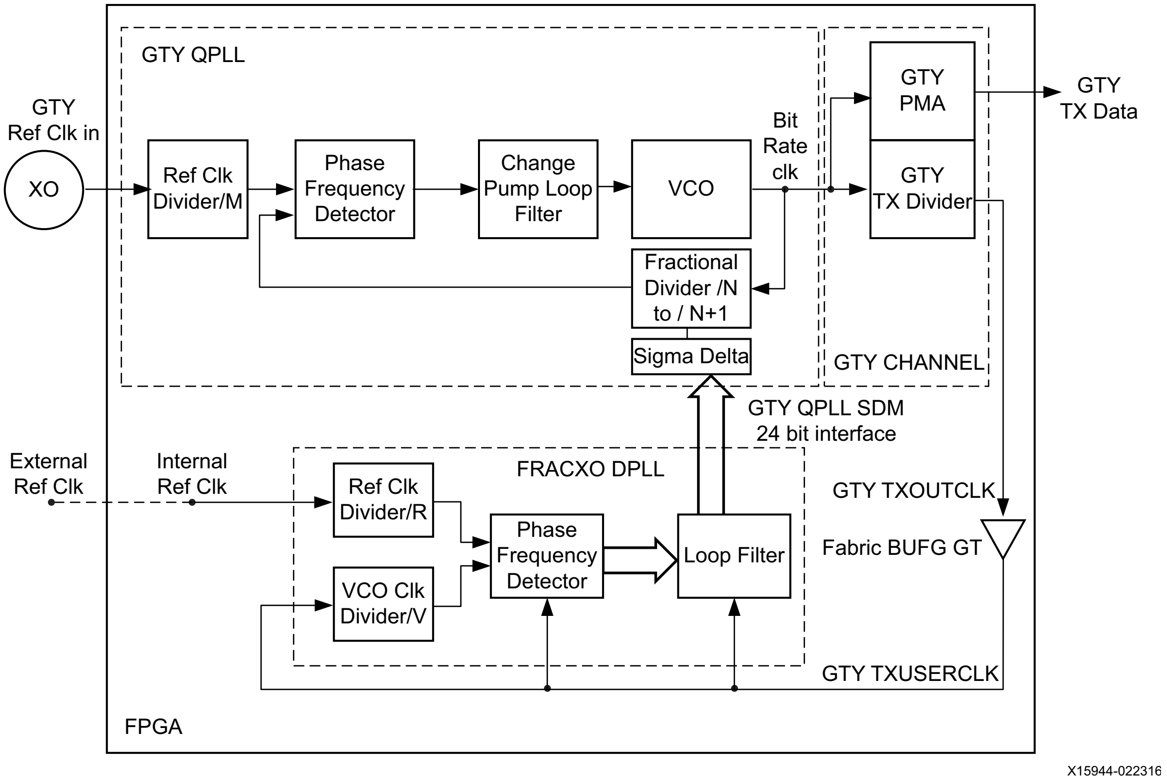


Figure 2: **System Overview**

An example of how the system could be configured in Figure 2 is demonstrated as follows. The GTY TX data output is at a nominal rate of 10.3125 Gb/s and is required to lock to a transceiver recovered clock of 257.8125 MHz using the fPLL.

In the first instance, the external XO needs to be selected based on the output frequency required. Given the fPLL can operate with divide ratios between N and N+1 based on the SDM input word, the nominal rate should not be set to an integer multiple. This can then allow for tune range. Additionally, with GTY transceivers in UltraScale FPGAs, the fPLL allows only 1/64 of its range to be dynamically adjusted, the coarse adjust being a user set fixed value. This results in the boundaries for continuous tuning being N to (N+1) quantized into 64 discrete sub-tuning ranges. The effective tuning range is then (N+m/64) to (N+(m+1)/64) where N is the QPLL divider ratio and m is the user set dynamic tune range from 0 to 63.

Considering the case of GTY transceivers in UltraScale FPGAs where the first tune range is used (m = 0), we can then define the required divider ratio as (N+0.5/64) to generate the nominal center tune frequency. N can be set to any of the legal values. For this example, N can be set to 40.

Solving for the equation 10.3125 GHz = XO Frequency × (N+0.5/64) gives a nominal XO rate of 257.762 MHz. This yields a full tune range of between 257.762 MHz × 40 to 257.762 MHz × 40.015625 MHz. The resultant fPLL continuous tune range for this setting is 10.31048 GHz to 10.31451 GHz, or ±195 ppm from the nominal rate. The user should maintain a maximum dynamic frequency shift of ±200 ppm from nominal after a QPLL reset.

In all FRACXO use cases it is the user's responsibility to ensure the transceiver SDM capability is adhered to. This is detailed in the appropriate device user guides and data sheets. Currently the following restrictions apply:

- For both UltraScale and UltraScale+ devices: The maximum supported dynamic SDM excursion from a QPLL reset event is ±200 ppm.
- For only UltraScale devices: Only the lower 18 bits should be dynamically tuned.

The FRACXO provides a programmable limiter function that can be used to ensure these conditions are met.

The FRACXO DPLL directly controls the SDM input to lock the TXUSERCLK to the input reference clock. Because the TXUSERCLK is derived directly from the QPLL, this allows locking of the system to the desired reference signal. Because the FRACXO DPLL has integer dividers, R and V, these need to be set according to the input frequencies TXUSERCLK and the input reference clock with the requirement that the compare frequencies at the FRACXO phase frequency detector are equal to lock the system. In the example design, both the recovered clock rate and the TXUSERCLK rate are equal, making R and V the same value. Normally, the FRACXO DPLL would be operated with relatively low compare frequencies (e.g., below 2 MHz) to achieve overall transfer bandwidths less than 1 kHz. The FRACXO design spreadsheet can estimate the overall transfer function between the input reference clock and the output TX data signal based on the control settings. Detailed operation is described in FRACXO DPLL, however the normal use model is for the FRACXO DPLL to enable the output to be locked to a nosier, lower speed input clock, thus replicating a traditional VCXO function.

FRACXO DPLL

The FRACXO parameters must be set appropriately to generate the QPLL locked to a reference signal. The DPLL can be analyzed using standard methods from a derivation of the transfer function outlined in this section.

The FRACXO DPLL circuit, for analysis purposes, is considered to be in three functional blocks:

1. Phase frequency detector (PFD): A high-performance oversampling based circuit designed to give low phase noise, high dynamic range, and a linear response with gain G_{PD}.
2. Loop filter: Gains are defined by the terms G_1 and G_2. The output represents the required tune value for the fPLL SDM in the transceiver. Gain values scale 2^{G1} and 2^{G2}.
3. Numerically controlled oscillator (NCO): The numerically controlled oscillator function is performed by the transceiver and has gain G_{FRAC}.

These blocks are shown in a standard DPLL configuration in Figure 3.

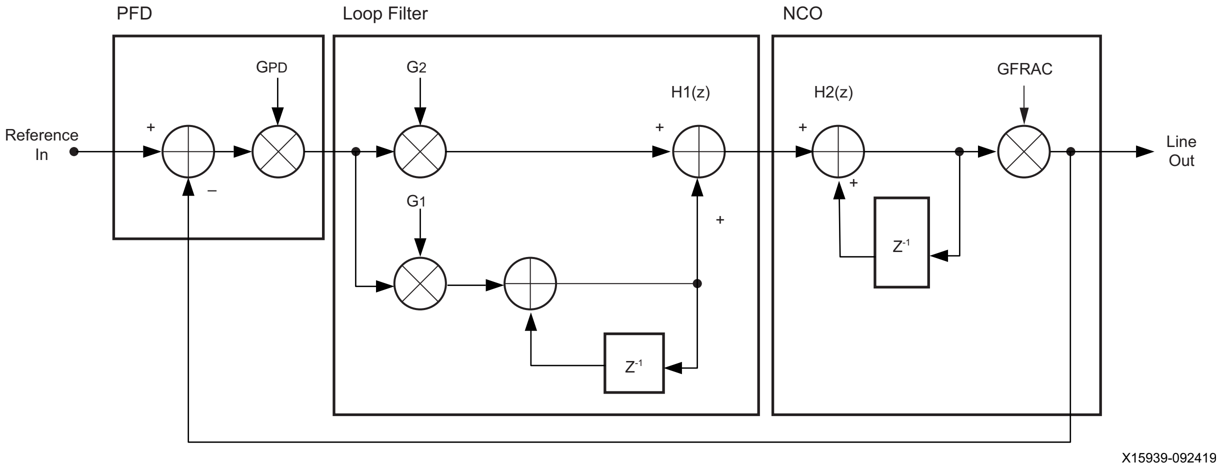


Figure 3: **FRACXO DPLL Digital Equivalent**

The transfer of the reference input clock to the line output data is represented by the function in Equation 1 to Equation 3. This allows the clock cleaning and tracking of the digital VCXO replacement to be exactly controlled by your application.

$$H(z) = \frac{H1(z)H2(z)G_{PD}}{1 + H1(z)H2(z)G_{PD}} \qquad \textit{Equation 1}$$

with:

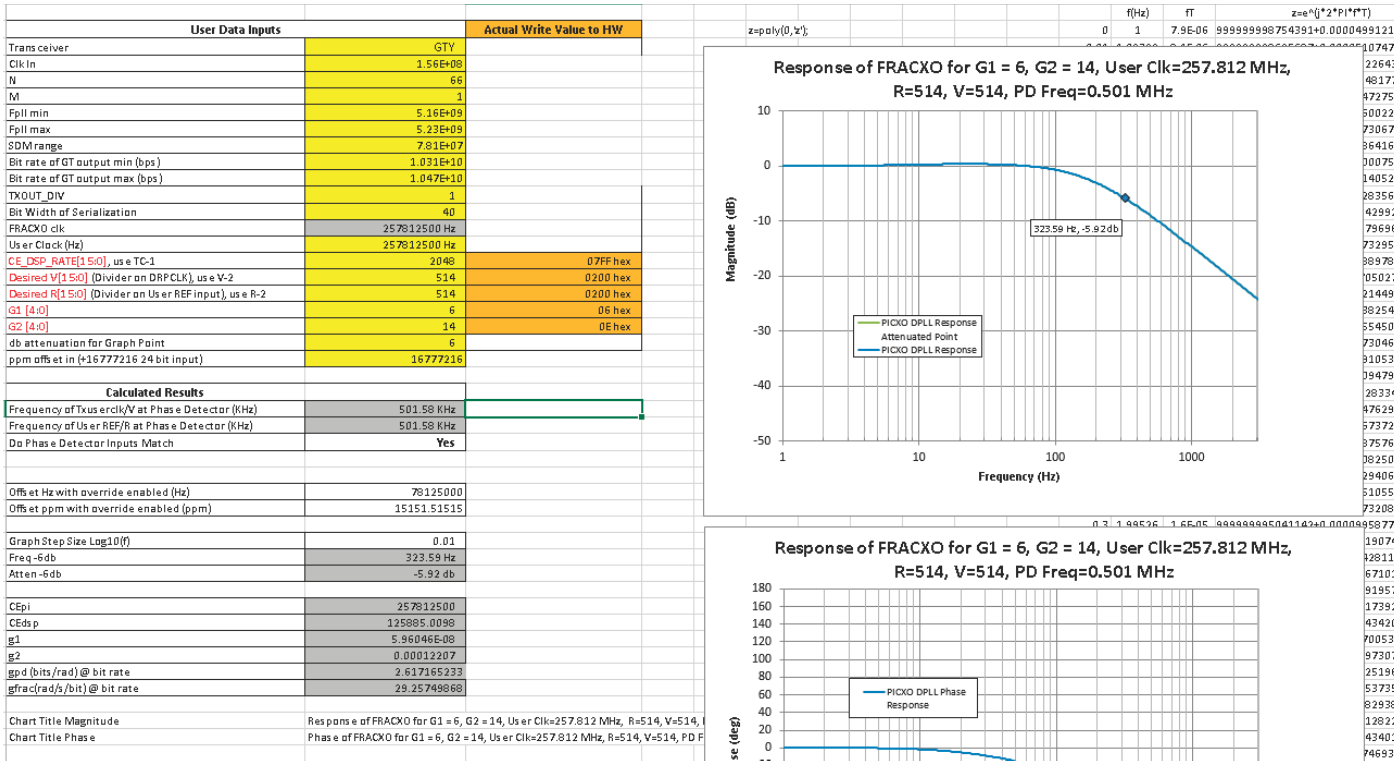
$$H1(z) = \frac{(g1 + g2)z - g2}{(z - 1)} \qquad \textit{Equation 2}$$

and

$$H2(z) = \frac{z(G_{FRACXO})}{(z - 1)} \qquad \textit{Equation 3}$$

The Excel spreadsheet tool included in the FRACXO design file package allows you to estimate the overall FRACXO response when setting the configurable parameters listed above (Figure 4).

The FRACXO DPLL allows complete flexibility with settings, therefore it is advisable to understand the performance trade-offs of the PLL in the end system.



User Data Inputs		Actual Write Value to HW
Transceiver	GTY	
Clk In	1.56E+08	
N	66	
M	1	
Fpll min	5.16E+09	
Fpll max	5.23E+09	
SDM range	7.81E+07	
Bit rate of GT output min (bps)	1.031E+10	
Bit rate of GT output max (bps)	1.047E+10	
TXOUT_DIV	1	
Bit Width of Serialization	40	
FRACXO clk	257812500 Hz	
User Clock (Hz)	257812500 Hz	
CE_DSP_RATE[15:0], use TC-1	2048	07FF hex
Desired V[15:0] (Divider on DRPCLK), use V-2	514	0200 hex
Desired R[15:0] (Divider on User REF input), use R-2	514	0200 hex
G1 [4:0]	6	06 hex
G2 [4:0]	14	0E hex
db attenuation for Graph Point	6	
ppm offset in (+16777216 24 bit input)	16777216	
Calculated Results		
Frequency of Txuserclk/V at Phase Detector (KHz)	501.58 KHz	
Frequency of User REF/R at Phase Detector (KHz)	501.58 KHz	
Do Phase Detector Inputs Match	**Yes**	
Offset Hz with override enabled (Hz)	78125000	
Offset ppm with override enabled (ppm)	15151.51515	
Graph Step Size Log10(f)	0.01	
Freq -6db	323.59 Hz	
Atten -6db	-5.92 db	
CEpi	257812500	
CEdsp	125885.0098	
g1	5.96046E-08	
g2	0.00012207	
gpd (bits/rad) @ bit rate	2.617165233	
gfrac(rad/s/bit) @ bit rate	29.25749868	
Chart Title Magnitude	Response of FRACXO for G1 = 6, G2 = 14, User Clk=257.812 MHz, R=514, V=514, I	
Chart Title Phase	Phase of FRACXO for G1 = 6, G2 = 14, User Clk=257.812 MHz, R=514, V=514, PD F	

z=poly(0,'z');		f(Hz)	fT	z=e^(j*2*PI*f*T)
	0	1	7.9E-06	999999998754391+0.0000499121

Response of FRACXO for G1 = 6, G2 = 14, User Clk=257.812 MHz, R=514, V=514, PD Freq=0.501 MHz
Magnitude (dB)
10
0
-10
-20
-30
-40
-50
1
10
100
1000
Frequency (Hz)
323.59 Hz, -5.92db
PICXO DPLL Response Attenuated Point
PICXO DPLL Response
Response of FRACXO for G1 = 6, G2 = 14, User Clk=257.812 MHz, R=514, V=514, PD Freq=0.501 MHz
180
160
140
120
100
80
60
40
20
0
se (deg)
PICXO DPLL Phase Response

X15945-092419

Figure 4: **FRACXO DPLL Spreadsheet Example Calculation**

For optimum jitter and cleaning performance, it is recommended that the FRACXO DPLL bandwidth be less than 1 kHz. Higher tracking bandwidths can be achieved, however, with some increase in jitter. It might be desirable to have a high bandwidth to acquire lock, then switching subsequently to a lower cleaning bandwidth. This is known as fast acquisition for the DPLL.

The DPLL architecture allows operational changes to the G_1 and G_2 values to support this while not losing phase lock. Changes can be supported in user logic by applying variable G_1 and G_2 values. It can be appropriate to monitor the error output from the DPLL as one method to ascertain a suitable point at which to switch gain values.

fPLL FRACXO Example Design

This section includes sample measurements of the example FRACXO design implemented on the VCU108 board where the system has been configured as a nominal 10.3125 Gb/s loop timed design (Figure 5). That is, the data is received on the GTY transceiver input and re-transmitted with the fPLL generated clock locking to and jitter cleaning the received recovered clock from the line data with the FRACXO DPLL. The system is operated with a reference clock of 257.762 MHz as per the example used in the fPLL operation section.

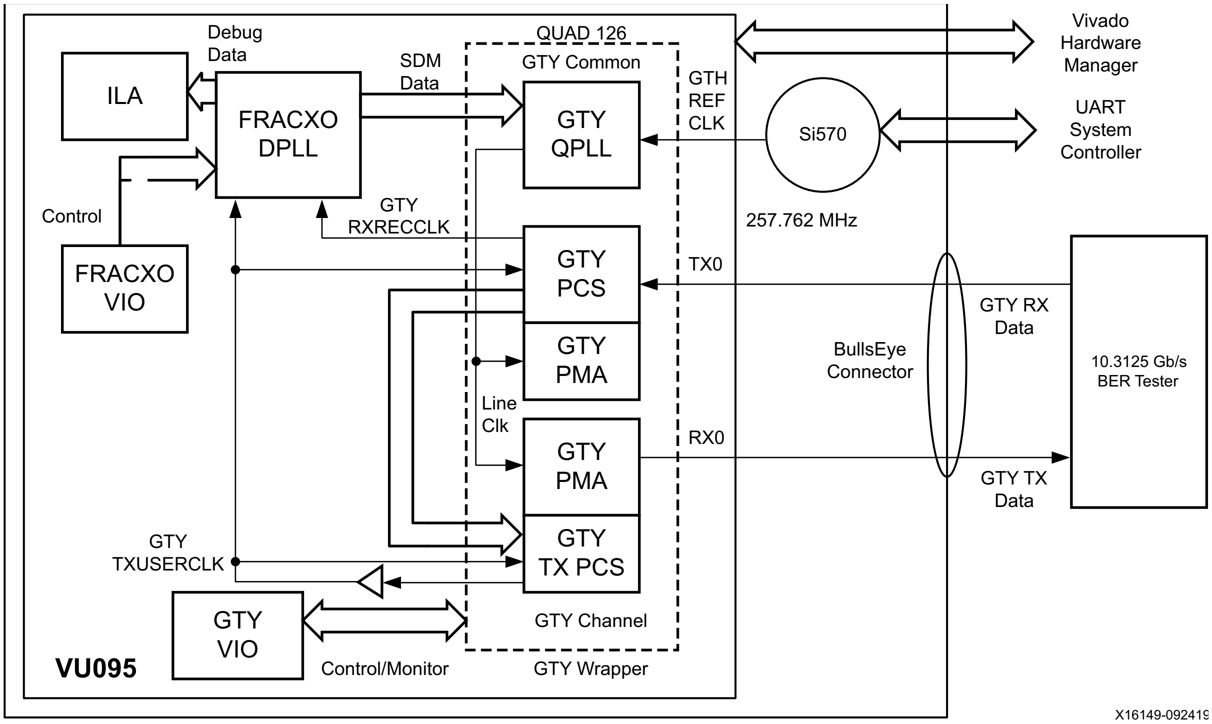


Figure 5: **Example Design Block Diagram**

The connections to GTY Quad 126 are made with a BullsEye cable as shown in Figure 6. The GTY reference clock is sourced on MGTREFCLK1 from the onboard Si570 clock generator. The Si570 can be set to 257.762 MHz using the UART interface and system controller. Information on how to do this and more detail on the VCU108 is given in the *VCU108 Evaluation Board User Guide* (UG1066) [Ref 5].

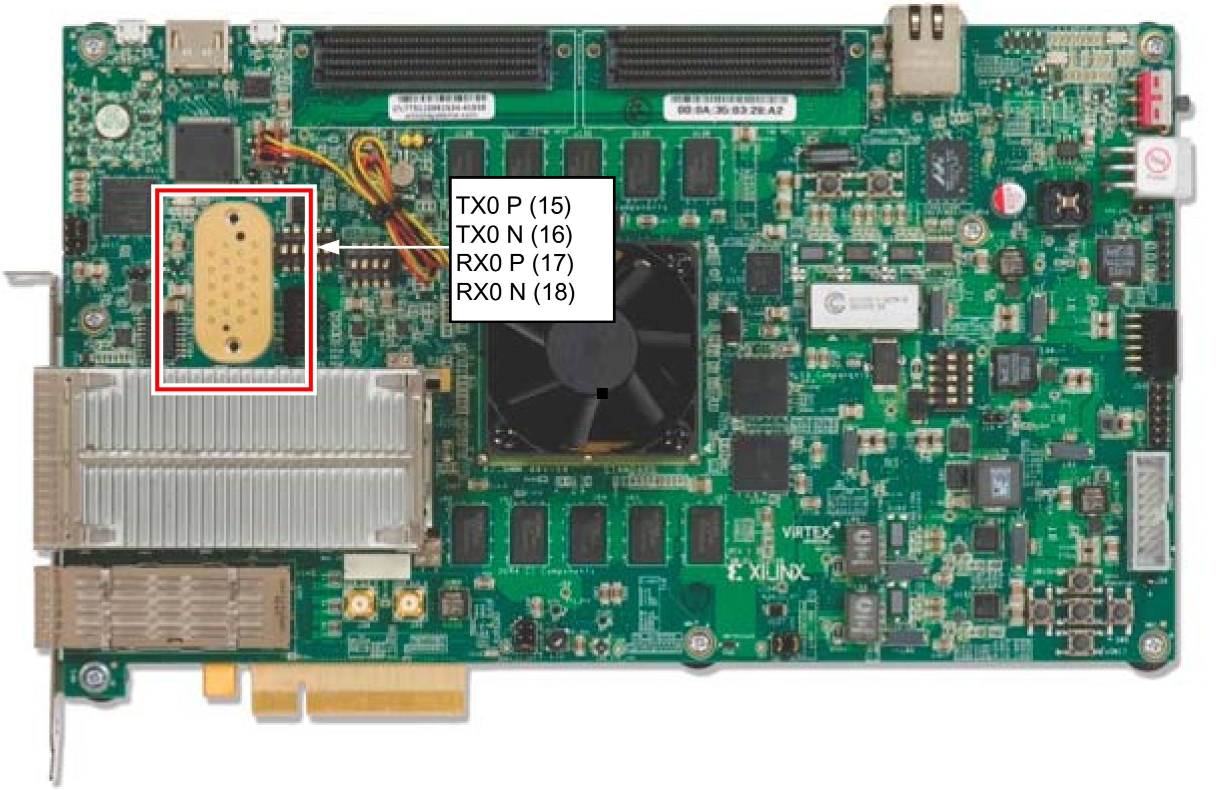
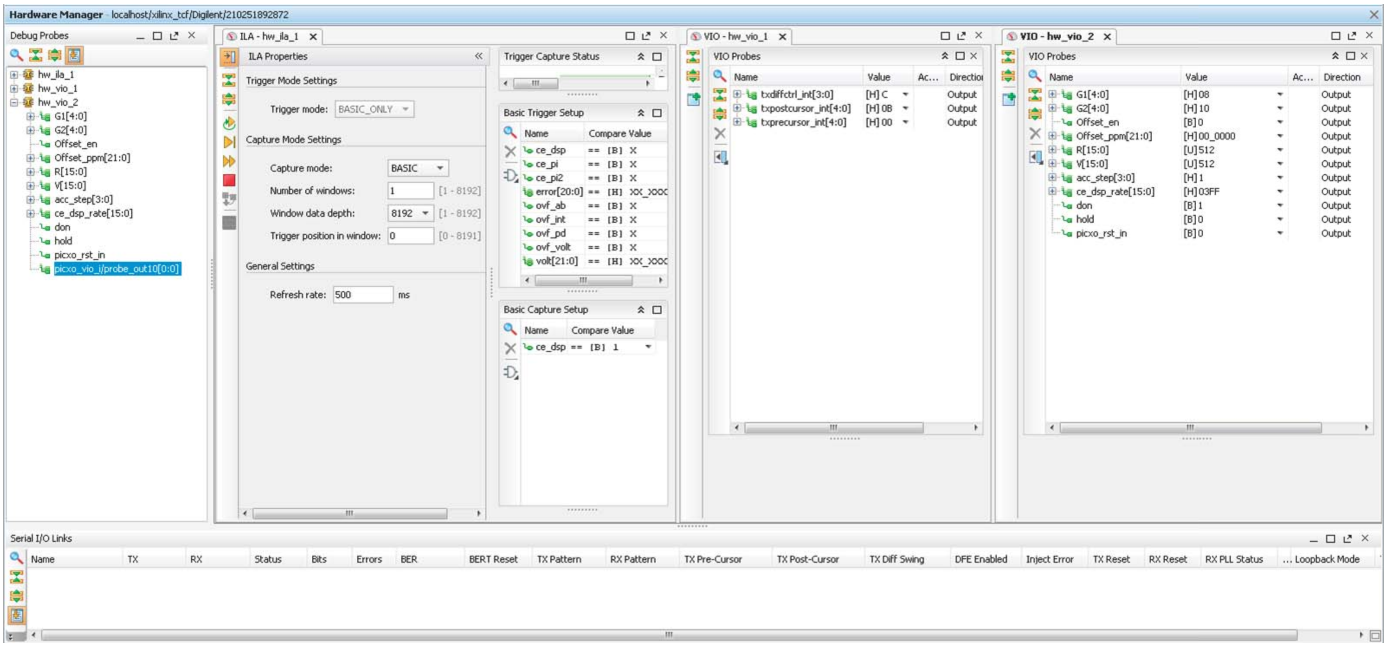


Figure 6: **VCU108 Connections**

After it is loaded from the Vivado® hardware manager, the interface shown in Figure 7 is available with access to the FRACXO configurable parameters and the GTY driver outputs. The default virtual input/output (VIO) configuration should enable the FRACXO to lock and loop the data through the device. For additional debug information, an integrated logic analyzer (ILA) is incorporated where the FRACXO operation can be observed (i.e., error and volt traces).



Hardware Manager - localhost/xilinx_tcf/Digilent/210251892872

Debug Probes

- hw_ila_1
- hw_vio_1
- hw_vio_2
  - G1[4:0]
  - G2[4:0]
  - Offset_en
  - Offset_ppm[21:0]
  - R[15:0]
  - V[15:0]
  - acc_step[3:0]
  - ce_dsp_rate[15:0]
  - don
  - hold
  - picxo_rst_in
  - picxo_vio_i/probe_out10[0:0]

ILA - hw_ila_1

ILA Properties

Trigger Mode Settings

Trigger mode: BASIC_ONLY

Capture Mode Settings

Capture mode: BASIC

Number of windows: 1 [1 - 8192]

Window data depth: 8192 [1 - 8192]

Trigger position in window: 0 [0 - 8191]

General Settings

Refresh rate: 500 ms

Trigger Capture Status

Basic Trigger Setup

Name	Compare Value
ce_dsp	== [B] X
ce_pi	== [B] X
ce_pi2	== [B] X
error[20:0]	== [H] XX_XXX
ovf_ab	== [B] X
ovf_int	== [B] X
ovf_pd	== [B] X
ovf_volt	== [B] X
volt[21:0]	== [H] XX_XXX

Basic Capture Setup

Name	Compare Value
ce_dsp	== [B] 1

VIO - hw_vio_1

VIO Probes

Name	Value	Ac...	Direction
txdiffctrl_int[3:0]	[H] C		Output
txpostcursor_int[4:0]	[H] 0B		Output
txprecursor_int[4:0]	[H] 00		Output

VIO - hw_vio_2

VIO Probes

Name	Value	Ac...	Direction
G1[4:0]	[H] 08		Output
G2[4:0]	[H] 10		Output
Offset_en	[B] 0		Output
Offset_ppm[21:0]	[H] 00_0000		Output
R[15:0]	[U] 512		Output
V[15:0]	[U] 512		Output
acc_step[3:0]	[H] 1		Output
ce_dsp_rate[15:0]	[H] 03FF		Output
don	[B] 1		Output
hold	[B] 0		Output
picxo_rst_in	[B] 0		Output

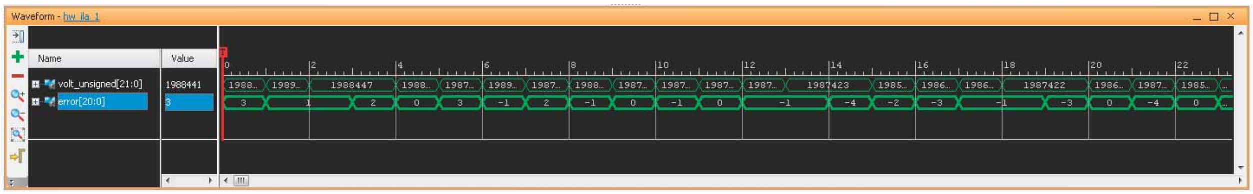
Serial I/O Links

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	... Loopback Mode

X16151-092419

Figure 7: **Vivado Hardware Manager Console**

Figure 8 shows the error and volt ILA captures from a system that is locked.



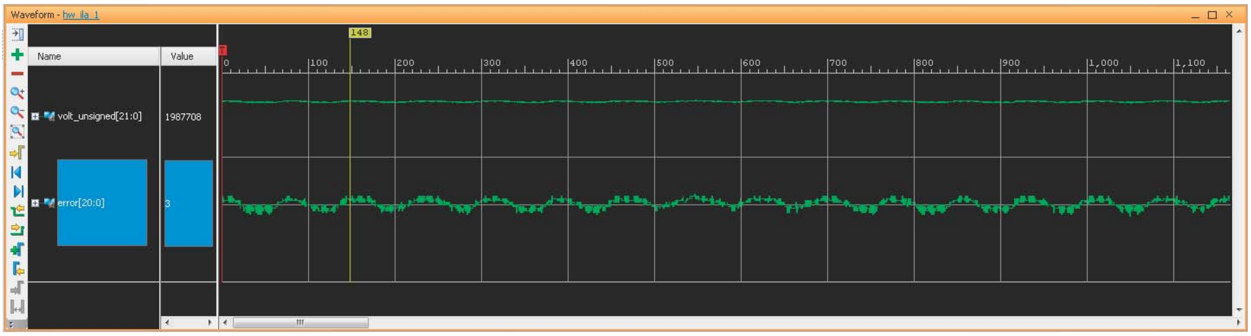
Waveform - hw_ila_1

Name	Value
volt_unsigned[21:0]	1988441
error[20:0]	3

X16152-022216

Figure 8: **Error and Volt in a Locked System**

It can be useful to examine the error and volt traces using the analog view. Using a capture qualified with CE_{DSP} active, you can see the DPLL time domain performance (Figure 9).



Waveform - hw_ila_1

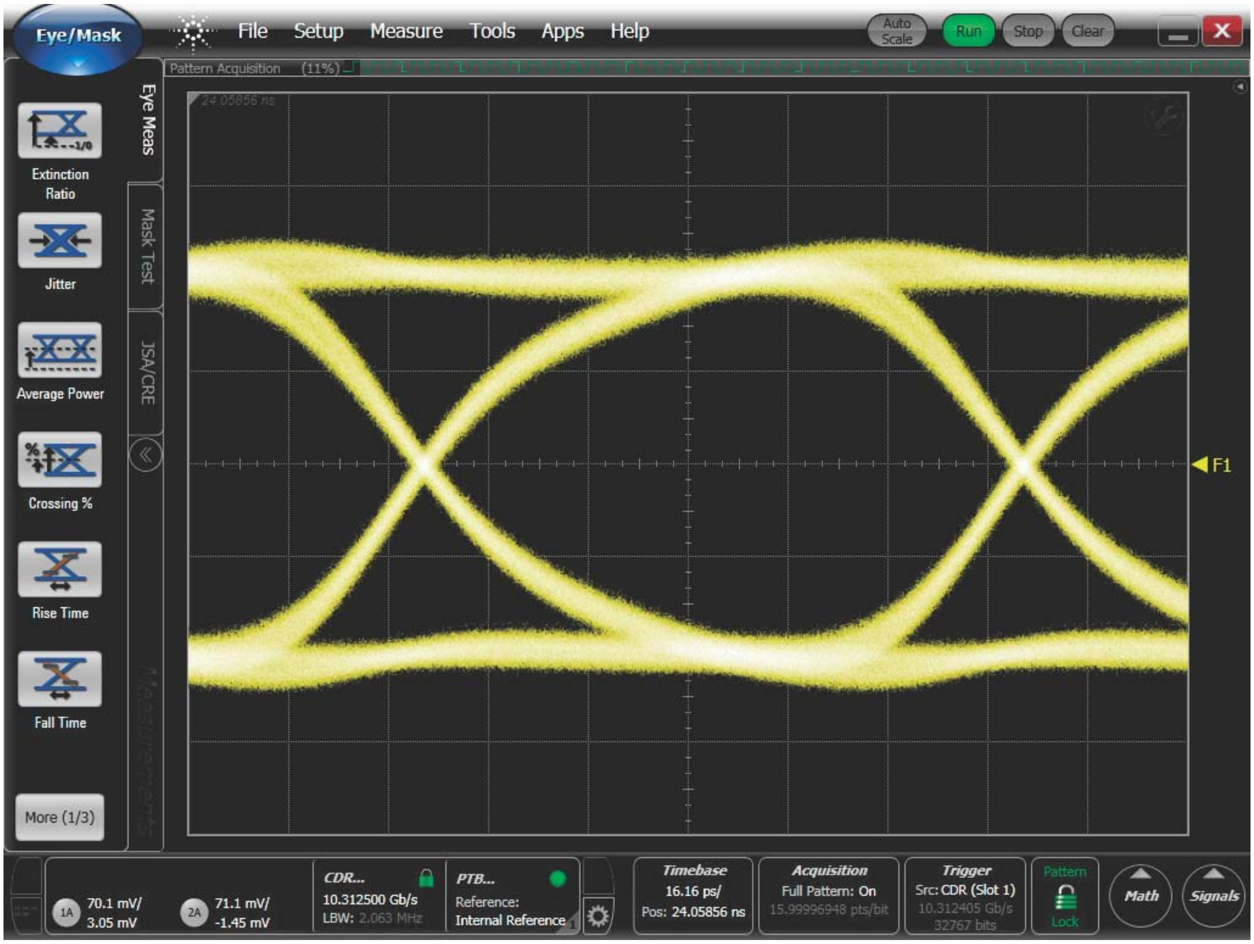
Name	Value
volt_unsigned[21:0]	1987708
error[20:0]	3

Figure 9: **Error and Volt Analog View**

The error signal represents the accumulated output of the on-chip phase detector. This is nominally 0 when in lock, and the volt is the filtered output to the SDM port where the value represents the current frequency generated by the QPLL. The full range of volt represents the dynamic operating range of the SDM, a 1/64 region within the range N to N+1 with the region being selected by the coarse tune value. So in this example, the coarse tune value is 0. The upper 18 bits of volt are used as part of the DPLL loop to make the entire SDM control word.

When UltraScale+ devices are used, the FRACXO control is different because there are no sub-tuning bands as in UltraScale devices. This means a more flexible approach is adopted as outlined in FRACXO DPLL Architecture Overview. In both UltraScale and UltraScale+ devices, a tuning limit of ±200 ppm should be observed from the nominal QPLL frequency at QPLL reset.

Figure 10 and Figure 11 show the output waveform and jitter decomposition, respectively, of the output data when the fPLL GTY transceiver with FRACXO is generating a nominal 10.3125 Gb/s locked to the input data. TX post cursor pre-emphasis on the GTY transceiver has been set to overcome channel losses and minimize inter-symbol interference (ISI).



1A 70.1 mV/ 3.05 mV

2A 71.1 mV/ -1.45 mV

CDR... 10.312500 Gb/s LBW: 2.063 MHz

PTB... Reference: Internal Reference

Timebase 16.16 ps/ Pos: 24.05856 ns

Acquisition Full Pattern: On 15.99996948 pts/bit

Trigger Src: CDR (Slot 1) 10.312405 Gb/s 32767 bits

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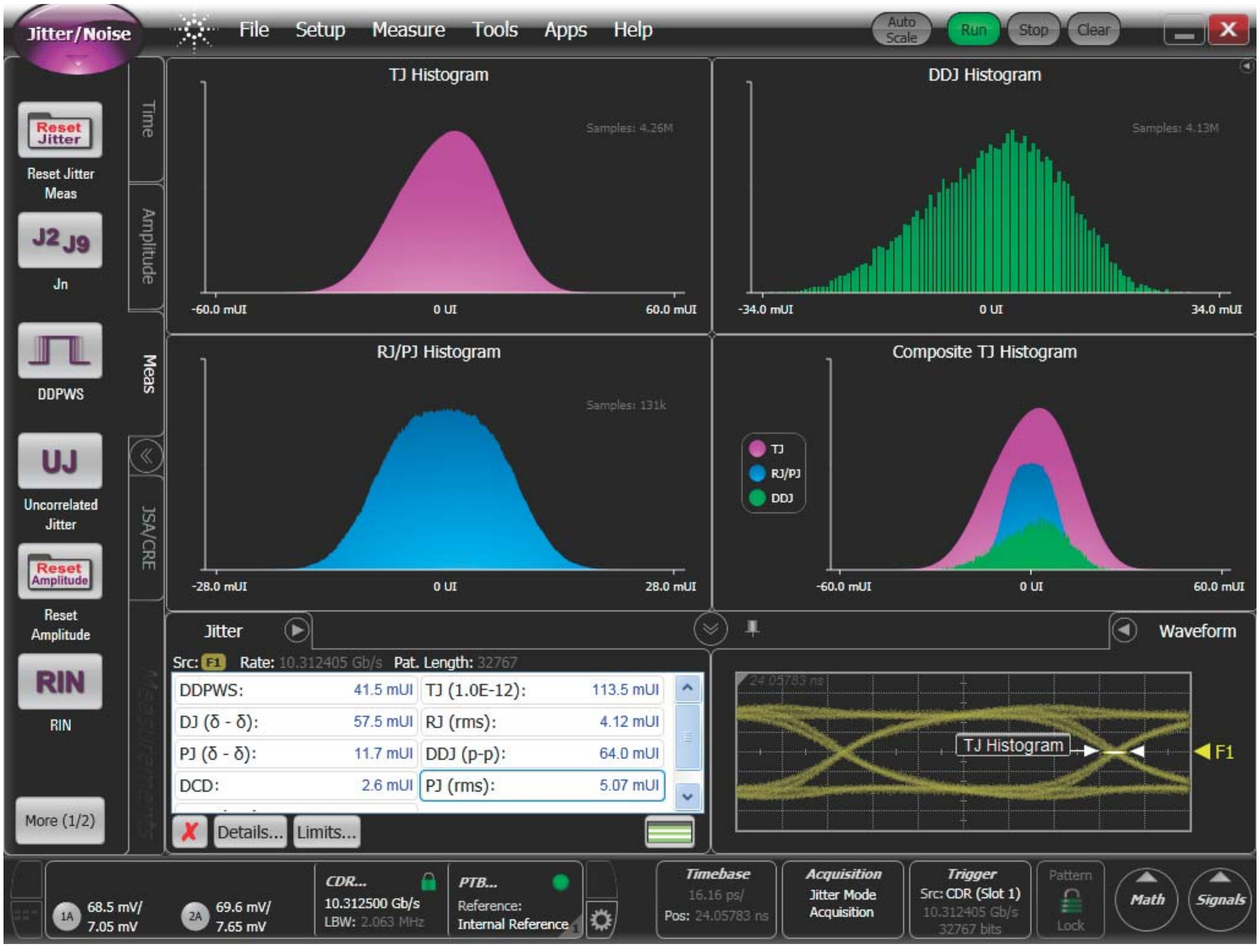
Figure 10: **10.3125 Gb/s Output**



Jitter

Src: F1 Rate: 10.312405 Gb/s Pat. Length: 32767

DDPWS:	41.5 mUI	TJ (1.0E-12):	113.5 mUI
DJ (δ - δ):	57.5 mUI	RJ (rms):	4.12 mUI
PJ (δ - δ):	11.7 mUI	DDJ (p-p):	64.0 mUI
DCD:	2.6 mUI	PJ (rms):	5.07 mUI

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Figure 11: **10.3125 Gb/s Output Jitter Decomposition**

FRACXO DPLL Architecture Overview

A complete digital PLL and clock cleaner can be created using a system consisting of the fPLL in the QPLL, the transceiver channel, the FRACXO DPLL, and an external clock source (XO). The FRACXO macro operation for the QPLL and channel is shown in the functional block diagram of Figure 2.

The reference clock or pulse is applied to REF_CLK_I. Because the phase frequency detector (PFD) is positive edge triggered, the input can be any digital clock or enable and can be sourced either from local FPGA logic resources or any clock buffer network. This may be also come from an external input from a user-defined pin.

The FRACXO clock is derived from the TXOUTCLK and is normally shared with the TXUSERCLK used for the data interface. The programmable dividers R and V are used to scale the FRACXO clock and the reference clk (REF_CLK_I) to a common compare frequency where the DPLL can lock the TXOUTCLK, and therefore the QPLL, to the reference input.

The error values (accumulated phase values) are input to the filter block that has a traditional digital proportional integral control circuit. The volt value is applied to the SDM input port on the QPLL that directly controls the tune frequency of the QPLL. The DPLL itself runs on two clocks, the main TXOUTCLK and a slower CE_DSP that sets the integration period for phase error accumulation and therefore the base DSP loop update rate.

The frequency response of the DPLL, the transfer function between REF_CLK_I and the QPLL output, is controlled primarily by the G_1, G_2, and RANGE values, and for loop stability G_2 is always greater than G_1. The response is a factor of TXOUTCLK frequency, V divider, and CE_DSP_RATE together with the G_1, G_2, and RANGE settings. To aid the frequency response estimation, a spreadsheet is provided with the design files.

Additional ports on the FRACXO design can be used as follows:

- CENTRE_F: Sets the start SDM value for the system. Applies to UltraScale+ devices only.
- SDM_MAX_I: Programmable limiter value to set the maximum value applied to the SDMDATA port. Applies to UltraScale+ devices only.
- SDM_MIN_I: Programmable limiter value to set the minimum value applied to the SDMDATA port. Applies to UltraScale+ devices only.
- DON_I: Adds dither to the PFD to linearize the base quantization steps.
- DISABLE: Disables the Volt output from the DPLL allowing the SDM value for CENTRE_F to be used as a manual override. Applies to UltraScale+ devices only.
- HOLD: Freezes the volt value at its current value and can be used to maintain the current output frequency when the input reference is removed.
- SDM(23:18): Coarse tune for the fractional QPLL SDM value. Must be constant in operation. Applies to GTY transceivers in UltraScale devices only.
- OFFSET_PPM: Can be enabled to provide a user control input to the SDM port for frequency manual control. Applies to GTY transceivers in UltraScale devices only.

Normally the circuit uses one BUFG_GT per line rate generated. When locked, this clock is synchronous with the reference clock and can be used for other user downstream logic. Figure 12 shows a detailed diagram of the DPLL for GTY transceivers in UltraScale devices.

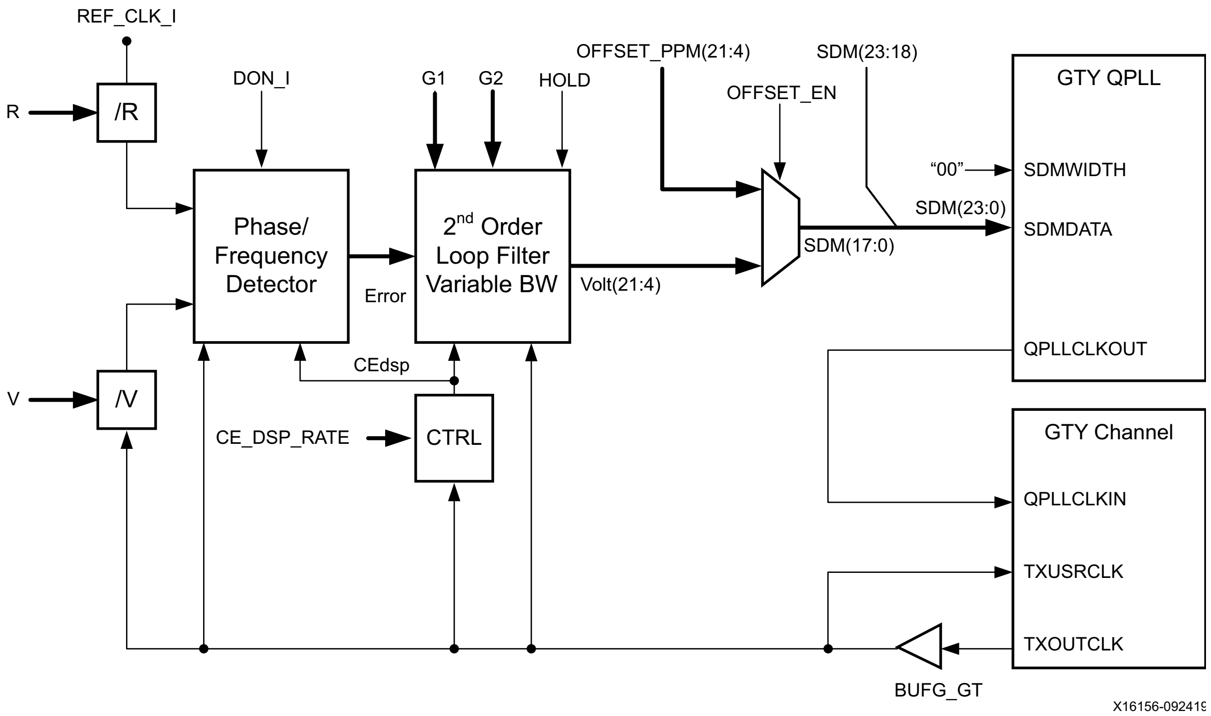

Figure 12: **DPLL for GTY Transceiver in UltraScale Devices**

Figure 13 shows a detailed diagram of the DPLL for GTH, GTM, and GTY transceivers in UltraScale+ devices.

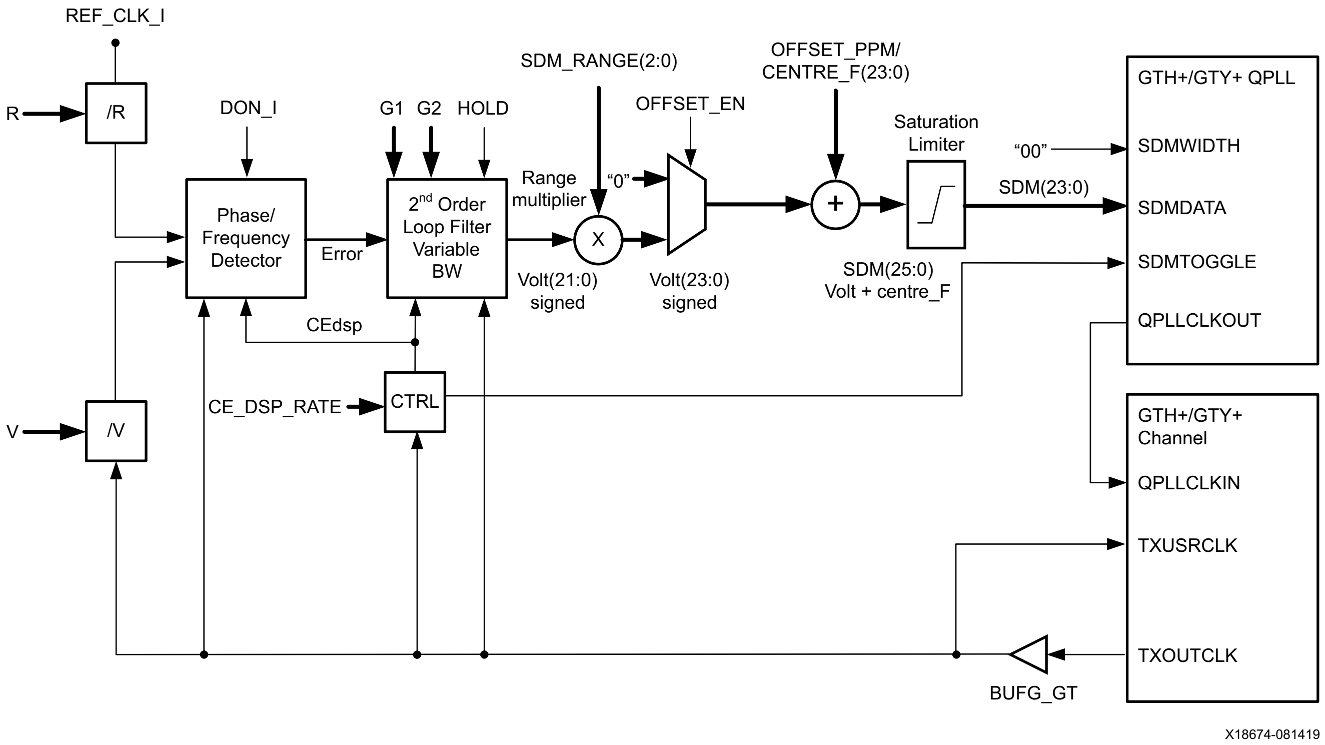

Figure 13: **DPLL for GTH, GTM, and GTY Transceivers in UltraScale+ Devices**

Designing with FRACXO

Physical Interface

Table 1 through Table 3 show the port definitions.

Table 1: **Clocks, Reset, and Interface to the Transceiver Ports**

Signal Name	Direction	Description
RESET_I	Input	Synchronous reset. Active-High. Needs eight clock cycles to reset correctly.
REF_CLK_I	Input	Reference clock. Can be any clock (local, BUFG, pulse, etc.).
TXOUTCLK_I	Input	Connects to TXOUTCLK of the serial transceiver via a BUFG_GT.
SDM_DATA_O[24:0]	Output	Connects to SDM0/1DATA on the transceiver.
SDM_TOGGLE_O	Output	Connects to SDM0/1TOGGLE on the transceiver. GTH, GTM, and GTY transceivers in UltraScale+ devices only

Table 2: **Debug Ports**

Signal Name	Direction	Description
ERROR_O[20:0]	Output	Output of phase detector. Signed number.
VOLT_O[21:0]	Output	Output of low-pass filter. Signed number. Only [21:4] are used.
CE_PI_O	Output	Clock enable for accumulator.
CE_PI2_O	Output	Clock enable for low-pass filter and digital-to-analog converter (DAC).
CE_DSP_O	Output	Reset phase detector counters, load phase detector error into the low-pass filter.
OVF_PD	Output	Overflow in the phase detector.
OVF_AB	Output	Saturation of the low-pass filter inputs.
OVF_INT	Output	Saturation of the low-pass filter integrator.
OVF_VOLT	Output	Saturation of the low-pass filter output.

Table 3: **FRACXO Loop Parameters**

Signal Name	Direction	Description
G1[4:0]	Input	Filter linear path gain, with range: • –8 to 20 valid • –8 to –1 coded as twos complement • 0 to 20 coded as positive binary
G2[4:0]	Input	Filter integrator path gain: range 0 to 20.
R[15:0]	Input	Reference divider: range `0` to `65535`. Divides by R+2.
V[15:0]	Input	TXOUTCLK_I divider: range `0` to `65535`. Divides by V+2.
RANGE[2:0]	Input	Gain decrease range 0 to 7. Effective gain $1/2^{(range*2)}$. UltraScale+ devices only.
CENTRE_F[23:0]	Input	Sets the nominal SDM value. UltraScale+ devices only.

Table 3: **FRACXO Loop Parameters *(Cont'd)***

Signal Name	Direction	Description
SDM_MAX[23:0]	Input	Sets the maximum limit value for SDM. Must be greater than the CENTRE_F value. UltraScale+ devices only.
SDM_MIN[23:0]	Input	Sets the minimum limit value for SDM. Must be lesser than the CENTRE_F value. UltraScale+ devices only.
SDM_COARSE_I[5:0]	Input	Coarse tune of the fPLL. GTY transceivers in UltraScale devices only.
CE_DSP_RATE[23:0]	Input	DSP divider. Default `x0007FFh`. Control CE_DSP rate.
VSIGCE_I	Input	Clock enable of the TXOUTCLK_I divider. Connects to `1` for normal operation.
VSIGCE_O	Output	Reserved. Floating.
RSIGCE_I	Input	Clock enable of reference divider. Connects to `1` for normal operation.
C_I[7:0]	Input	Reserved. Connect to `0`.
P_I[9:0]	Input	Reserved. Connect to `0`.
N_I[9:0]	Input	Reserved. Connect to `0`.
OFFSET_PPM[21:0]	Input	Direct frequency offset control. Signed number. OFFSET_PPM overwrites the output of the low-pass filter (VOLT_O) when OFFSET_EN is High. The top 18 bits are used with SDM_COARSE_I to form SDM_DATA_O. UltraScale devices only.
OFFSET_EN	Input	Enable direct frequency offset control input. Active-High. Enables OFFSET_PPM input to overwrite output of low-pass filter (Volt). UltraScale devices only.
HOLD	Input	Hold low-pass filter output value (Volt). Clock enable of Volt that stops Volt to the latest known ppm.
DISABLE	Input	Disconnects the Volt control input from the SDM sum port. Forces the SDM output to the CENTRE_F value. UltraScale+ devices only.
DON_I	Input	Potential jitter reduction. Active-High.

Interface Operation

General Operation

The FRACXO parameters (V, R, SDM_COARSE, CE_DSP_RATE) can affect the FRACXO lock if changed, therefore they are considered pseudo-static inputs. The gains G_1 and G_2 can be changed without loss of lock. All input and output signals to/from the FRACXO are synchronous to TXOUTCLK_I except REF_CLK_I and R. Figure 14 shows the timing dependency between TXOUTCLK_I and the main debug outputs.

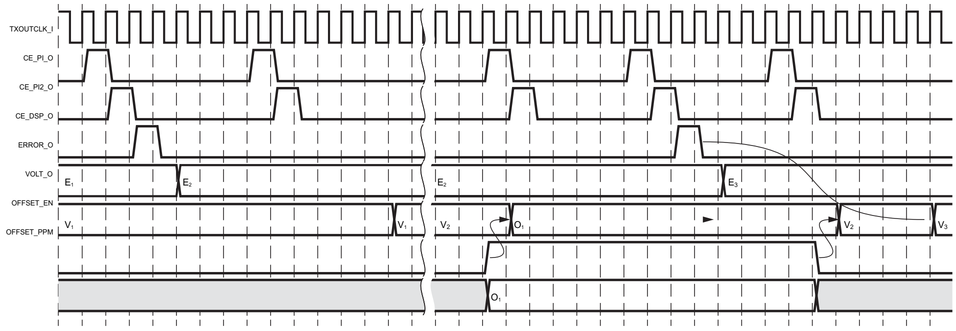

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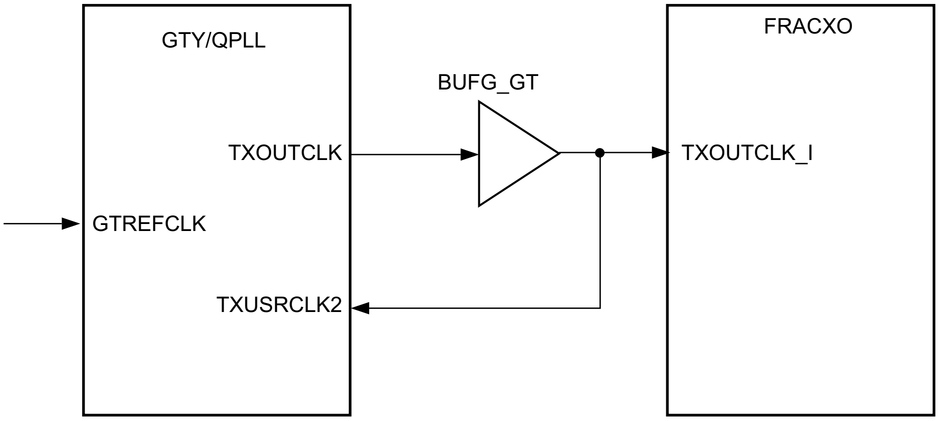
Figure 14: **Timing Waveforms of Main Debug Outputs**

Reset Considerations

The FRACXO main reset RESET_I requires a minimum of eight TXOUTCLK_I cycles to reset the FRACXO correctly. When applied, RESET_I resets all blocks, including the phase detector and low-pass filter. When releasing RESET_I, the first phase detector output (ERROR_O) is zero, and the first word written in the transceiver fractional PLL is zero. The transceiver QPLL and TX physical medium attachment (PMA) reset sequence must be completed before the FRACXO reset is released for operation.

UltraScale FPGA Transceiver Clocking

The primary clocking scheme is detailed in Figure 15. The transceiver TXOUTCLK connects to a BUFG_GT that drives the FRACXO input clocks TXOUTCLK_I.



X15941-020216

Figure 15: **UltraScale FPGA FRACXO Clocking Scheme**

HOLD Input Operation

The HOLD input is a clock enable to the low-pass filter integrator and output (VOLT_O). While HOLD is High, the phase detector continues to operate as normal. When HOLD returns to Low, the low-pass filter output is not synchronized anymore with the phase detector. Figure 16 illustrates this behavior.

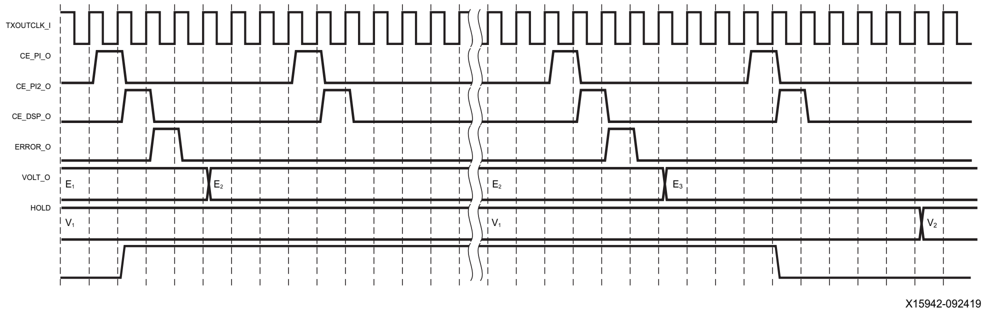


Figure 16: **HOLD Input Operation**

Direct Offset Control

OFFSET_PPM and OFFSET_EN allow direct control of the frequency offset. When OFFSET_EN is High, the output of the low-pass filter (VOLT_O) takes the OFFSET_PPM value. During this time, the phase detector and low-pass filter integrator operate normally. When OFFSET_EN returns to Low, the output of the low-pass filter (VOLT_O) takes the current value calculated by the phase detector and low-pass filter. Figure 17 illustrates this behavior.

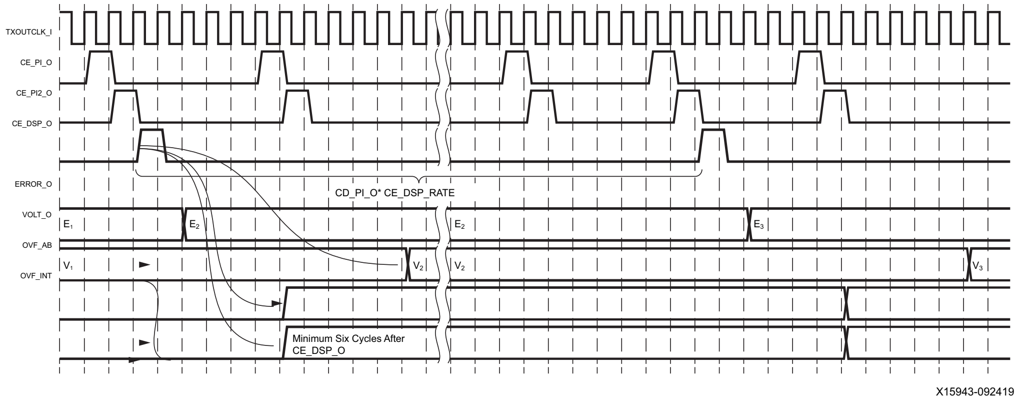


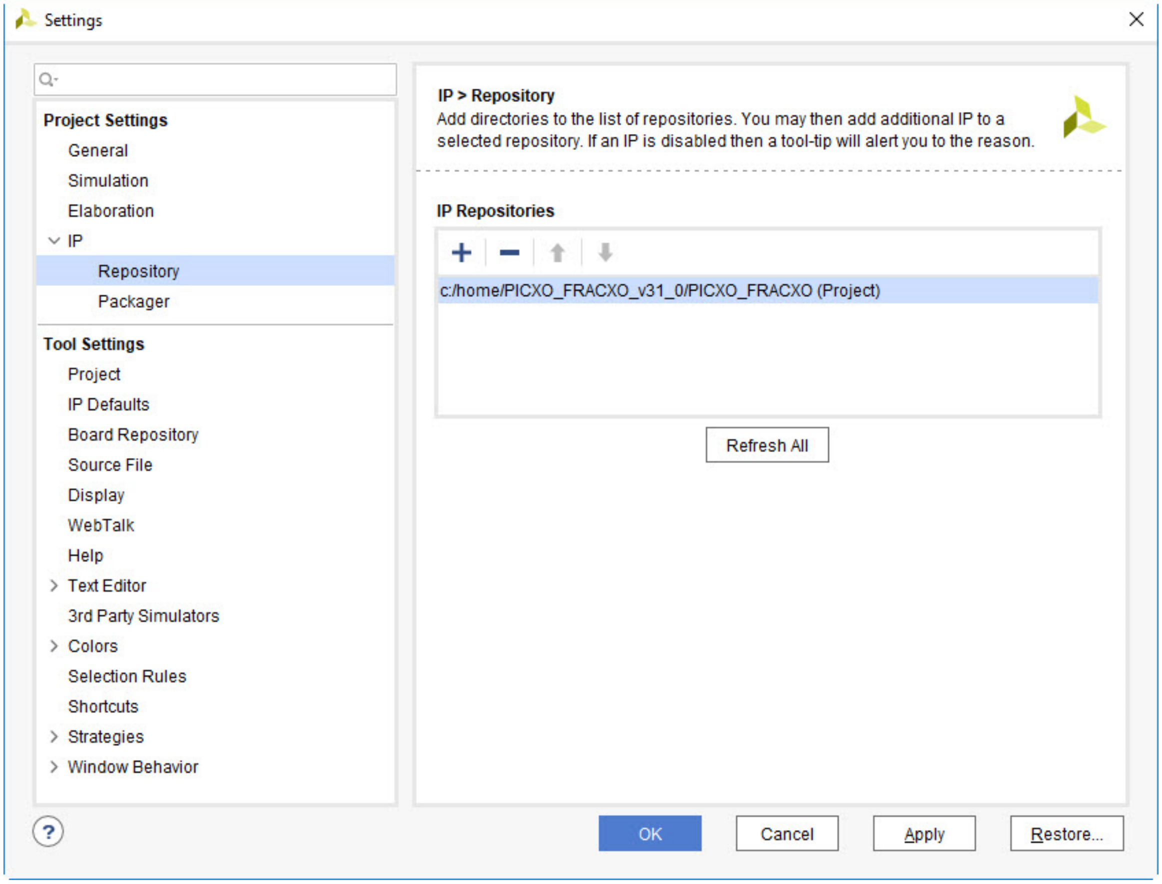
Figure 17: **Direct Offset Control**

Implementation

Vivado Tools Implementation

The FRACXO design is delivered as a custom IP. This section describes the steps to add the design to a project:

1. Unzip the file in a location.
2. Add the IP repository to the project by selecting **Tools > Project Options**, select **IP** on the left pan, click **Add Repository**, and select the **PICXO_FRACXO** folder (Figure 18).



IP > Repository

Add directories to the list of repositories. You may then add additional IP to a selected repository. If an IP is disabled then a tool-tip will alert you to the reason.

IP Repositories

c:/home/PICXO_FRACXO_v31_0/PICXO_FRACXO (Project)

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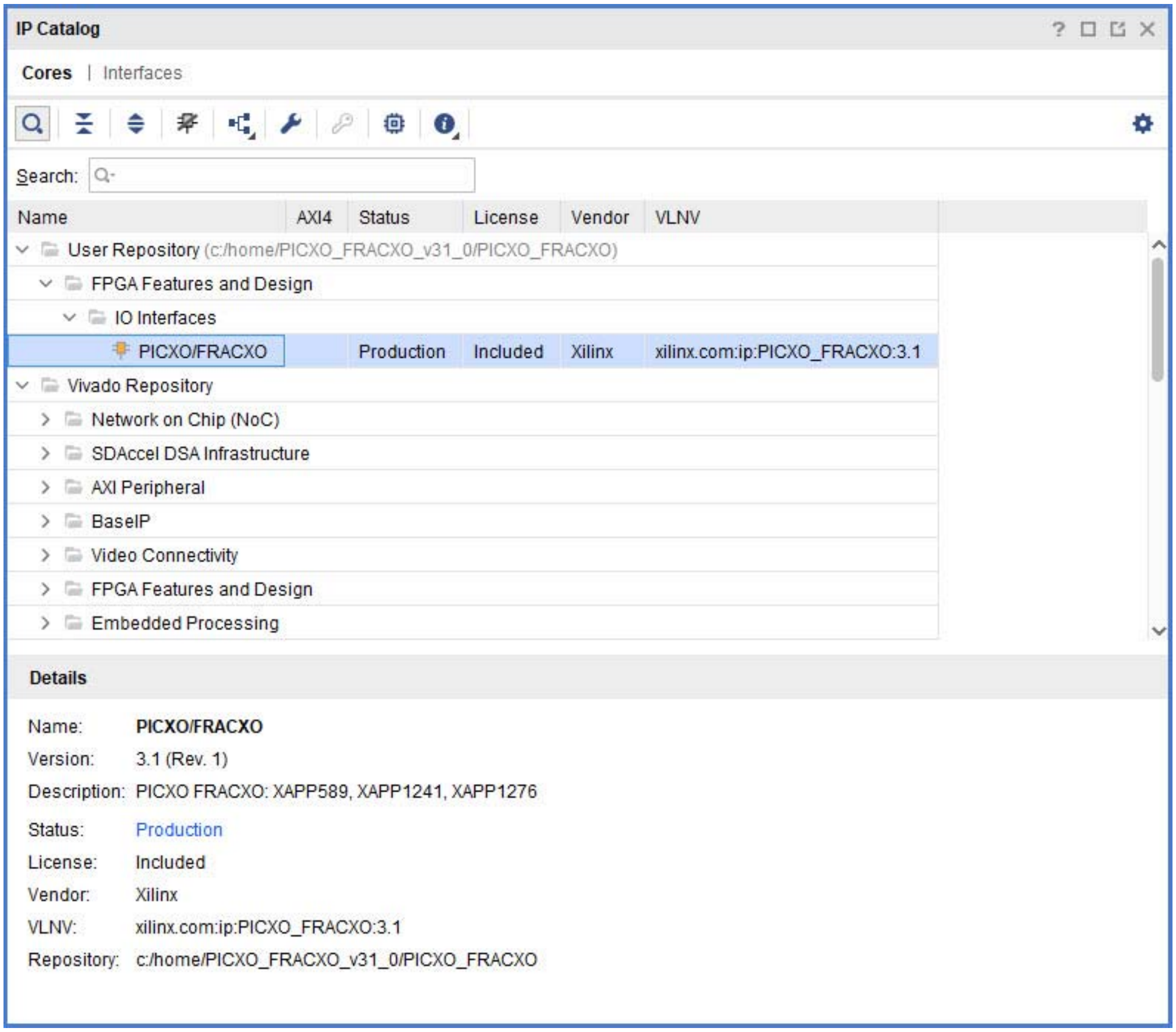
Figure 18: **Project Settings**

3. Select the IP catalog. The PICXO/FRACXO IP is under **FPGA Features and Design > IO Interfaces** (Figure 19).



Name	AXI4	Status	License	Vendor	VLNV
User Repository (c:/home/PICXO_FRACXO_v31_0/PICXO_FRACXO)					
FPGA Features and Design					
IO Interfaces					
PICXO/FRACXO		Production	Included	Xilinx	xilinx.com:ip:PICXO_FRACXO:3.1
Vivado Repository					
Network on Chip (NoC)					
SDAccel DSA Infrastructure					
AXI Peripheral					
BaseIP					
Video Connectivity					
FPGA Features and Design					
Embedded Processing					

Name: PICXO/FRACXO
Version: 3.1 (Rev. 1)
Description: PICXO FRACXO: XAPP589, XAPP1241, XAPP1276
Status: Production
License: Included
Vendor: Xilinx
VLNV: xilinx.com:ip:PICXO_FRACXO:3.1
Repository: c:/home/PICXO_FRACXO_v31_0/PICXO_FRACXO

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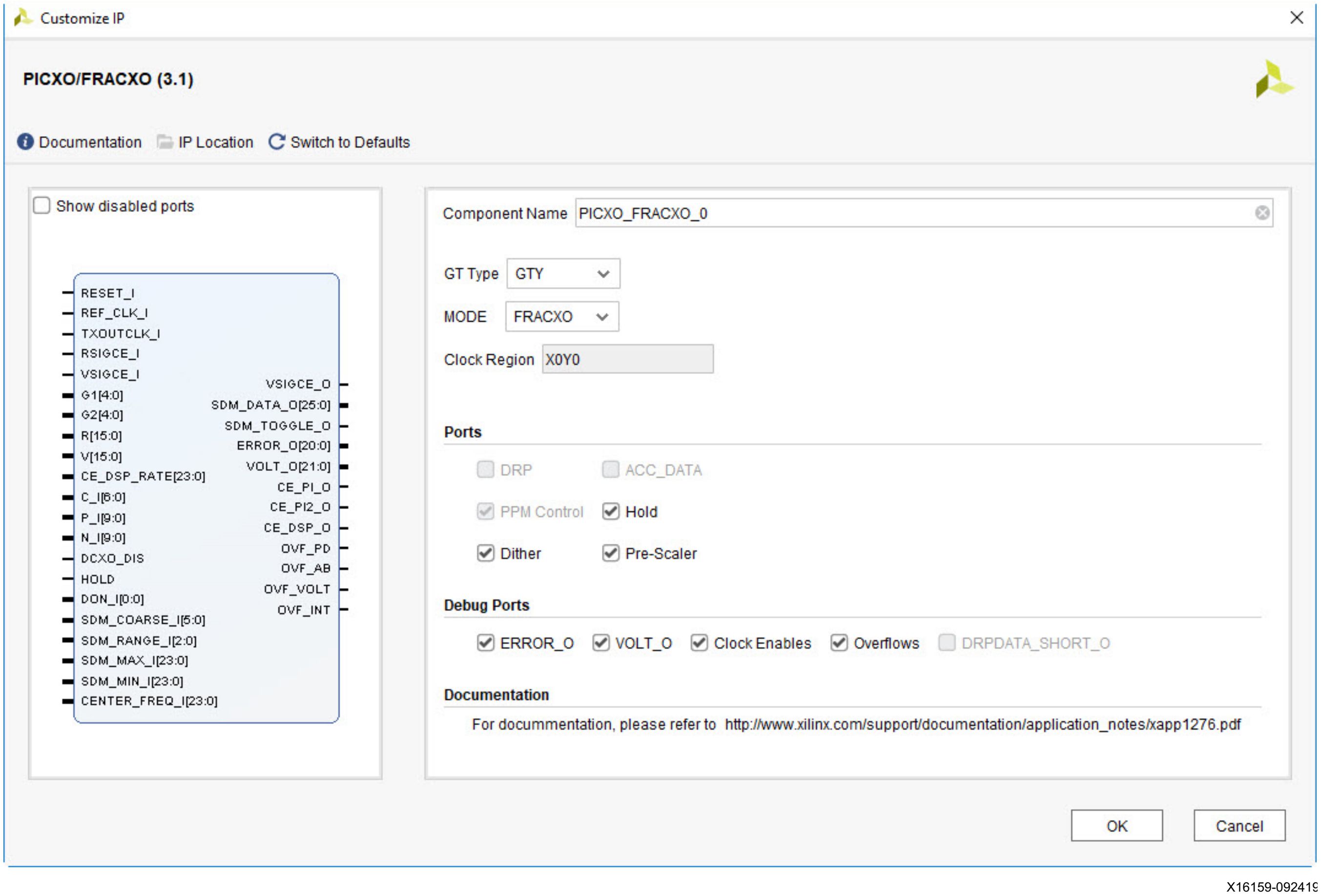
Figure 19: **IP Catalog**

4. Right-click **PICXO/FRACXO** and select **Customize IP**.

5. Select the IP module name, the type of GT, and the FRACXO mode. Click **OK** (Figure 20).



PICXO/FRACXO (3.1)

□ Show disabled ports

Component Name: PICXO_FRACXO_0

GT Type: GTY

MODE: FRACXO

Clock Region: X0Y0

Ports

□ DRP □ ACC_DATA

☑ PPM Control ☑ Hold

☑ Dither ☑ Pre-Scaler

Debug Ports

☑ ERROR_O ☑ VOLT_O ☑ Clock Enables ☑ Overflows □ DRPDATA_SHORT_O

Documentation

For documentation, please refer to http://www.xilinx.com/support/documentation/application_notes/xapp1276.pdf

Figure 20: **Customize IP**

6. The example design can be generated by selecting the IP source, right-clicking, and selecting **generate example design**.

The transceiver associated with the FRACXO must be constrained to a specific location. Period constraints are necessary on TXOUTCLK_I and REFCLK_I.

Mandatory Conditions and Limitations

UltraScale and UltraScale+ Device Transceiver

- QPLL0/1 SDM functionality and ports must be enabled.[1]
- QPLL0/1 must clock transceiver channel being used.
- TXPLLCLKSEL must be set to `10` or `11`.

[1] For each transceiver, the SDM functionality needs to be selected at wrapper and example design generation to ensure the correct attributes are set to enable the QPLL fractional capability.

A DRC check is performed during opt_design, and a critical warning is generated if the above conditions are not met. No DRC check is performed for the reference clock frequency setting–it is your responsibility to ensure that the FRACXO covers the output frequency range required.

Reference Design

The reference design files are based on the UltraScale transceiver wrapper v1.0 [Ref 3]. The design targets the VCU108 development platforms that loopback the receive data to the transmitter. The FRACXO instance locks the transmitter to the recovered clock RXRECLK.

The output error_o of the phase/frequency detector can be captured when CE_DSP_O is High to monitor the FRACXO response. When locked, ERROR_O should oscillate around 0 (see Figure 9). Simulation of the example design is not supported.

Download the reference design files for this application note from the Xilinx website. Table 4 shows the reference design matrix.

Table 4: **Reference Design Matrix**

Parameter	Description
General	
Developer name	David Taylor, Matt Klein, Vincent Vendramini, and Antonello Di Fresco
Target devices	Virtex UltraScale XCVU095-2FFVA2104E
Source code provided	Yes
Source code format	VHDL
Design uses code and IP from existing Xilinx application note and reference designs or third party	Yes, Vivado ILA and VIO
Simulation	
Functional simulation performed	No
Timing simulation performed	No
Test bench used for functional and timing simulations	No
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/versions used	Vivado Design Suite 2019.1
Implementation software tools/versions used	Vivado Design Suite 2019.1
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	VCU108

Table 5 shows the device utilization table for the reference design.

Table 5: **Device Utilization and Performance for Reference Design (Vivado Design Suite 2016.1)**

	Zynq UltraScale+ MPSoC (One GTH Transceiver)	Virtex UltraScale (One GTY Transceiver)
	Full Design	Full Design
CLB LUTs	3087	3076
CLB registers	4514	4510
Occupied CLB[1]	716	835
BlockRAM	14	13.5
BUFGCE/BUFG_GT	3/2	3/2
GTY transceivers	1	1
MMCM	0	0

Notes:

1. The number of occupied slices can vary depending on packing results.

Table 6 shows the statistics and performance expectations for a standalone FRACXO.

Table 6: **Statistics and Performance Expectations for a Standalone FRACXO (Vivado Design Suite 2016.1)**

Target Devices	Zynq UltraScale+ MPSoC (GTH Transceiver)	Virtex UltraScale (GTY Transceiver)
LUTs	763	764
Registers	919	919
SRLs	33	33
Maximum FRACXO clock rate	Speed grade dependent, matches TXUSRCLK2 maximum frequency	Speed grade dependent, TXUSRCLK2 maximum frequency

References

1. *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)* (XAPP589)
2. *All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs)* (XAPP1241)
3. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
4. *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893)
5. *VCU108 Evaluation Board User Guide* (UG1066)
6. *Virtex UltraScale+ FPGAs GTM Transceivers User Guide* (UG581)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/27/2016	1.0	Initial Xilinx release.
04/11/2017	1.1	Updated transceiver operating frequency in Summary. Expanded footnote on page 2. Updated paragraphs after Figure 2. Added paragraph about volt output bit mappings after Figure 9. Updated description of SDM port in FRACXO DPLL Architecture Overview. Added Figure 13. Added SDM_TOGGLE_O to Table 1. Updated SDM_COARSE_I[5:0] description in Table 3. Added footnote to first bullet in UltraScale and UltraScale+ Device Transceiver.
10/30/2019	1.2	Added GTM transceivers throughout. Updated footnote on page 2. Updated description of maximum dynamic frequency shift and SDM capability in Summary. Updated description of FRACXO control in fPLL FRACXO Example Design. Added CENTRE_F, SDM_MAX_I, SDM_MIN_I, and DISABLE to list of ports in FRACXO DPLL Architecture Overview. Updated Figure 13, Figure 18, Figure 19, and Figure 20. In Table 3, updated descriptions of G1[4:0], G2[4:0], CE_DSP_RATE[23:0], OFFSET_PPM[21:0], and OFFSET_EN, and added RANGE[2:0], CENTRE_F[23:0], SDM_MAX[23:0], SDM_MIN[23:0], and DISABLE. Updated Vivado software version in Table 4.
01/28/2022	1.2.1	Editorial updates only. No technical content changes.

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