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AXI Thin Film Transistor (TFT) Controller on the 7 Series Platform

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Summary

This application note demonstrates a simple integrated display system using the LogiCORE™ IP AXI Thin Film Transistor (TFT) core on the Kintex®-7 FPGA KC705 Evaluation Kit. The AXI TFT Controller core supports DVI and VGA modes with a 640x480 resolution using a frame buffer in DDR memory. This application note details implementation of the AXI TFT Controller core in DVI mode using the Vivado® Design Suite IP integrator feature with the KC705 Evaluation board. An example of frame buffer management is also provided.

Included Systems

The reference design is created and built using the Vivado Design Suite: System Edition 2014.1. The Vivado Design Suite helps simplify the task of instantiating, configuring, and connecting IP blocks to form complex integrated systems. The design also includes a software application built with the Xilinx Software Development Kit (SDK). The application runs on the MicroBlaze™ embedded processor and implements control, status and monitoring functions. Complete IP integrator and SDK project files are provided with the reference design to allow easy examination and modification of the design or to provide a template for beginning a new design.

Included with this application note is one reference system, `tft_top_kc705`, and one software application, `app_invader`, available in the ZIP file, `xapp1215-axi-tft-on-7-series.zip`. See the [Reference Design](#) section.

Introduction

Designing the proper architecture for a complex, FPGA-based video system is a challenging task. The critical elements for meeting the system performance requirements are the interconnect, memory architecture, and video timing.

The AXI TFT Controller core is a hardware display controller for a 640x480 resolution display device. The core is capable of displaying up to 256K colors using either a VGA or DVI interface. The design features an AXI4 master interface to read video data from an attached memory device and transfer the data to the TFT display. The design also includes an AXI4 slave interface to provide register access.

The AXI TFT Controller core stores pixel data in an internal line buffer from which it is transferred to the TFT device with the necessary timing to correctly display the image. This process repeats continuously for every line and frame for the 640x480 TFT display.

Hardware Requirements

The AXI TFT display controller reference design requires these hardware components:

- One Kintex-7 FPGA KC705 evaluation board (Rev. 1.1)
- One KC705 Universal 12v power adapter
- One Avnet DVI I/O FMC module (model AES-FMC-DVI-G)
- One high-quality HDMI™ cable
- One TFT display device
- One USB Type-A to Mini-B 5-pin cable
- One USB Type-A to Micro-B 5-pin cable

Software Requirements

Software tool requirements for the AXI TFT display controller:

- Vivado Design Suite 2014.1: System Edition

Reference System Specifics

The design contains the minimal number of components required to evaluate the AXI TFT Controller core. To showcase the capabilities of the core, a simple game based on Space Invaders is included in the software application.

A block diagram of the design is shown in [Figure 1](#). The IP cores and their base and high address values are shown in [Table 1](#). The TFT controller output is configured for a 12-bit DVI interface. An external IIC bus interface module is used by the software application to configure the DVI I/O FMC transmitter module.

DDR memory is used to store the video data and application code. When enabled, the AXI TFT Controller core begins reading video data from DDR memory through the AXI4 interface using burst transactions. A GPIO core is used to map the onboard push buttons used to control the game.

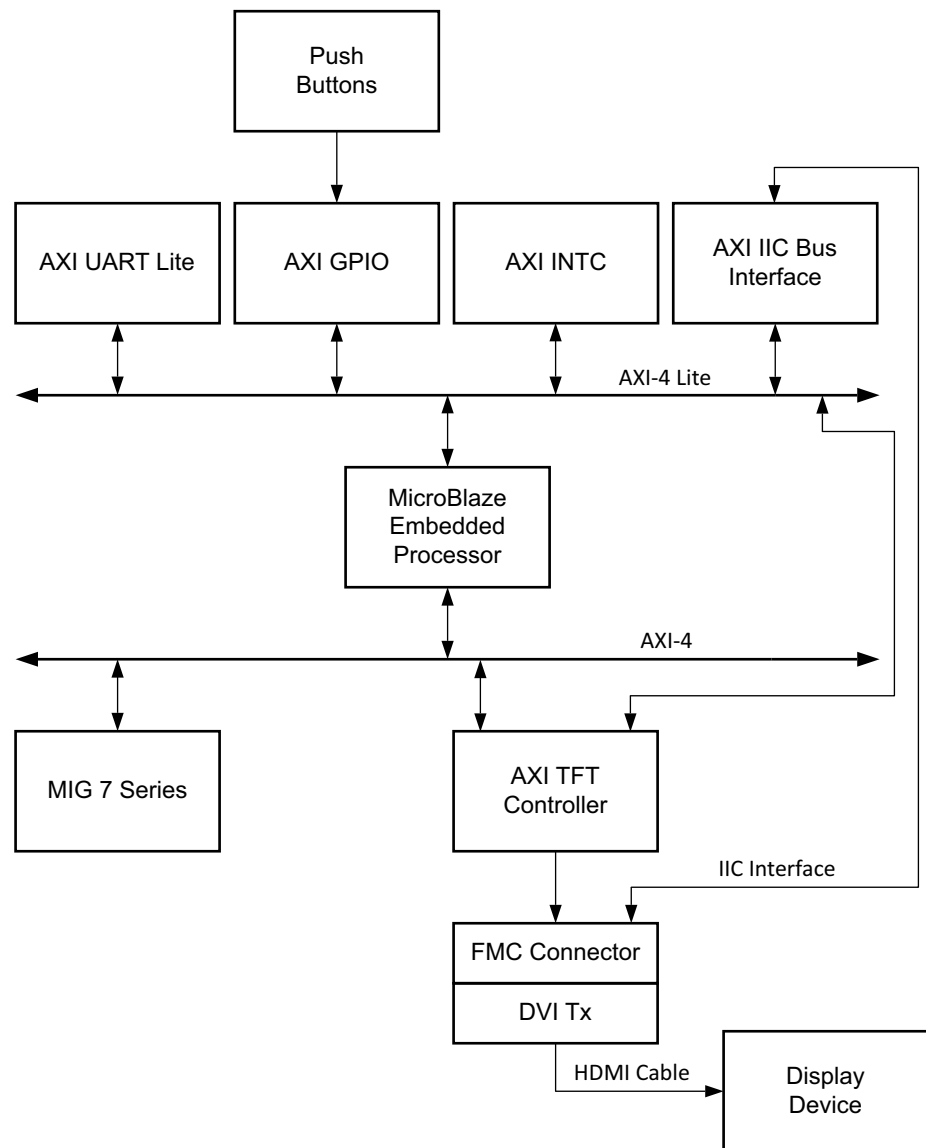


Figure 1: TFT Controller System Block Diagram

Table 1: TFT Controller System Address Map

Core	Base Address	High Address
axi_gpio_0	0x40000000	0x4000FFFF
axi_tft_0	0x44A00000	0x44A0FFFF
mig	0x80000000	0xBFFFFFFF
axi_uartlite_0	0x40600000	0x4060FFFF
axi_iic_0	0x40800000	0x4080FFFF
axi_mb_intc	0x41200000	0x4120FFFF
lmb_bram	0x00000000	0x0001FFFF

Software Application

The software application includes a basic display test and a simple game. The application demonstrates display buffer management and synchronization with the AXI TFT Controller core. It includes a simple game based on Space Invaders. Controls to move the onscreen object are mapped to GPIO push buttons on the KC705 evaluation board.

The game scenario involves enemy objects moving left and right as they descend toward the shooter object at the bottom of the screen while firing green projectiles. The player moves the shooter object right or left to avoid the green projectiles and fires white projectiles at the enemy objects. A row of objects above the shooter provide protection from the projectiles. When all enemy objects are destroyed, a new level is presented.

The left/right push buttons move the shooter left and right while the center push button fires projectiles. The software application manages the display of all moving objects on the screen.

Building Hardware

This section covers rebuilding the hardware design using Vivado IP integrator. Ensure that Vivado design suite 2014.1: System Edition is installed prior to rebuilding the project.

Vivado Tools Design Flow

Follow these steps to open and rebuild the TFT controller design:

1. Unzip the reference design files accompanying this application note (see [Reference Design, page 13](#)). The local folder into which the design files are placed is subsequently referred to as <unzip dir>.

2. Launch Vivado Design Suite.

Windows:

Double-click the Vivado 2014.1 shortcut icon on the desktop or select **Start > Xilinx Design Tools > Vivado 2014.1 > Vivado 2014.1**.

Linux:

```
% vivado
```

3. Select **Open Project** ([Figure 2](#)).

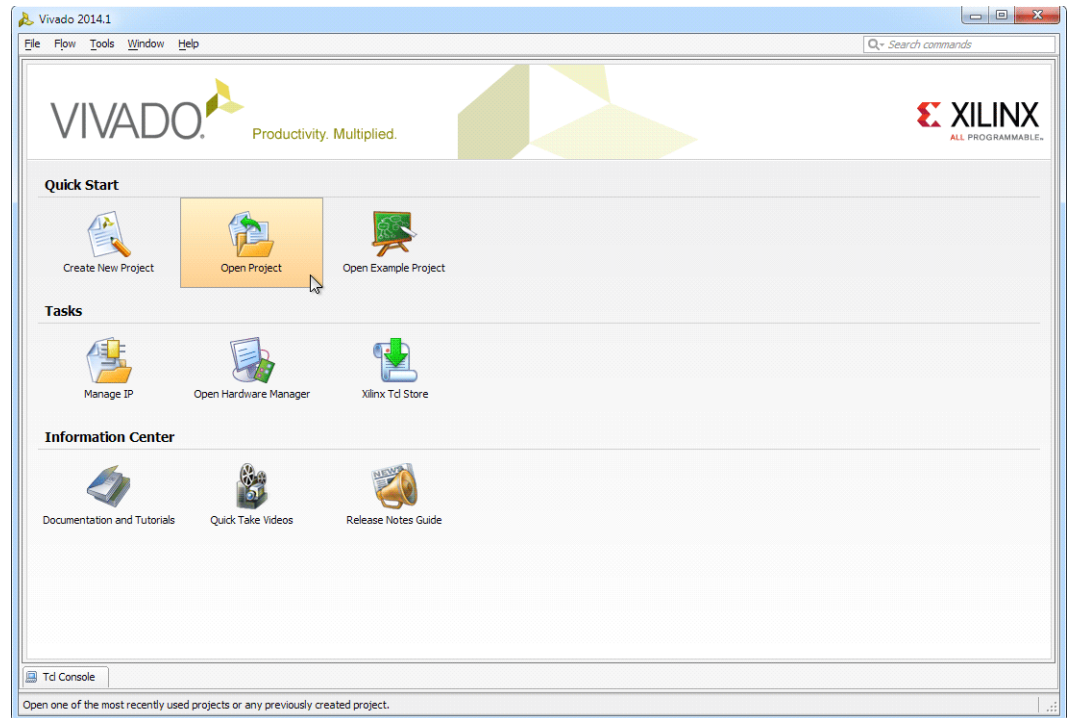


Figure 2: Vivado IDE

4. Select `<unzip dir>/XAPP1215/HW/project_1/project_1.xpr` and click **OK** (Figure 3).

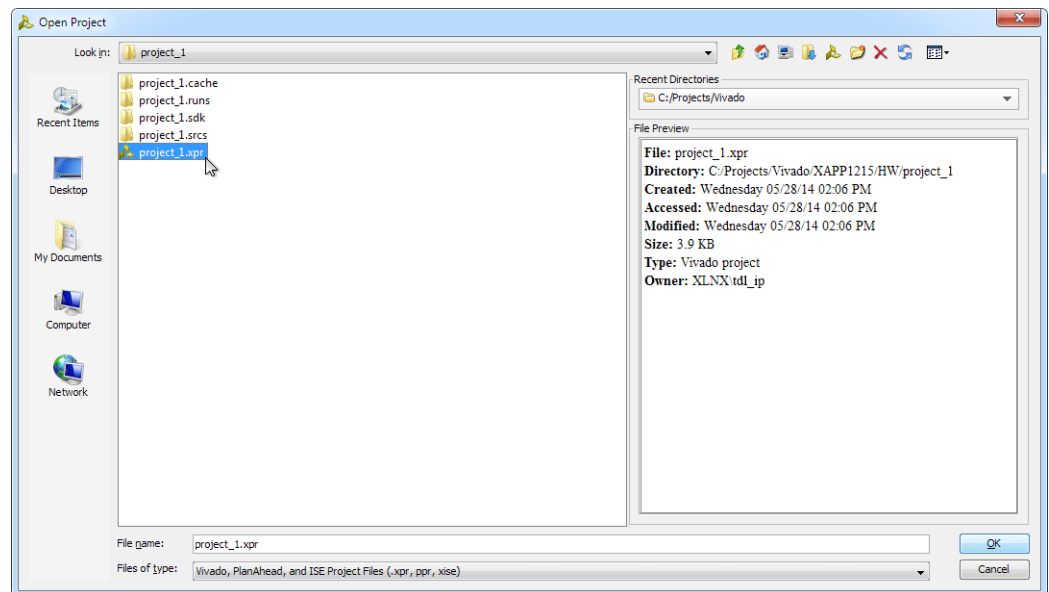


Figure 3: Open Project

5. Select **Flow > Generate Bitstream** or click **Generate Bitstream** under **Program and Debug** in the Flow Navigator pane (Figure 4). Click **Yes** if prompted to run Synthesis and Implementation.

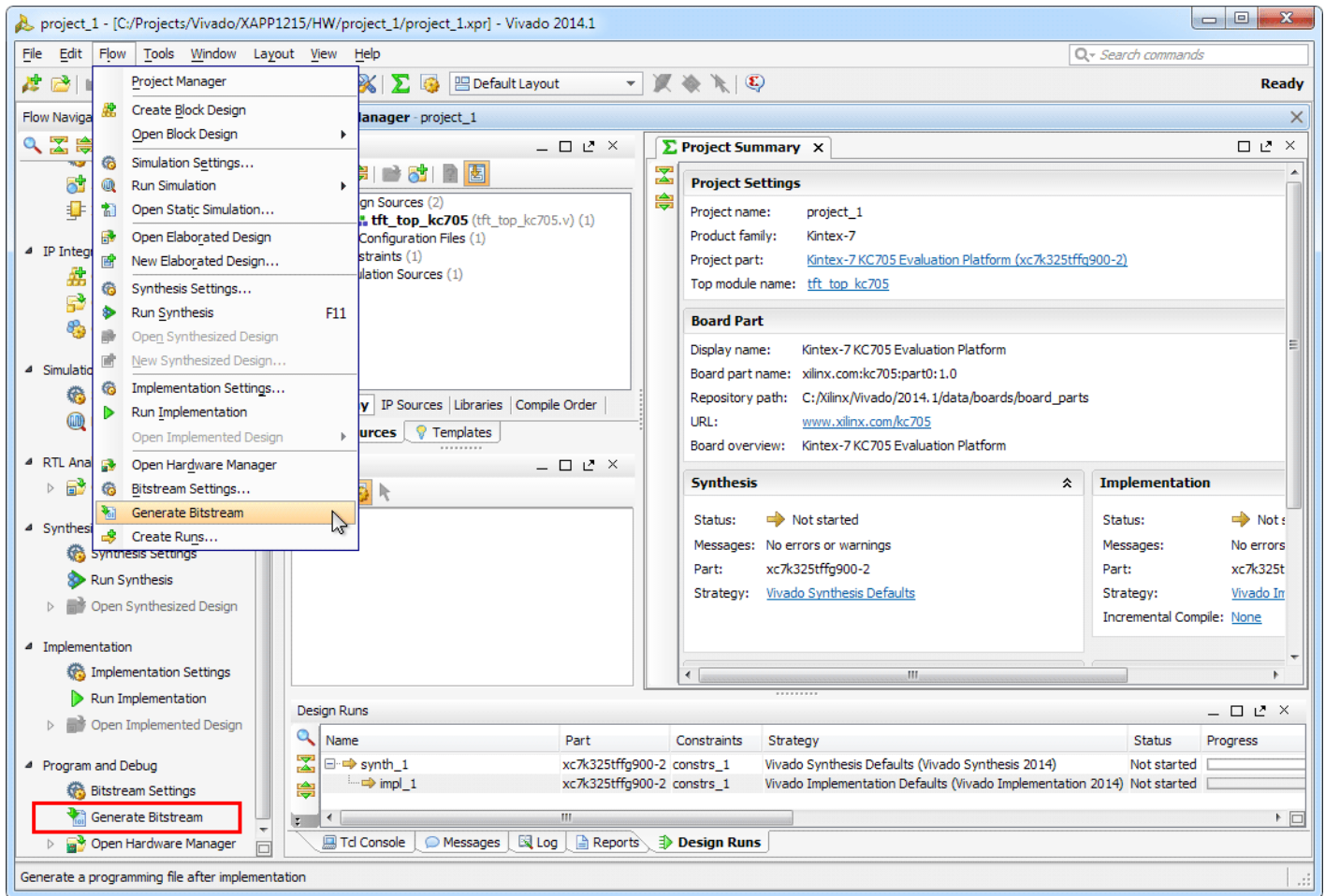


Figure 4: Generate Bitstream

- When complete, select **View Reports** and click **OK** (Figure 5).

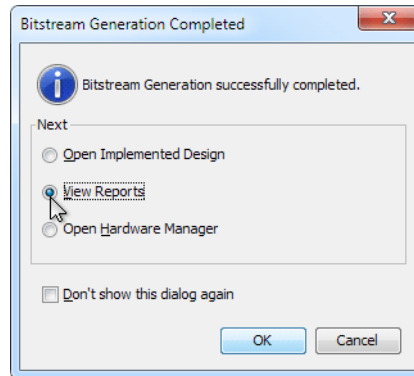


Figure 5: Bitstream Generation Completed

The generated bitstream is stored at this location:

```
<unzip dir>/XAPP1215/HW/project_1/project_1.runs/impl_1/tft_top_kc705.bit
```

Note: Synthesis and Implementation for this design can take from thirty minutes to more than one hour to complete depending upon system speed and available resources.

Compiling the Software Application in SDK

- Launch SDK.

Windows:

Double-click the Xilinx SDK 2014.1 shortcut icon on the desktop or select **Start > Xilinx Design Tools > SDK 2014.1 > Xilinx SDK 2014.1**.

Linux:

```
% xsdk
```

- In the Workspace Launcher, select the following workspace path and click **OK** (Figure 6):

```
<unzip dir>/XAPP1215/HW/project_1/project_1.sdk/SDK/SDK_Export/
```

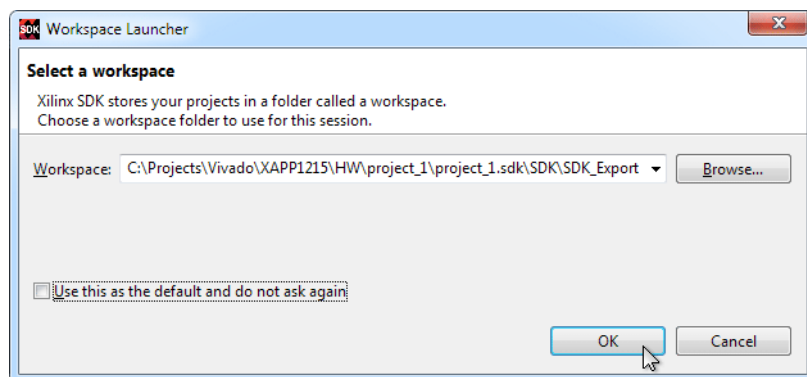


Figure 6: SDK Select Workspace

- If the SDK projects are visible in the workspace, select **Project > Build All**.
- If the SDK projects are *not* visible in the workspace, import the SDK project by following these steps:
 - Select **File > Import**.
 - Select **General > Existing Projects into Workspace** (Figure 7).

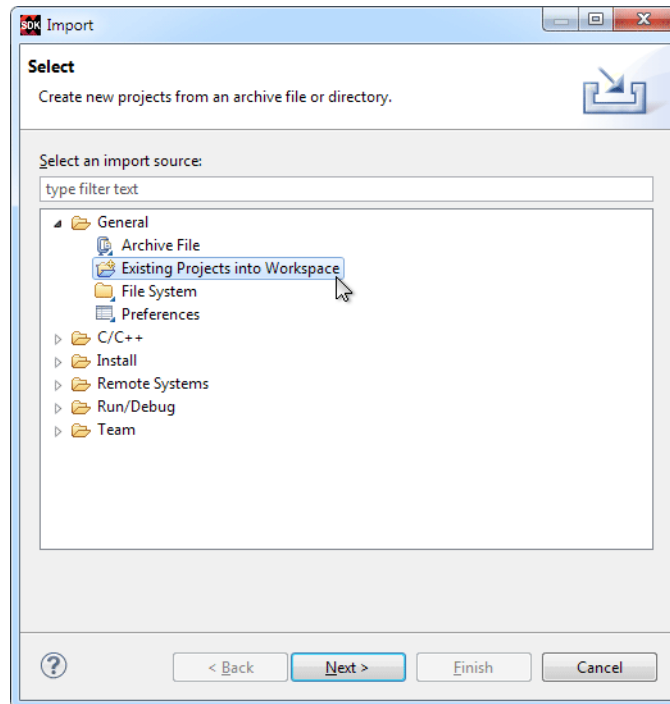


Figure 7: Import Existing Projects into Workspace

- c. Click **Next**.
- d. Change Root Directory to:
`<unzip dir>/XAPP1215/HW/project_1/project_1.sdk/SDK/SDK_Export/`
- e. Click **Finish**.

The board support package (BSP) and software applications are compiled at this step. The process takes from two to five minutes. Upon completion, existing applications can be modified and new applications can be created using the SDK.

Note: The following steps are only required if the goal is to rebuild the hardware as described in [Building Hardware](#).

5. Right-click `hw_platform_0` and select **Change Hardware Platform Specification** ([Figure 8](#)).

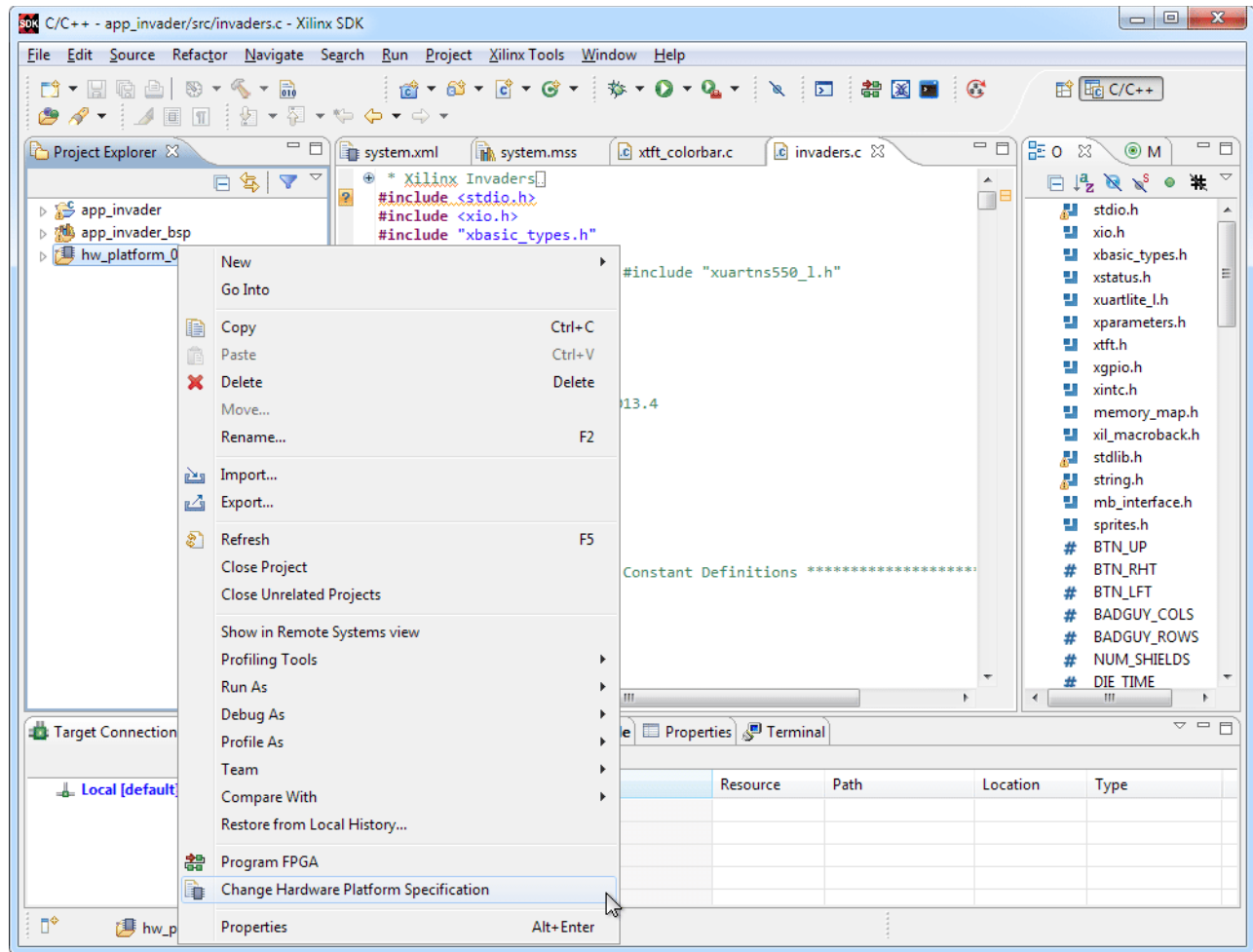


Figure 8: Change Hardware Platform Specification

6. Click **Yes**.
7. Select the `design_1.xml` file at this location and click **Open** (Figure 9):

```
<unzip dir>/XAPP1215/HW/project_1/project_1.sdk/SDK/SDK_Export/hw/design_1.xml
```

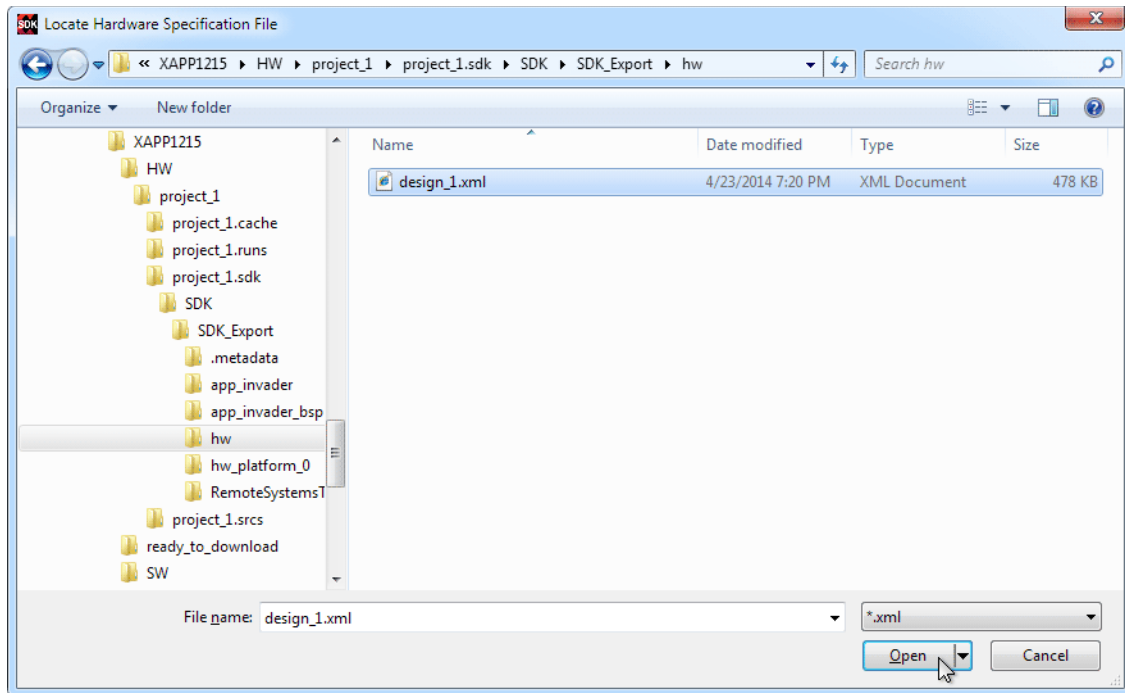



Figure 9: Locate Hardware Specification File

8. Click **OK**.
9. Select **Project > Build All**.

The BSP and software applications are again compiled at this step. The process takes from two to five minutes.

Executing the Reference Design in Hardware

Setting up the KC705 Example

This section provides instructions to run the AXI TFT Controller reference design on the Kintex-7 FPGA KC705 Evaluation Kit board shown in [Figure 10](#).

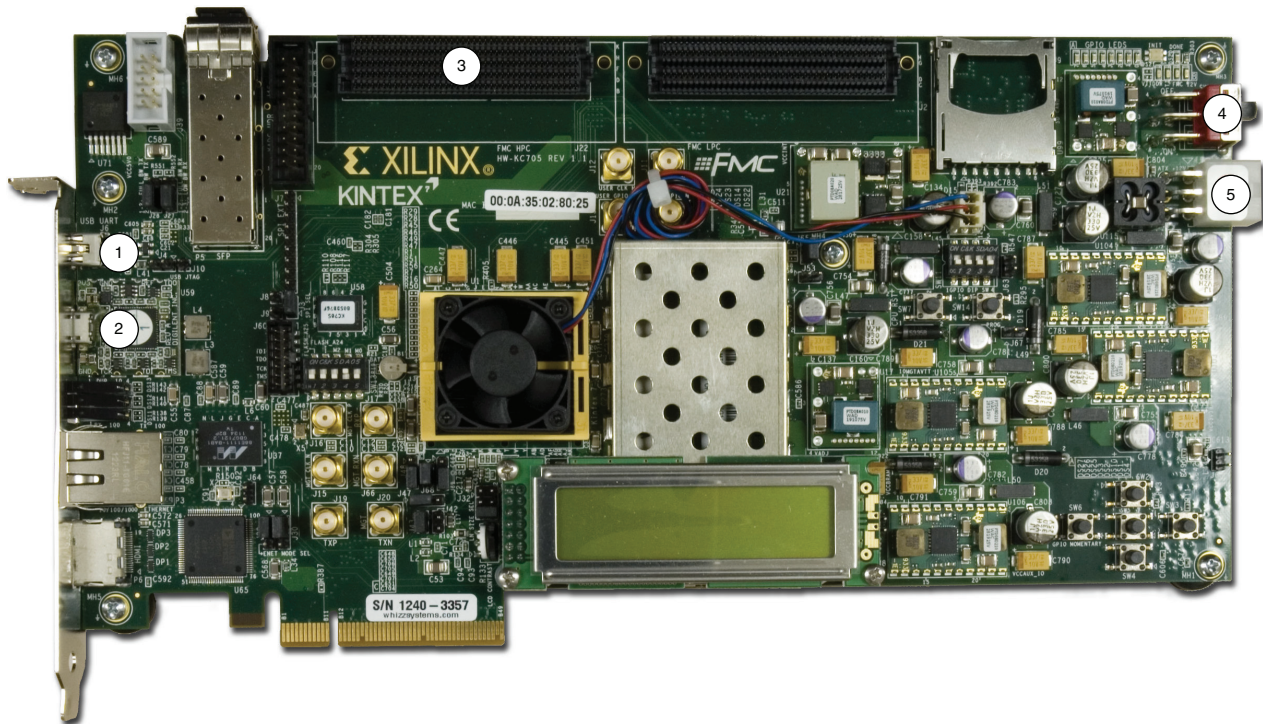


Figure 10: **KC705 Board Features**

In these instructions, numbers in parentheses correspond to callout numbers in [Figure 10](#).

1. Connect a USB Type-A to Micro-B cable from the host PC to the USB JTAG port (2). Ensure that the appropriate device drivers are installed on the host PC. See *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883), [\[Ref 5\]](#)
2. Connect a USB Type-A to Mini-B cable from the host PC to the USB UART port (1). Ensure that the appropriate device drivers are installed on the host PC. See *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883), [\[Ref 5\]](#)
3. Connect the Avnet DVI I/O FMC module to the FMC HPC connector (3).
4. Connect the KC705 Universal 12v power adapter to the power connector (5).
5. Connect the HDMI cable from the TFT monitor to the DVI-D output of the Avnet DVI I/O FMC card.
6. Set the power switch (4) to the ON position.

The completed setup should resemble that shown in [Figure 11](#).

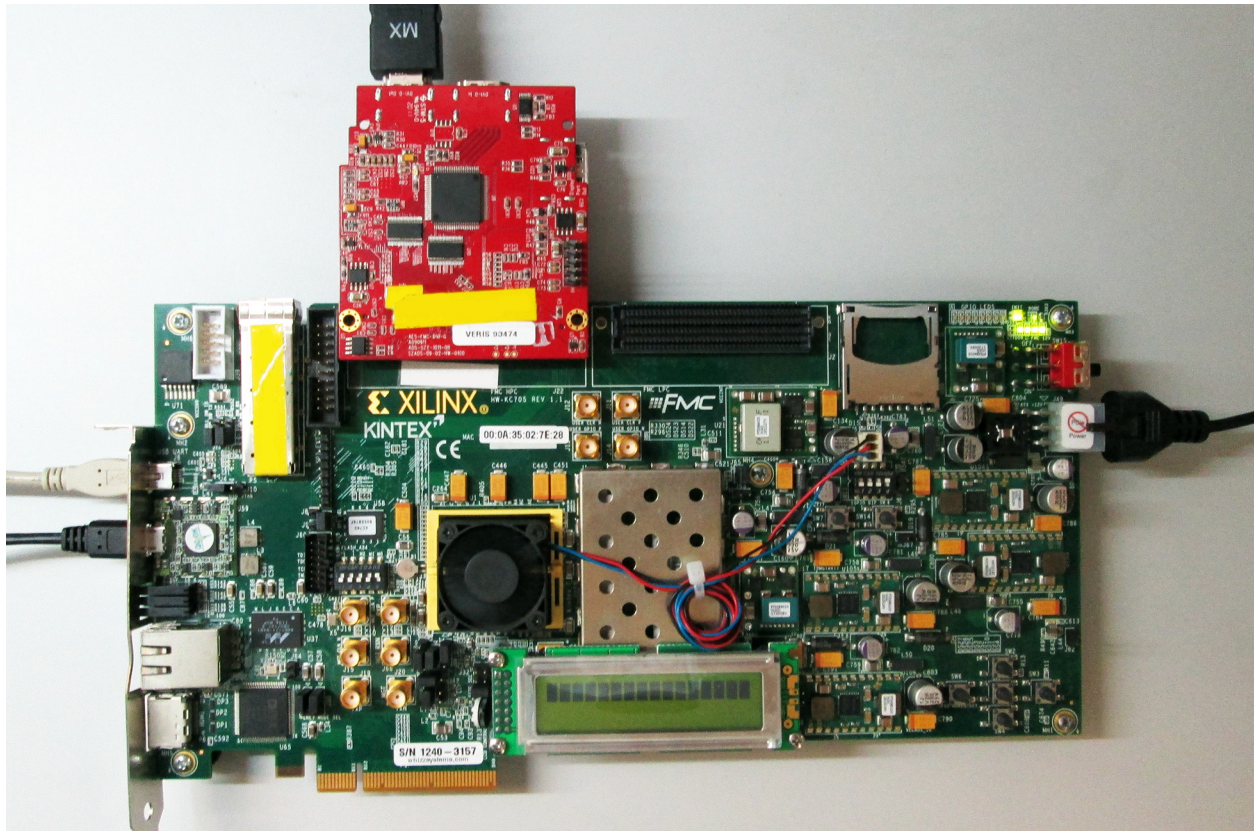


Figure 11: AXI TFT Controller Reference Design Setup

Executing the Reference System

Follow these steps to execute the reference system using the pre-built bitstream in the design files.

1. Start a terminal program on the host PC such as Tera Term or HyperTerminal. Use these settings:
 - Baud Rate: **9600**
 - Data Bits: **8**
 - Parity: **None**
 - Stop Bits: **1**
 - Flow Control: **None**
2. In a command shell or terminal window, change to the `ready_for_download` directory:

```
% cd <unzip dir>/XAPP1215/ready_for_download
```
3. Invoke the Xilinx Microprocessor Debugger (XMD):

```
% xmd
```
4. Download the bitstream:

```
XMD% fpga -f tft_top_kc705.bit
```
5. Connect to the processor:

```
XMD% connect mb mdm
```
6. Download the processor code (ELF) file:

```
XMD% dow app_invader.elf
```

7. Run the application:
`XMD% run`
8. Press GPIO pushbutton SW6 to move the shooter object to the left. Press SW3 to move the shooter object to the right. Press SW5 to fire projectiles (Figure 12).

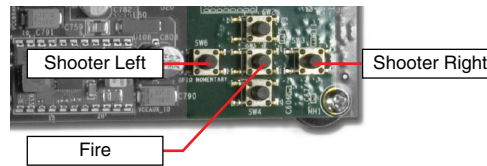


Figure 12: Game Application Controls

Figure 13 shows the terminal output from the game application. Figure 14 shows the content of the TFT display during game play.

```

..... Starting TFT System Initialization .....

Display color
TFT test completed!
Starting Invader App
Initialize TFT
Initialize GPIO
Set background
create sprites
draw sprites
He shot me!
DIE
Cleanup:
Set background
create sprites
draw sprites
    
```

Figure 13: Game Application Terminal Output

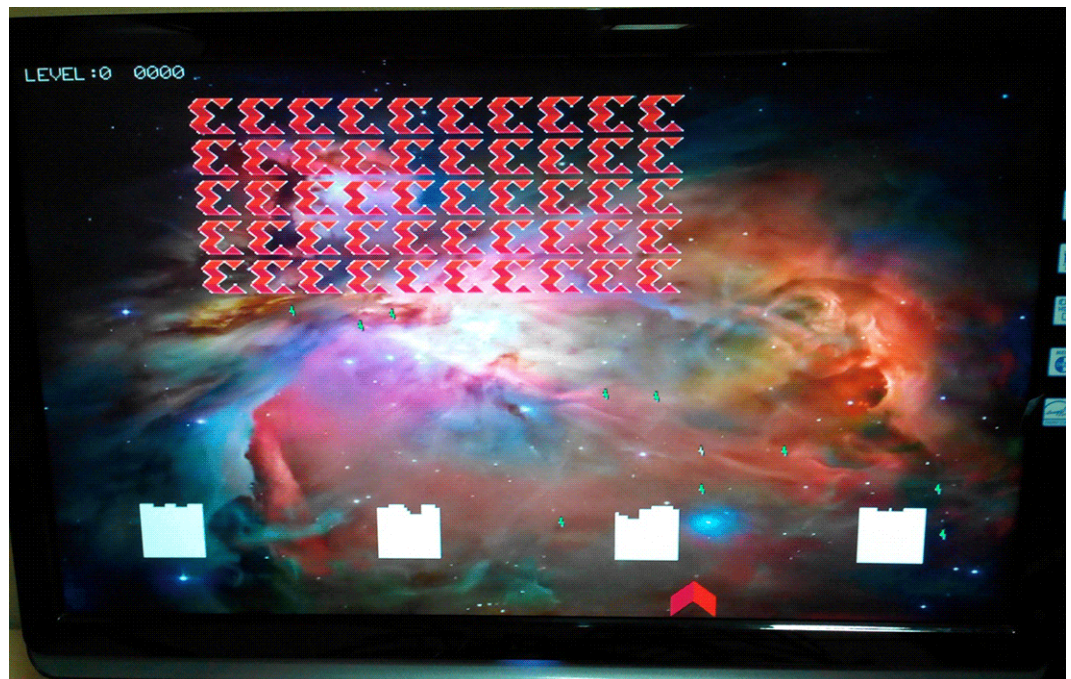


Figure 14: TFT Display Content

Reference Design

The reference design files for this application note can be downloaded from:

<https://secure.xilinx.com/webreg/clickthrough.do?cid=362333>, registration required.

Table 2 shows the reference design checklist.

Table 2: Reference Design Checklist

Parameter	Description
General	
Target devices (stepping level, ES, production, speed grades)	Kintex-7 XC7K325T-2FFG900
Source code provided	Yes
Source code format	VHDL/Verilog
Design uses code/IP from existing Xilinx application note/reference designs, Vivado IP Catalog, or third party	N/A
Simulation	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/version used	Vivado Design Suite 2014.1
Implementation software tools/versions used	Vivado Design Suite 2014.1
Static timing analysis performed	Yes (timing passed with Vivado design suite implementation)
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	Kintex-7 FPGA KC705 evaluation kit

Design Characteristics

The reference design is implemented using Vivado Design Suite 2014.1 and a Kintex-7 FPGA (XC7K325T-2FFG900) target device.

Utilization and Performance

Table 3 shows the utilization and performance figures for the reference design on the KC705 evaluation board.

Table 3: Utilization and Performance

Component	Value
Slice Logic	
Slice LUTs	18,500
Slice Registers	16,525
IOBs	
I/O	144
Memory	
RAMB36E1	45
RAMB18E1	6
Clocking	
BUFGCTRL	5
MMCME2_ADV	1
PLLE2_ADV	1
General	
Run Time	64 minutes CPU time
Timing Violations	None

Table 4 shows the utilization figures at the module level for the reference design on the KC705 evaluation board.

Table 4: Module Level Utilization

Instance	Total LUTs	FFs	RAMB36	RAMB18
Top	18,500	16,525	45	6
microblaze_1	1,752	1,575	10	0
mig_1	13,128	10,768	0	0
axi_tft_0	706	1,091	0	1
axi_intc_1	171	172	0	0
axi_interconnect_lite	164	120	0	0
axi_interconnect_full	1,929	2,147	3	5
concat_0	0	0	0	0
axi_gpio_0	30	59	0	0
axi_iic_0	428	365	0	0
lmb_v10_1	8	4	32	0
mdm_1	82	105	0	0
proc_sys_reset_1	19	31	0	0

Notes:

1. The utilization information is approximate due to the cross-boundary logic optimizations and logic sharing between modules.

Conclusion

The Kintex-7 FPGA KC705 Evaluation Kit provides an excellent platform to implement and test the AXI TFT Controller core. Various configurations can be quickly evaluated and custom software applications can be developed using the KC705 board, the Vivado Design Suite and SDK.

References

These documents provide supplemental information useful with this application note:

1. AMBA AXI4 [specifications](#)
2. *Vivado Design Suite Tutorial: Designing IP Subsystems Using IP Integrator* ([UG995](#))
3. *LogiCORE IP AXI Interconnect Product Guide* ([PG059](#))
4. *LogiCORE IP AXI Thin Film Transistor Controller Product Guide* ([PG095](#))
5. *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* ([UG883](#))
6. *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* ([UG810](#))
7. *Vivado Design Suite: AXI Reference Guide* ([UG1037](#))
8. *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* ([UG994](#))

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
07/18/2014	1.0	Initial Xilinx release.

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