Accelerated Algorithmic Trading

INTRODUCTION

The Xilinx Accelerated Algorithmic Trading (AAT) system is a fully featured opensource, license-free HLS hardware and software reference design for trading applications. Give your development team a head start to create their own hardware-accelerated algorithmic trading platform.

SOLUTION OVERVIEW

Trading strategies running on CPUs incur additional latency, particularly from traversing the PCIe bus. FPGA based trading strategies can significantly lower latency, but typically need large teams of experts and long design cycles.

Xilinx AAT reference design (Fig 1) provides all the infrastructure required to create a trading application on the FPGA using Xilinx Vitis™ unified platform, and standard Xilinx shells. The design is written in HLS, and all the source code is provided. The design is modular, allowing you to easily replace IP blocks in the reference design with your IP. Xilinx AAT reduces the time to take your solution to market and enables building FPGA based trading solutions at minimal cost.

Features and Benefits

- Full implementation in HLS
- Designed for Software Engineers
- Source code provided
- Integrated with Vitis™
- Runs out of the box on Xilinx Alveo™
- Supported on Alveo™ U250 , U50
- Supports XDMA and host memory bridge based shells
- TCP, UDP, ethernet IPs provided
- Orderbook module managed by CME MBP scheme provided
- Feed handler module for FIX format

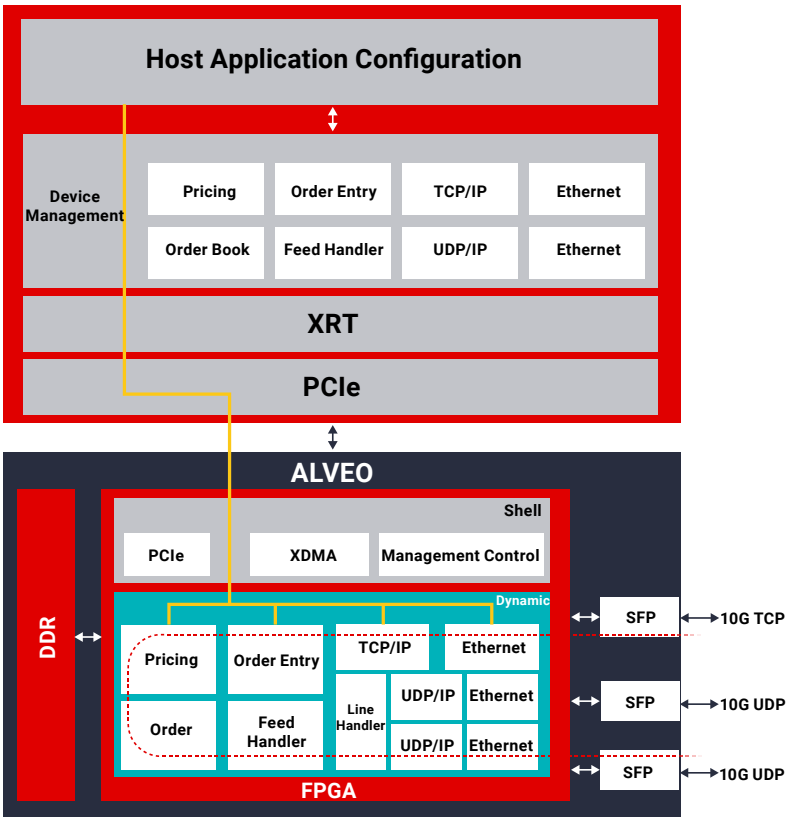

Figure 1: Xilinx infrastructure for low-latency trading

SOLUTION DETAILS

The AAT reference design uses standard Vitis ™ shells for data transfer between host applications and kernels in the FPGA (Fig 2), as well as for card management. IP blocks are connected using AXI4-stream interfaces and can easily be replaced by 3rd party IP.

AAT provides upto three 10GbE ports, UDP IP blocks, as well as a line handler module for line arbitration. A feedhandler module, an orderbook module and a pricing module are provided as examples .

The reference design provides the ability to implement the pricing module on the host CPU. The order entry module and TCP IP modules can be used to execute orders with minimal latency. AAT provides drivers for each IP in the design, along with an application layer and a command line interface to interact with the solution.

The latest release of the AAT reference design provides the ability to run cycle accurate simulations using PCAP files as inputs. Hardware emulation (Fig. 3) makes debugging your designs easier by providing visibility into the path of a packet through each block in the design This feature reduces design time significantly and allows you to build and take high quality solutions to market sooner.

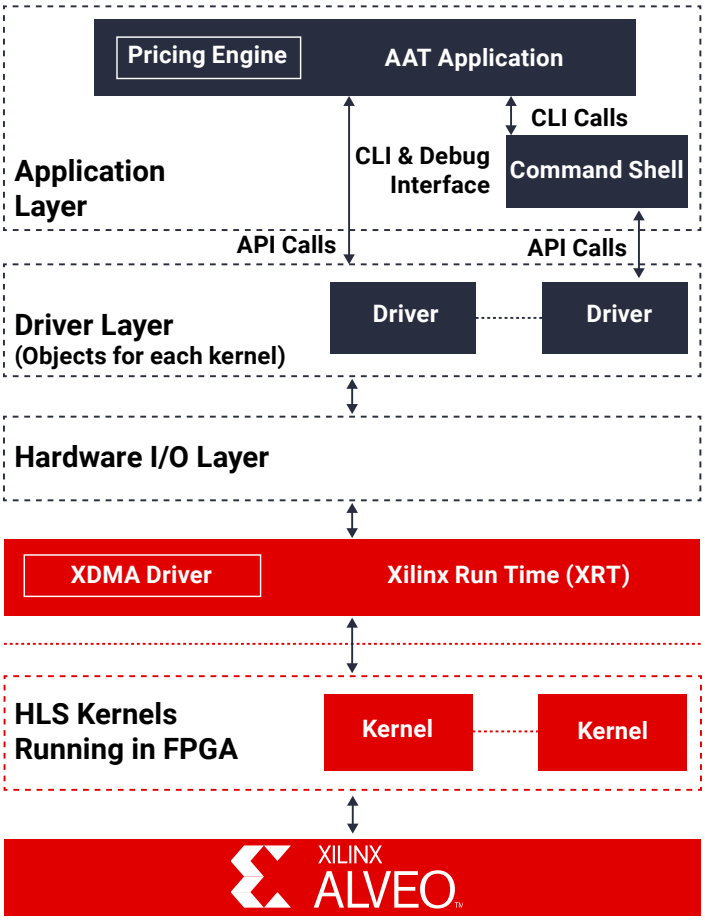

Figure 2: Xilinx AAT Software Stack

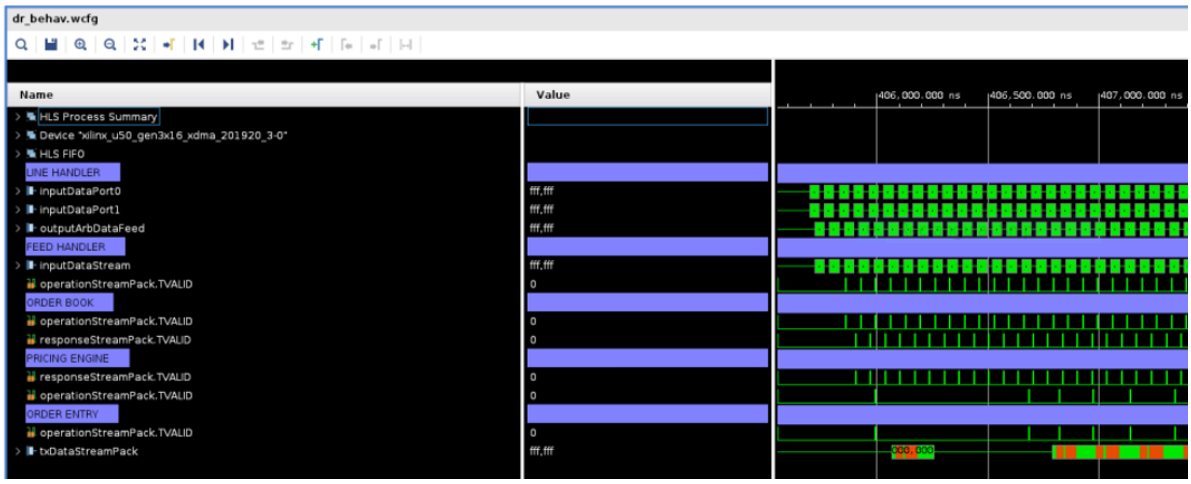

Figure 3: Hardware Emulation

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