SOLUTION BRIEF

Xilinx T2 Telco Accelerator Card

OVERVIEW

Xilinx T2 Telco Accelerator card provides high performance, low latency, and power efficiency needed for 5G O-DU deployments. The turnkey solution enables operators, system integrators, and OEMs to get to market quickly and to simplify the deployment of services at the edge. It has a strong channel coding scheme of Low Density Parity Check (LDPC) code for reliable data transmission over 5G radio interface and it also supports turbo coding Forward Error Correction (FEC) mechanism for data transmission over 4G interface.

T2 card uses 16nm Zynq UltraScale+ RFSoC device to accelerate real-time baseband (L1) lookaside processing. It assumes a separate solution for Front haul termination and focuses the entire PCIe bandwidth on LDPC FEC, HARQ, Rate matching and CRC attach/detach functions.

ZU48DR RFSoC includes 4G/5G encode and decode acceleration along with wrapper functions such as rate matching and CRC logic. Zynq UltraScale+ RFSoC has hardened soft-decision forward error correction (SD-FEC) blocks, which can perform high-performance encode and decode with low cost, latency and power. The T2 card has a PCIe® Gen3 x16/ 2x Gen4x8 connector and can plug into any commercial off the shelf (COTS) server thus improving network scalability, agility and total deployment costs.

The board is a single slot half height, half length (HHHL) form factor. The card is passively cooled and has a maximum electrical power limit of 50W. The high throughput, low latency and low power of T2 card make it an ideal solution for 5G massive MIMO radio configurations.

TARGET APPLICATIONS

> 5G L1 baseband acceleration and LDPC decoding/encoding with SD-FEC integrated block in network base station applications

> 4G L1 baseband acceleration with Turbo coding FEC mechanism

PERFORMANCE

Virtualization requires significant acceleration of latency-sensitive and compute-intensive functions. The T2 card performance metrics below are based on in-lab measurements of the card reference design.

Peak throughput and average latency of each SD-FEC core is given. The ZU48DR device has 8 SD-FEC cores which can be configured as LDPC encoder/decoder or turbo decoder to achieve the desired throughput.

L1 LDPC Performance	Throughput per SD-FEC Core	Average Latency
Encoder	35 Gb/s	< 10usec
Decoder	12 Gb/s	< 10usec

SPECIFICATION

SoCs	Zynq UltraScale+ RFSoC ZU48DR
SoC Resources	> System Logic Cells - 930K > CLB LUT - 425K > SDFEC - 8 > DSP Slices - 4,272 > Total BRAM - 38Mb > Max Distributed RAM - 13Mb > URAM - 22.5mb

SPECIFICATION

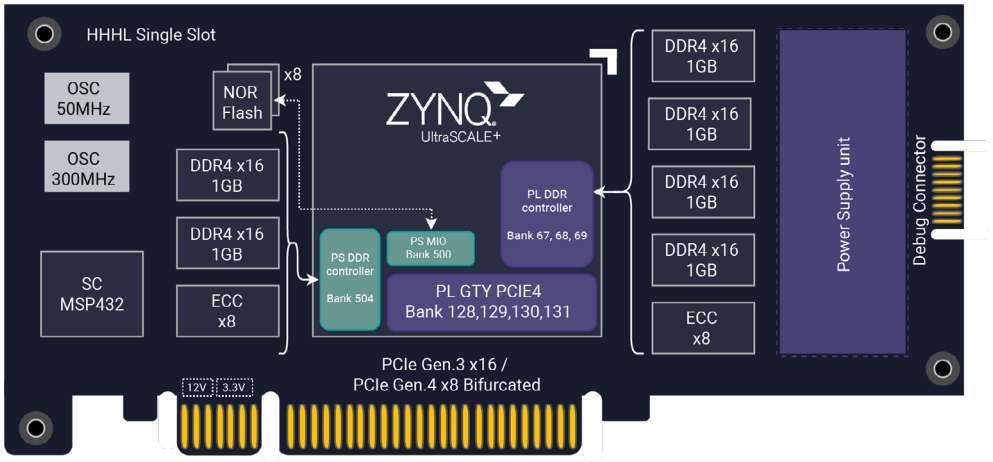
Form Factor	> Half Height Half Lenght (HHHL) > PCB Thickness: 1.59mm > Length: 167.65mm > x16 PCIe Form Factor > Primary Side Width: 14.22mm > Height: 56.14mm > Secondary Side Width: 2.5mm
PCIe Interface	PCIe® Gen3 x16/ 2x Gen4x8
On Board Memory	> 1x Banks of 4GB x72 (64 bit +8bit ECC) - PL > 1x Banks of 2GB x40 (32 bit +8bit ECC) - PS > Total Capacity 4GB in PL
	Total Capacity 2GB in PS
In System Upgrade	Standard Xilinx tandem and partial reconfiguration support for the device
Programming	1x 2Gb QSPI NOR Flash for FPGA configuration for ZU48DR
External Interfaces	Xilinx DMB2 connector for JTAG support (FPGA programming and debug) and access to BMC QSPI for ARM boot code and FPGA images
Reference Design	Vivado® design (diagnostic bit file) and commands for testing all datapath interfaces available for diagnostic bit files for both FPGAs
Cooling	Passive cooling, custom heat sink
Board Management Controller (BMC)	> Power Sequencing and Reset > Temperature Monitoring > Field Upgrades > USB 2.0 > FPGA Configuration and Control
Power	55W typical

Xilinx RFSoC details here: www.xilinx.com/support/documentation/selection-guides/zynq-usp-rfsoc-product-selection-guide.pdf

HIGH LEVEL BLOCK DIAGRAM

L1 Offload

- LDPC/TURBO codecs
- Polar codecs
- HARQ management
- Codec Surrounding/Wrapper logic
  - CRC logic
  - Rate Matching/De-Matching



Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Xilinx Europe

Xilinx Europe
Bianconi Avenue
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

India

Xilinx India Technology Services Pvt. Ltd.
Block A, B, C, 8th & 13th floors,
Meenakshi Tech Park, Survey No. 39
Gachibowli(V), Seri Lingampally (M),
Hyderabad -500 084
Tel: +91-40-6721-4747
www.xilinx.com

AMD XILINX

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