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Introducing Vivado® ML Editions

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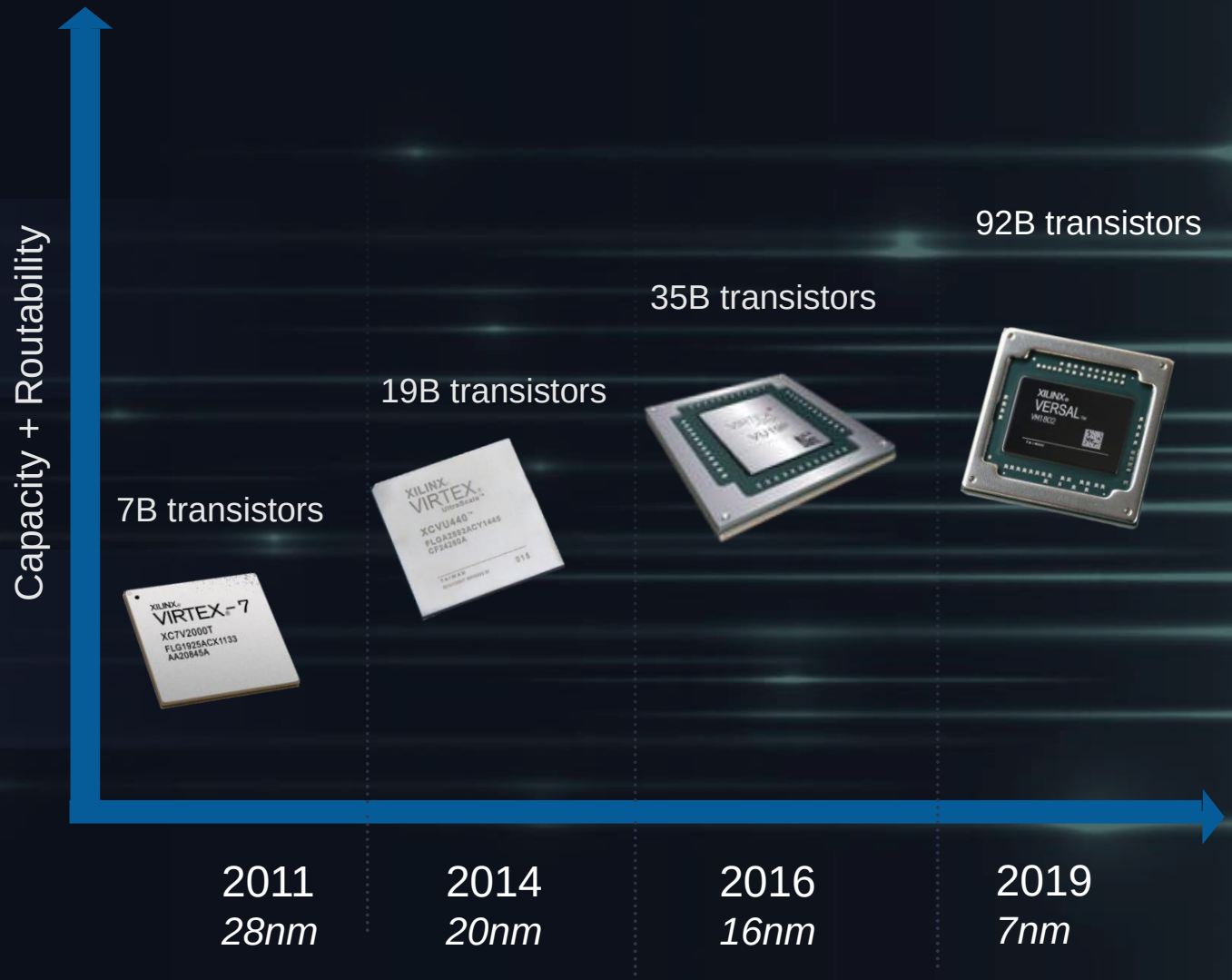
EDA Challenges Today

1. Lack of QoR Breakthrough
   Typically in 1-3% gain range

2. Design Sizes - 38% CAGR
   Compile and iteration time rising



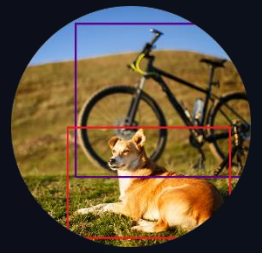
Machine Learning is All About Data

EDA = decades of data + massive design reuse

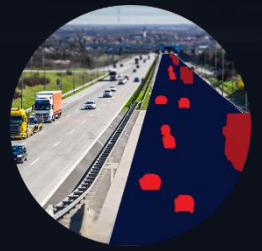
APPLICATIONS

Classification

Object Detection

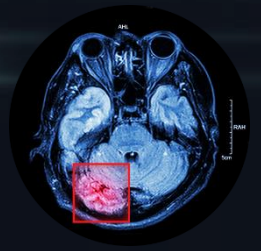


Segmentation



Speech Recognition

Anomaly Detection



Now… EDA

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1 Machine Learning: Next Big Leap for QoR

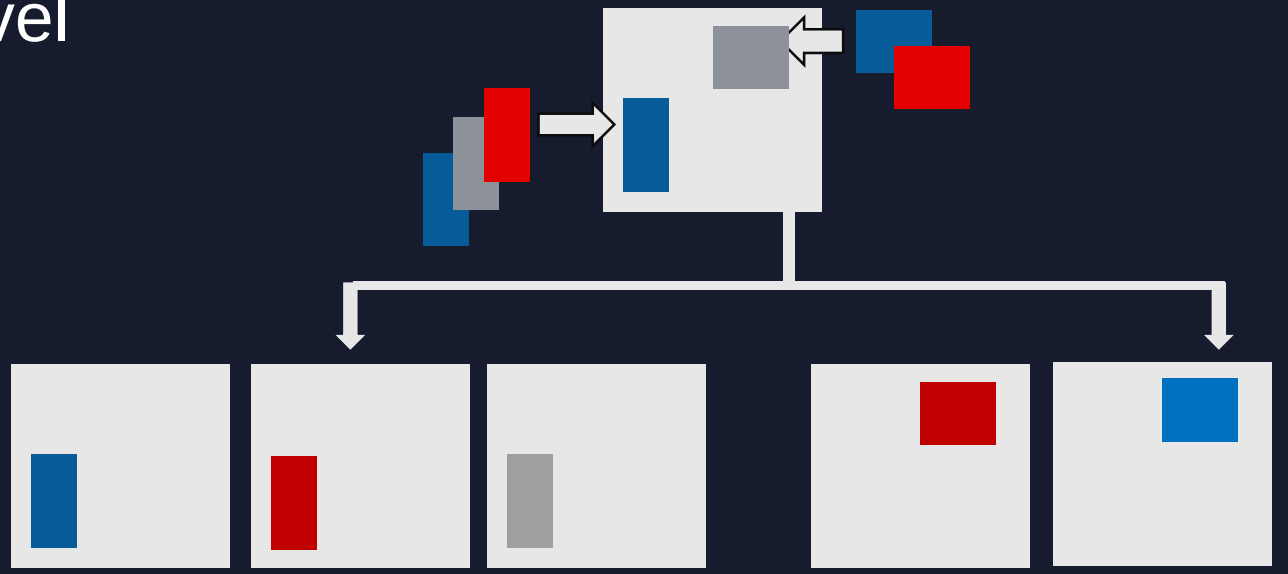
- Tipping point: EDA engineers “know-how” heuristics to data-driven ML models
- Breakthrough in QoR gain: 1% → 10%+
- Faster design iteration for a QoR target

EDA Task	ML
AIG/MIG optimizer selection	DNN
Classify optimal flow	CNN
Generate optimal flow	GCN, RL
Placement decisions	GCN, RL
Evaluate potential paths	SVM, NN
Routing congestion	CNN, GAN, ML, MARS
Predict wirelength	LDA, KNN

Table Source: Guyue Huang, et al. 2021. Machine Learning for Electronic Design Automation: A Survey. arXiv:2102.03357
Photo credit: Rohit Sharma, Machine Intelligence in Design Automation
CNN = Convolutional Neural Network, RL = Reinforcement Learning, KNN = K-Nearest-Neighbor, GAN = Generative Adversarial Network, SVM = Support Vector Machine, GCN = Graph Convolutional Networks, DNN = Deep Neural Network, MARS = Multivariate Adaptive Regression Splines, LDA = Linear Discriminant Analysis

2 Breaking Ever-Growing Design into Modules

- Modular designing for system-level reuse
- Hierarchical compile of reconfigurable modules
- Only load the modules you need in milliseconds while system is online



Introducing

ML-based Design Optimization

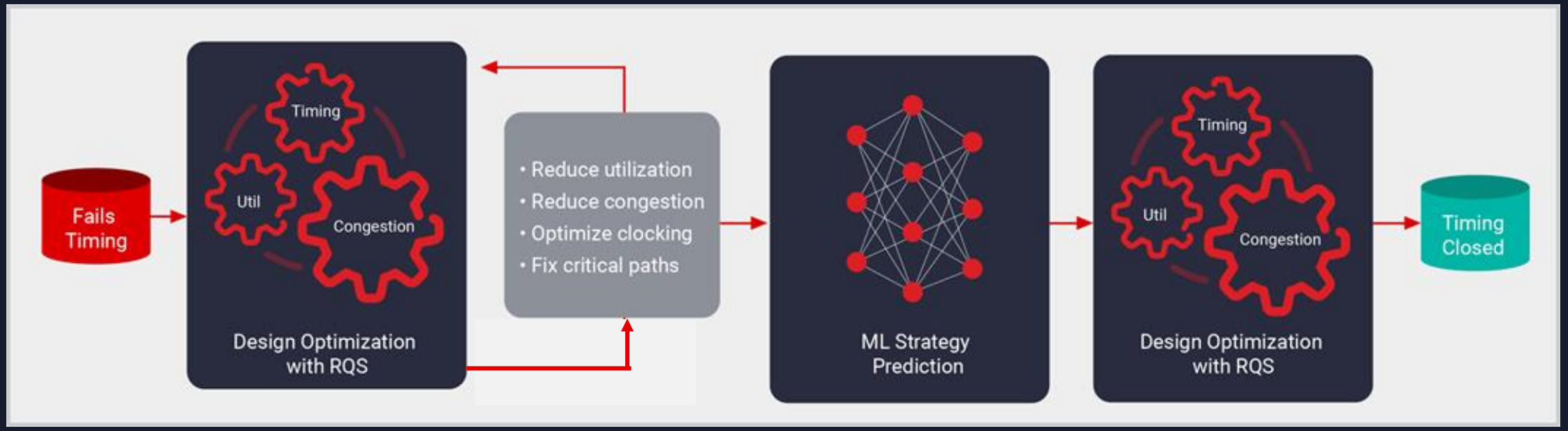
10% average QoR gain

Hierarchical compile of reconfigurable modules

5x average compile time reduction

Example: ML-Based Automatic Timing Closure

Intelligent Design Runs (IDR)



ML-based congestion estimation

Predicts router behavior and avoids creating congestion

ML-based delay estimation

Better delay predictions for complex routing

ML-based strategy prediction

Pick top strategies from 60+ custom strategies based on 100,000+ set of training data

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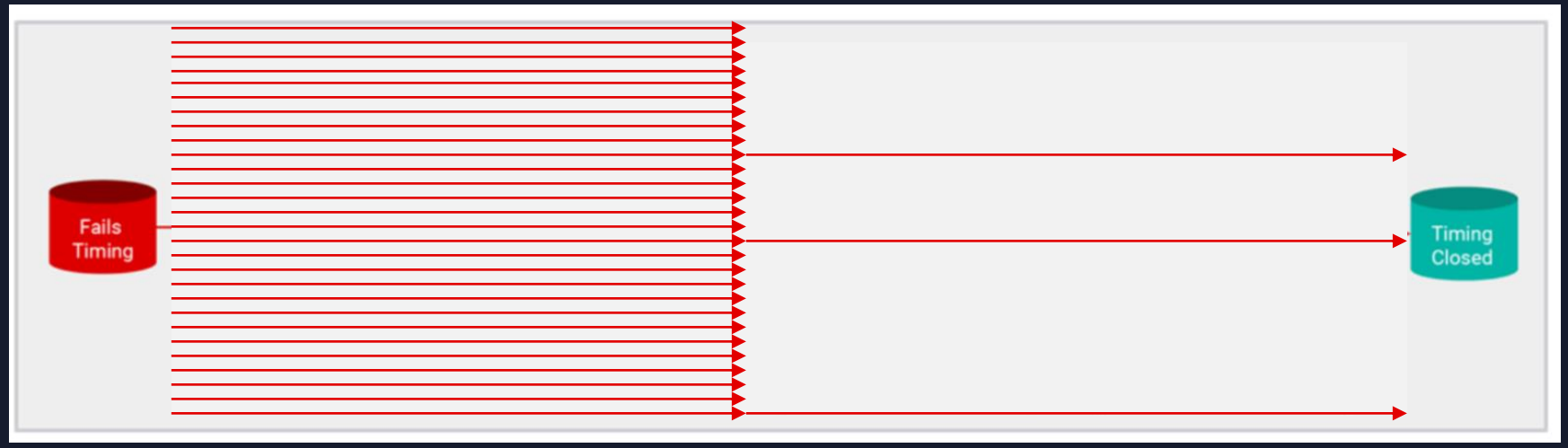
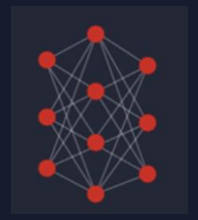
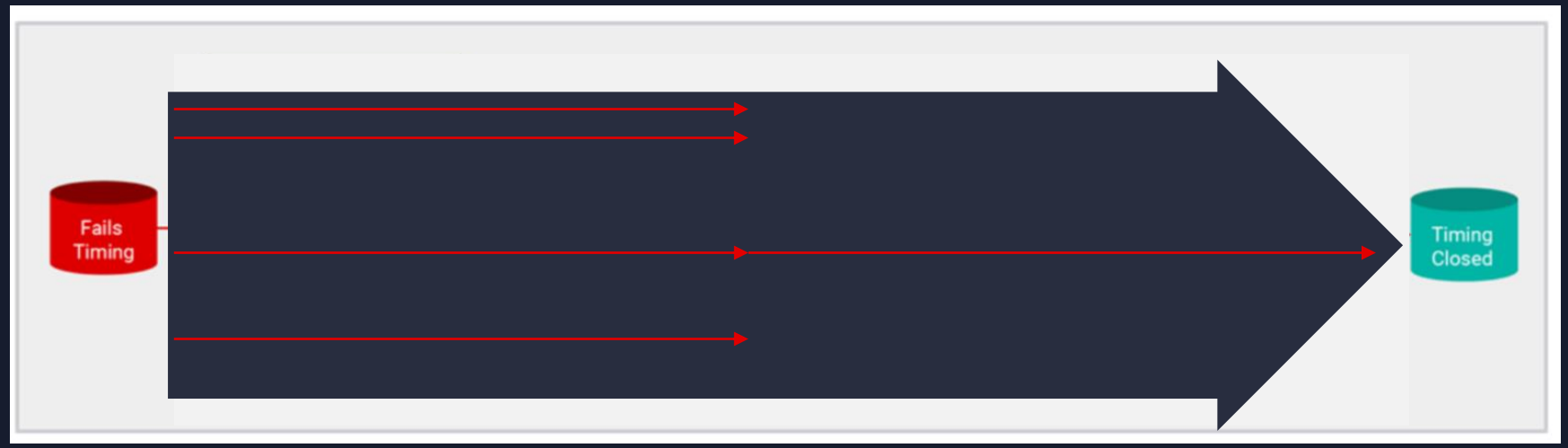
Design Iteration 5x Reduction on Difficult Designs

Without IDR
Typical iteration: 25





With IDR
User iteration: 1



Save Time and Compute Resources

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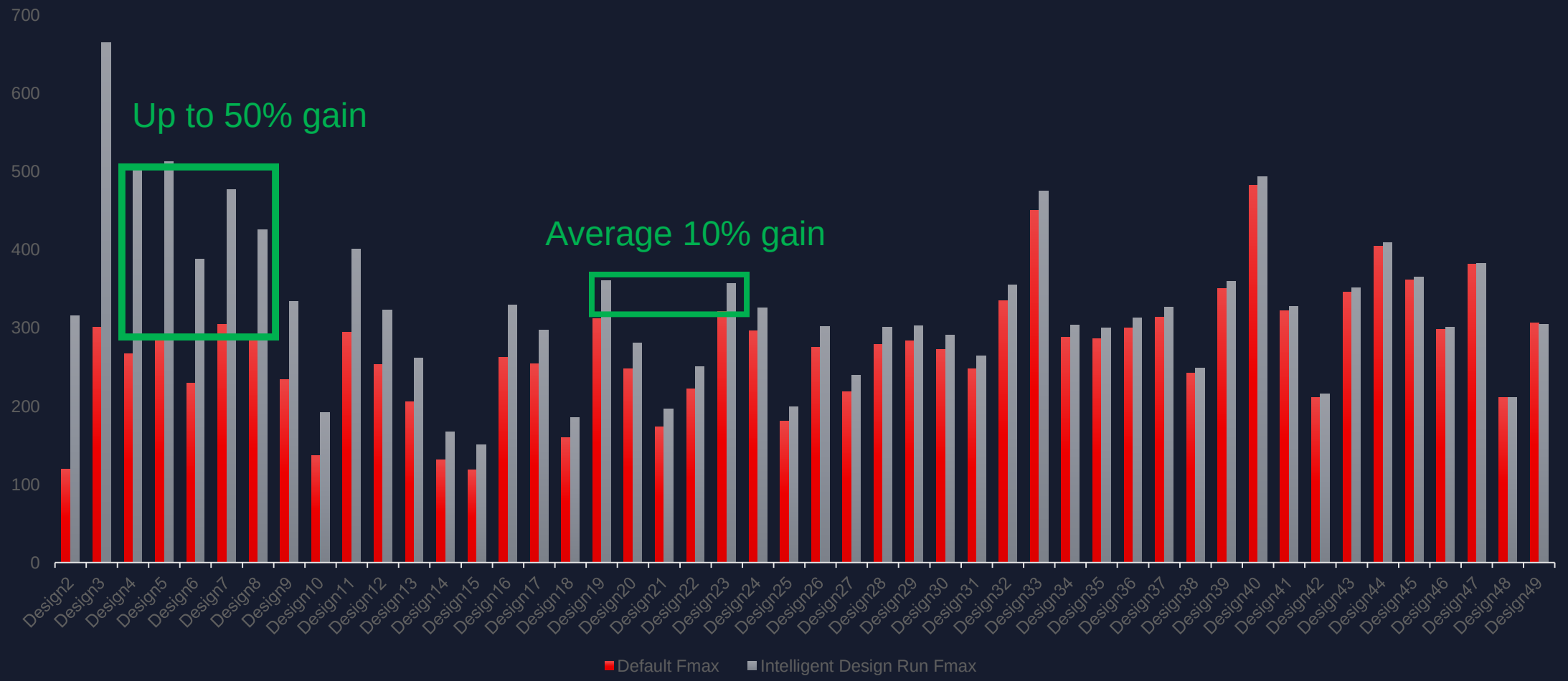
Average 10%, Up to 50% QoR improvement



Major breakthrough QoR gain for higher performance

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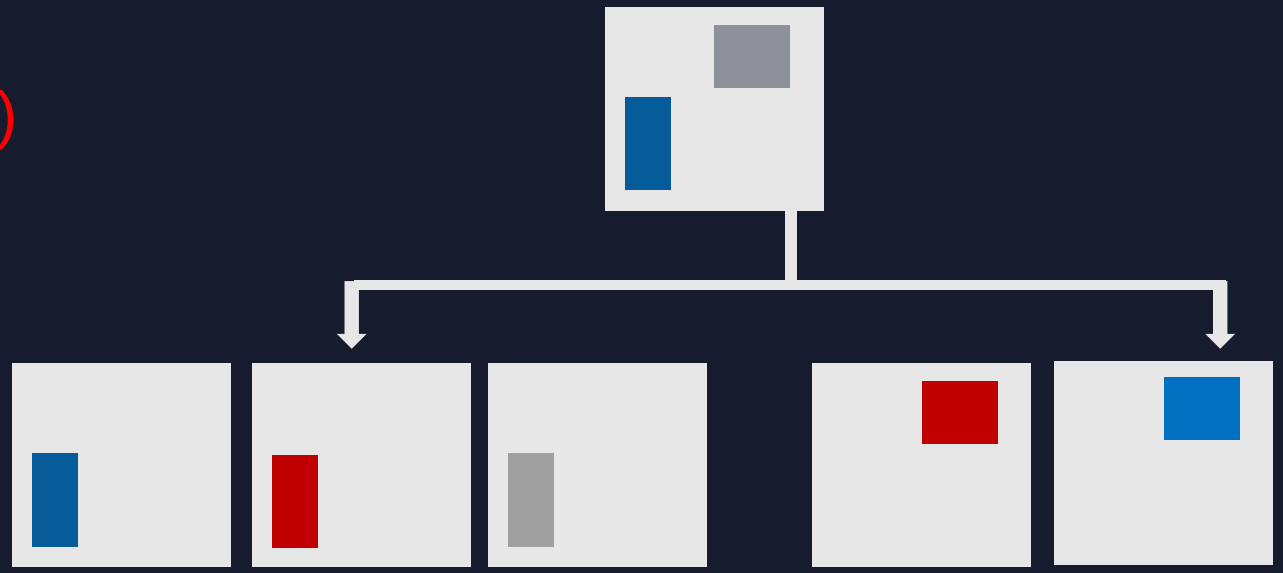
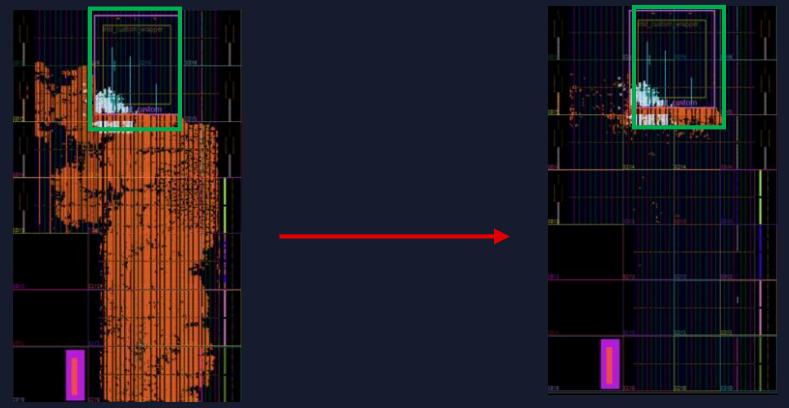
2 Hierarchical Module-Based Compilation

Define Reconfigurable Modules (RM)
Only compile and close timing what's in the RM

Hierarchical Compilation
Linear speedup with parallel tasks

Secure Handoff
Does not contain rest of design, only workspace





Most of the design is trimmed away

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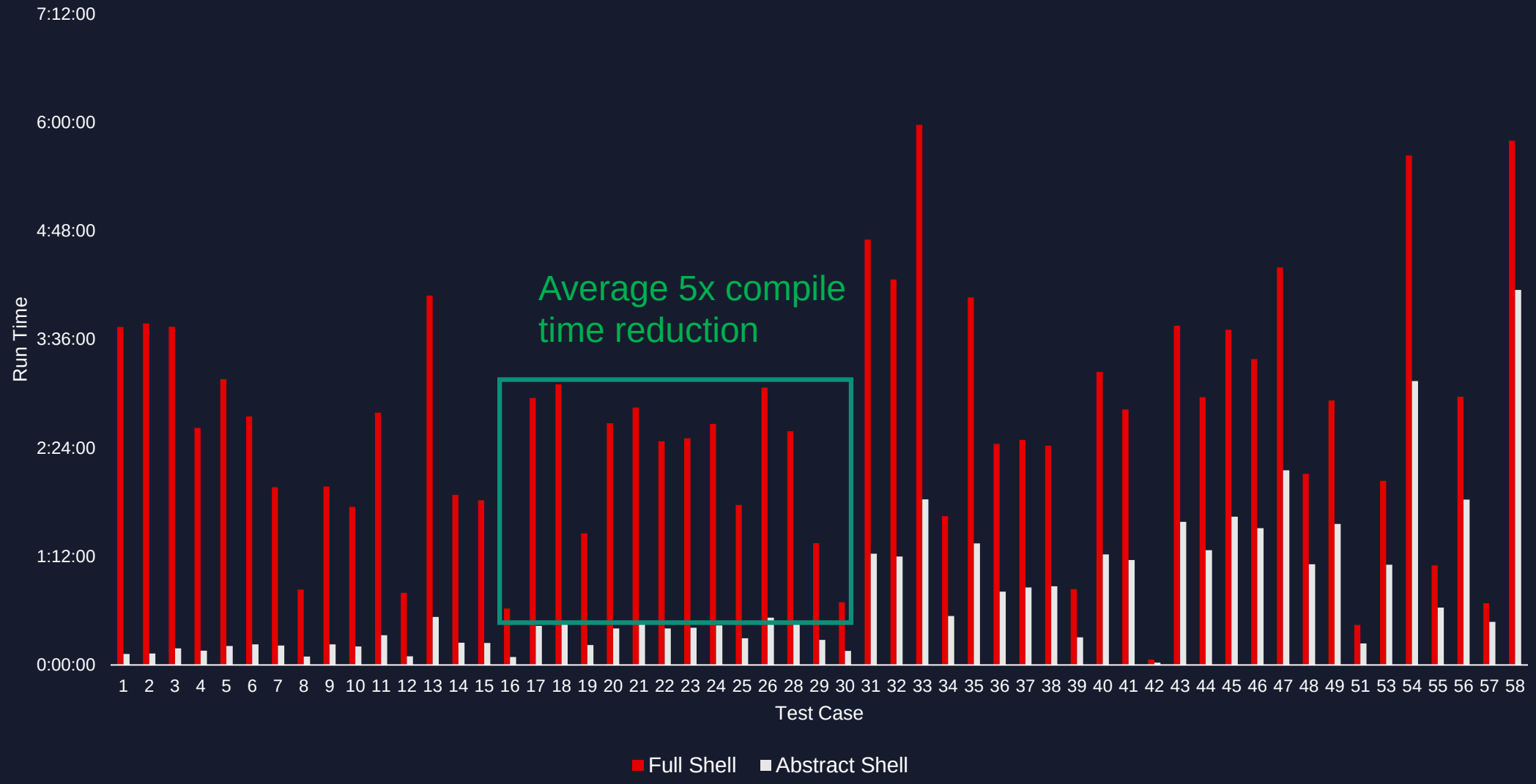
2 Compile Time Reduction with Abstract Shell



Lower better

5x more design runs every day

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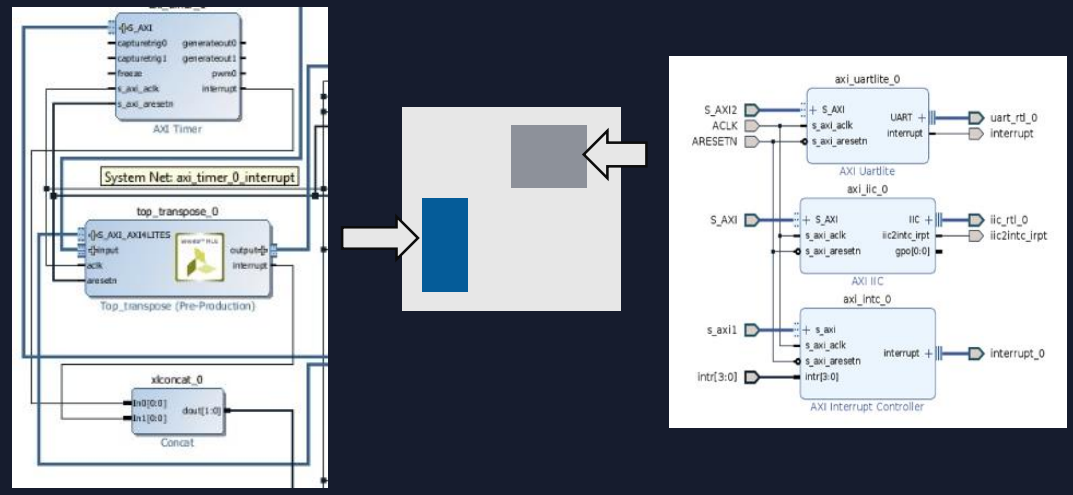
2 Extending Module Design into End-to-End Flow

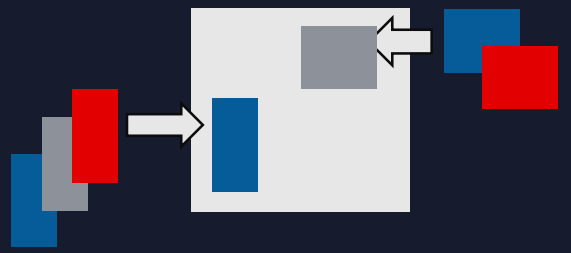
Block Design Containers

Team-based Graphical IP Design Flow with modules



Dynamic Function eXchange

Swap different hardware design in milliseconds while system is online



Team-based productivity boost

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Customer Success Stories

Intelligent Design Runs

'Intelligent Design Runs is a game-changer by offering a push-button method for aggressively improving timing results. IDR generates QoR suggestions that bring maximum impact, resulting in expert quality results and a reduction in user analysis, especially for tough to close designs.'

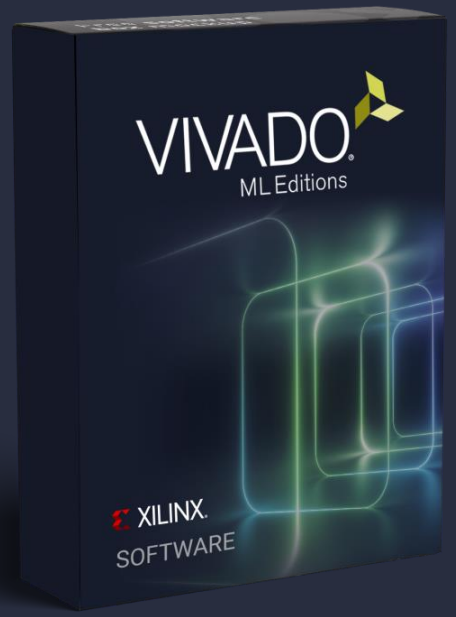
Block Design Containers

'Block Design Containers allowed us to reuse portions of our IPI design much more efficiently than previous versions of Vivado. This led to faster design times and less chance for manual design entry mistakes.'

Abstract Shell

'Using DFX and Abstract Shell has enabled us to keep our IP protected and at the same time allows our customers to create their own dynamic IP. DFX is especially valuable for mission-critical operations by permitting function swapping while the device remains operational.'

Vivado ML Editions

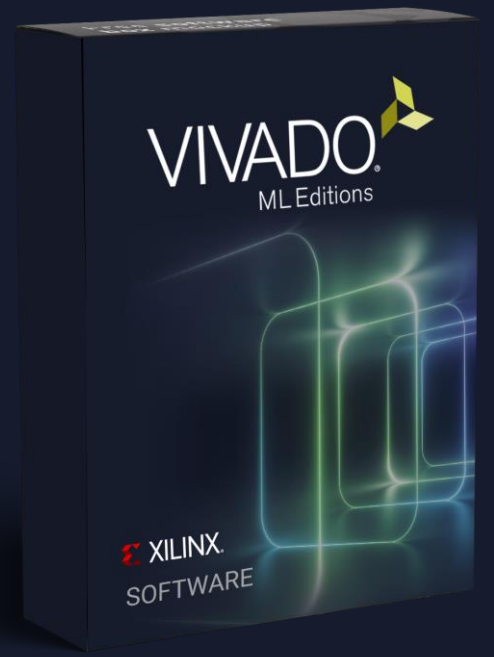


AVAILABLE NOW

Standard Edition

Free

Limited device support



AVAILABLE NOW

Enterprise Edition

NL: $2,995

FL: $3,595

Supports all Xilinx Devices

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Vivado ML: State-of-The-Art EDA with ML algorithms

1. ML-based design optimization
   10% average QoR gain

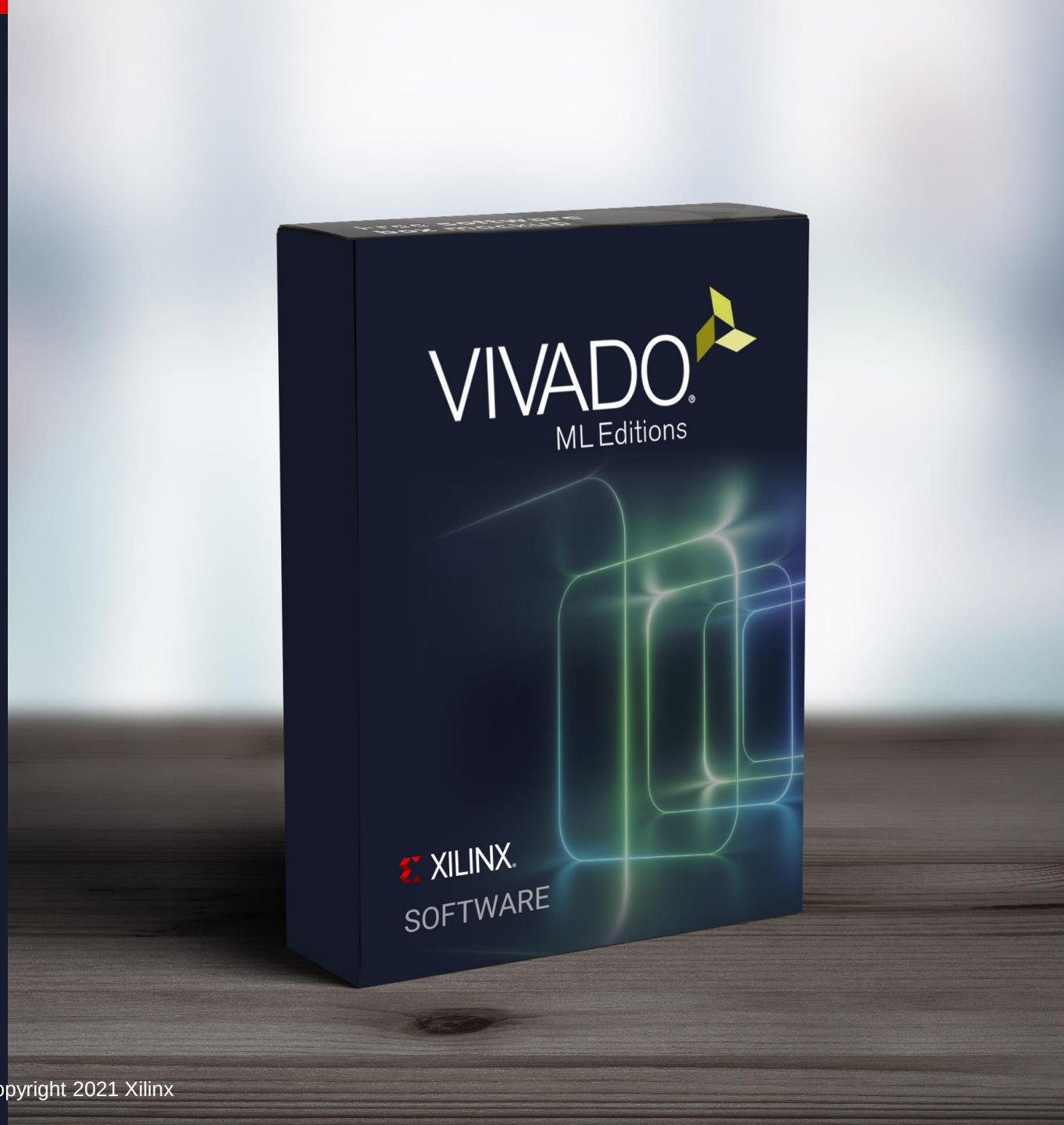
2. Hierarchical compile of reconfigurable modules
   5X average compile time reduction

Design Smarter

https://www.xilinx.com/products/design-tools/vivado.html

Link to video

Whitepapers



Thank You