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Accelerating Hardware Development

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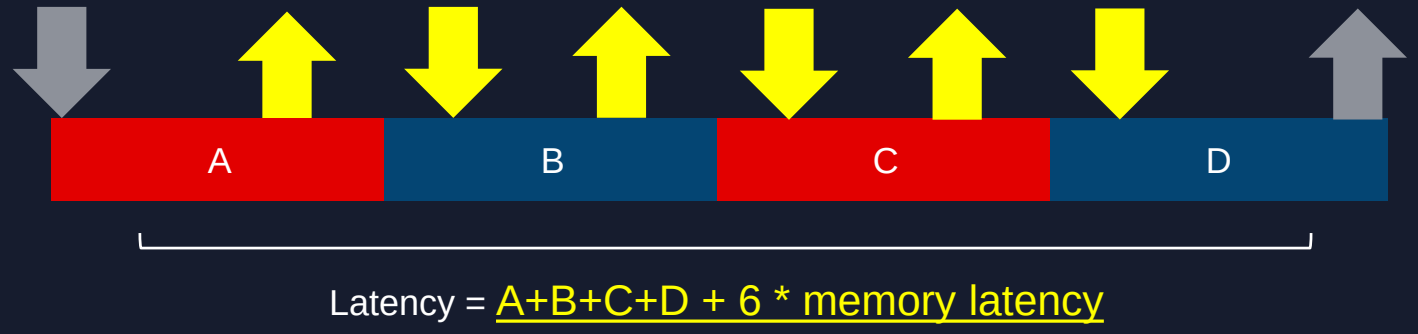
VP Software & AI

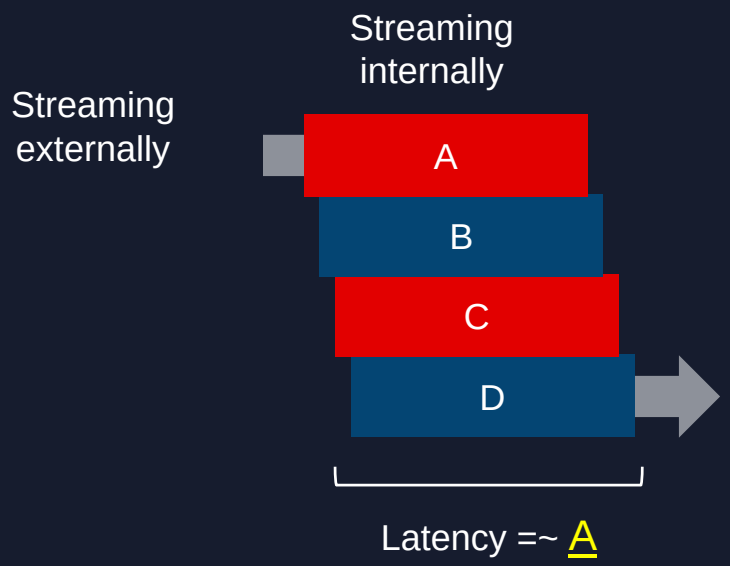
Xilinx Adapt – Vivado
2020

Why Adaptive Computing?

CPU & GPU: Memory Map



FPGA: Streaming



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Development Platforms

Top-Level Strategy

HW Developer

Iterations: O(days)
- 3x-10x in 5y

SW Developer (HW aware)

Iterations: O(hour)
- C++ programming, libraries
- Memory hierarchy abstractions
- Pre-compiled libraries

Data Scientist

Iterations: O(minute)
- Accelerated SW Frameworks (DSL, DSA)

Adaptive Computing Challenges – $250k in Prizes

- **Developer Contest**
  1,070 participants registered on hackster.io
- **70** countries

- **Startup Contest**
  60 Startups registered on xilinx.com

2020 Contest is now closed, watch for the 2021 contest!

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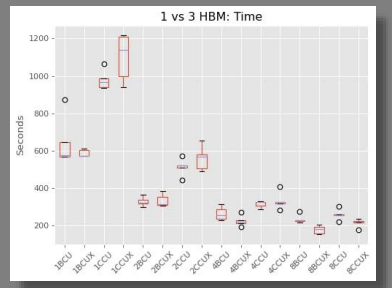
Developer Contest Winners: 9 Teams

Adaptable Compute Acceleration (U50)

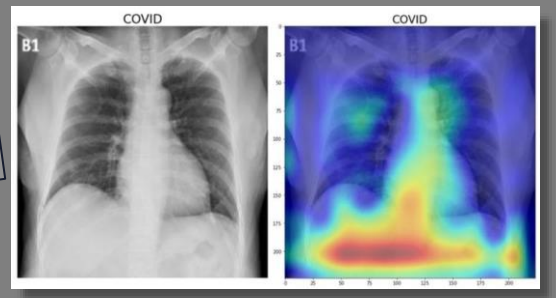
1. Reinforcement learning with Binarized NN

New Zealand



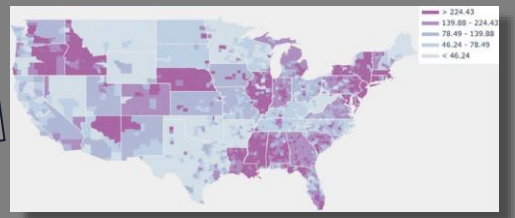
2. AI-based X-ray Covid detection

Greece



3. COVID19 prediction with graph

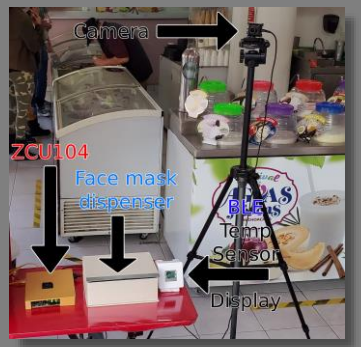
Singapore



Intelligent Video Analytics (ZCU104)

1. Facemask Detector (and thermal)

Mexico

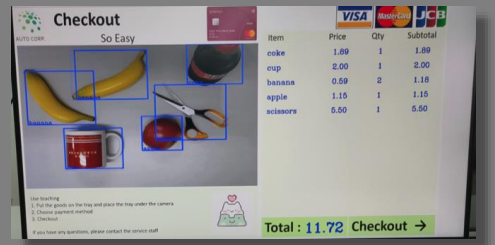


2. Automatic fall detection for elderly people

India

3. Real-time Smart PoS System

Taiwan



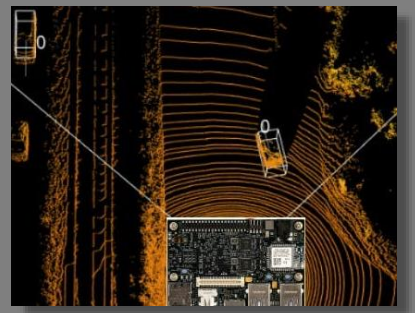
Adaptive IoT (U96)

1. Hand-gesture controlled drone

VT, USA

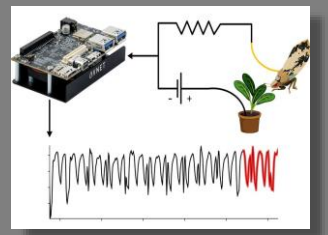
2. Real-time 3D Perception

Ireland



3. Time Series Similarity Prediction

CA, USA



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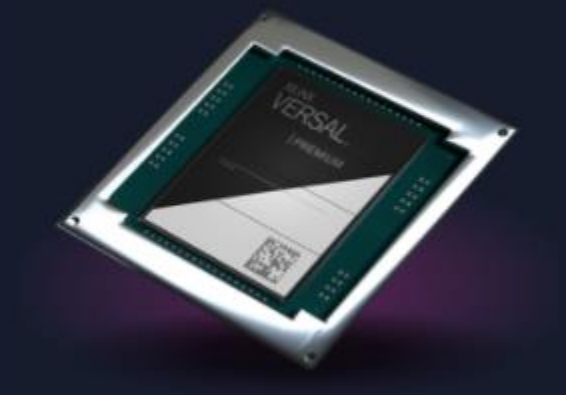
Vivado – A modern EDA tool

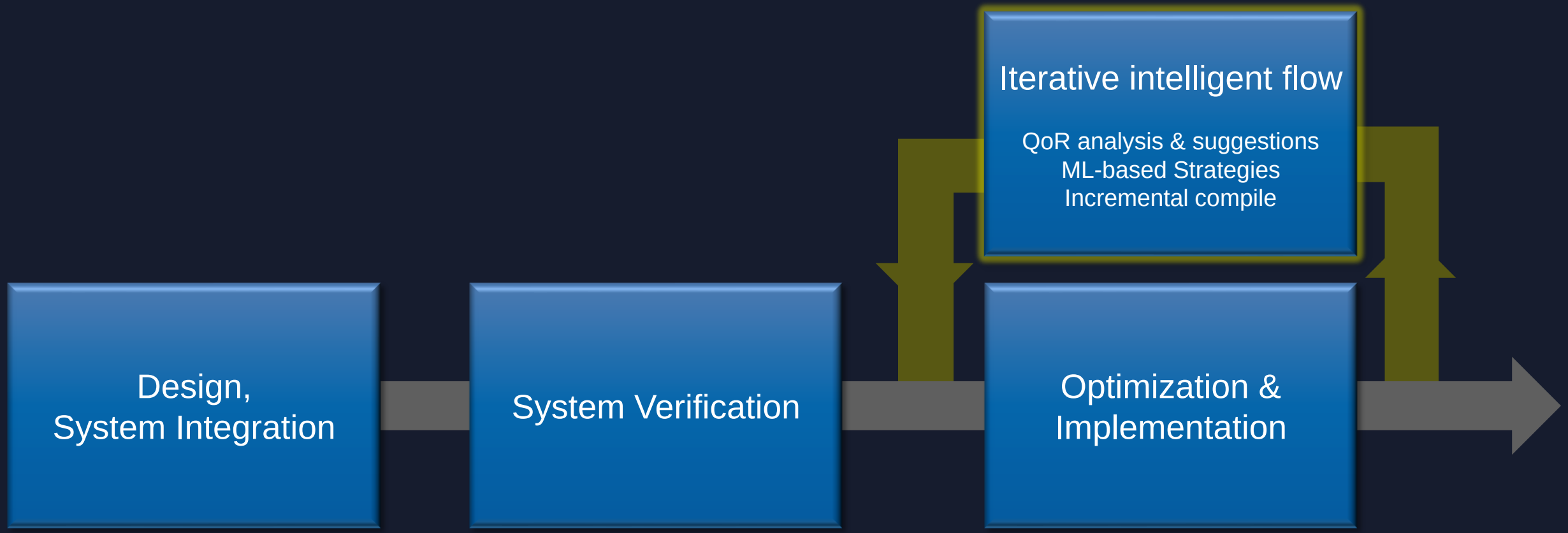
- State-of-the-Art Technology

- Methodology & Best Practices



- System-level design & verification with Versal

Vivado Design Flow Overview



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Compile Time Reduction

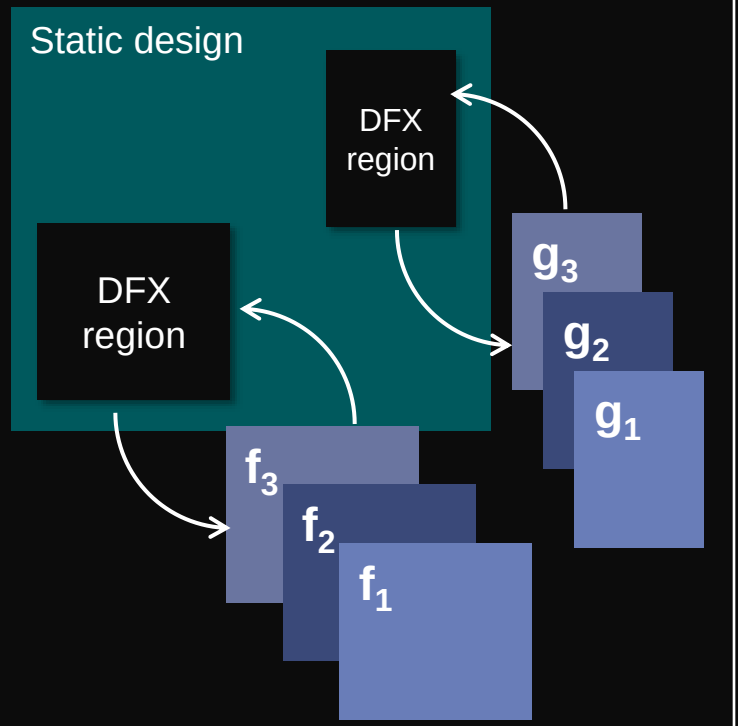
Methodology

Guidelines for fastest design closure

- Best practices for design closure
- Board, RTL, constraints, P&R

Dynamic Function eXchange

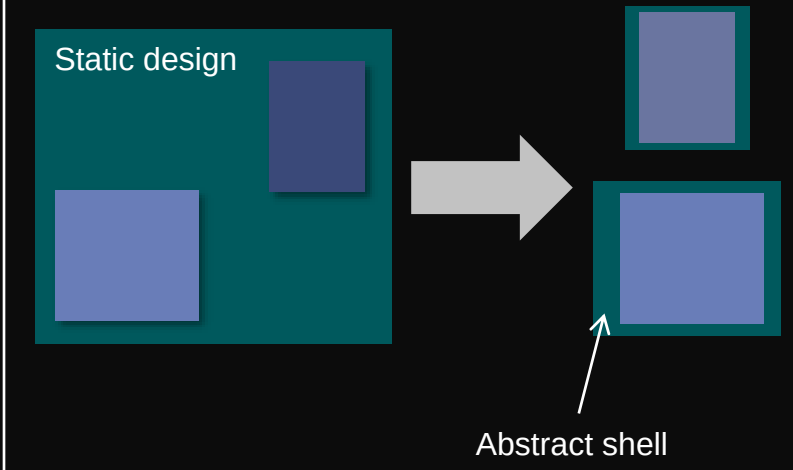
Time multiplexing of HW functions



- Increase device capacity
- Over the air update

Abstract Shell for DFX

Abstraction of the static design

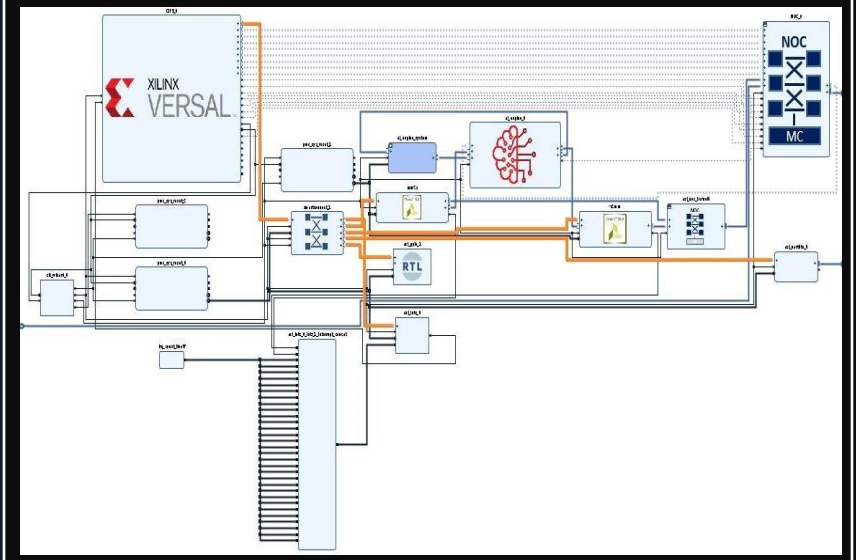


- Compiles 2-10x faster
- Static design security

Design Cycle Reduction

IP Integration (RTL, HLS, MATLAB)

IP-centric system integration



- Team design, CI, DFX
- Timing Closure at system level

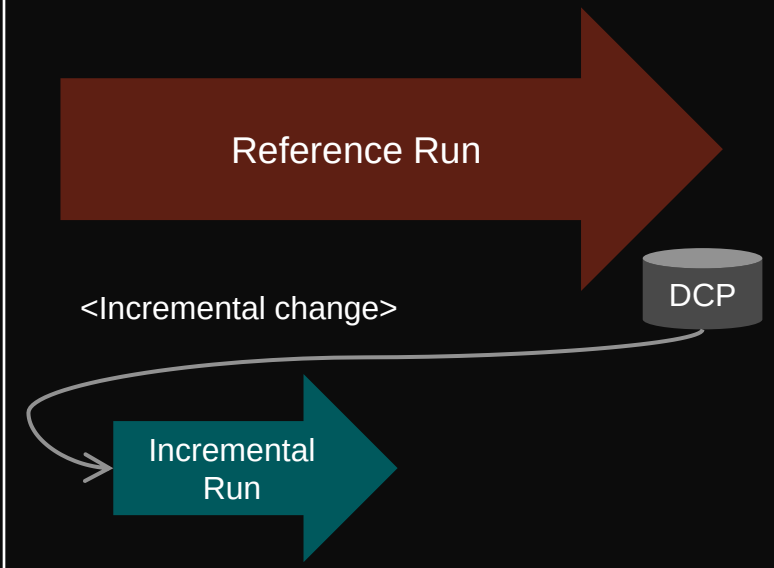
I² (intelligent iterative) Flow

QoR Analysis + ML strategies

- 10% automated QoR boost
- Expert in the box!

Incremental Compile

Guided flow for small changes



- 2x faster compile time
- Incremental synthesis and P&R

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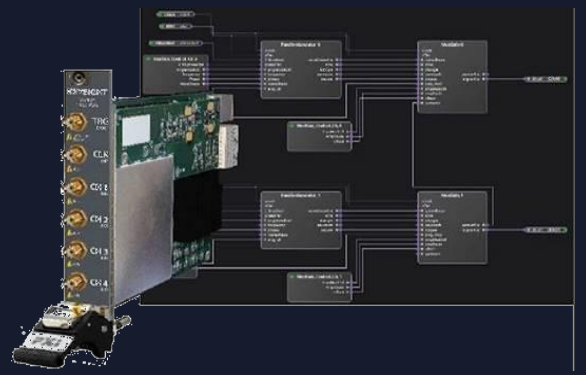
Recent Customer Successes

KEYSIGHT TECHNOLOGIES

PathWave FPGA



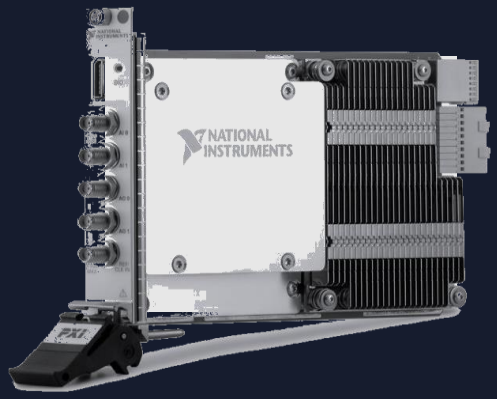
66% compile time reduction w/ DFX & Abstract Shell

abaco SYSTEMS

SBC3511

COTS vendor DFX & Abstract Shell

PXI systems



I^2 flow helped meet timing in first attempt

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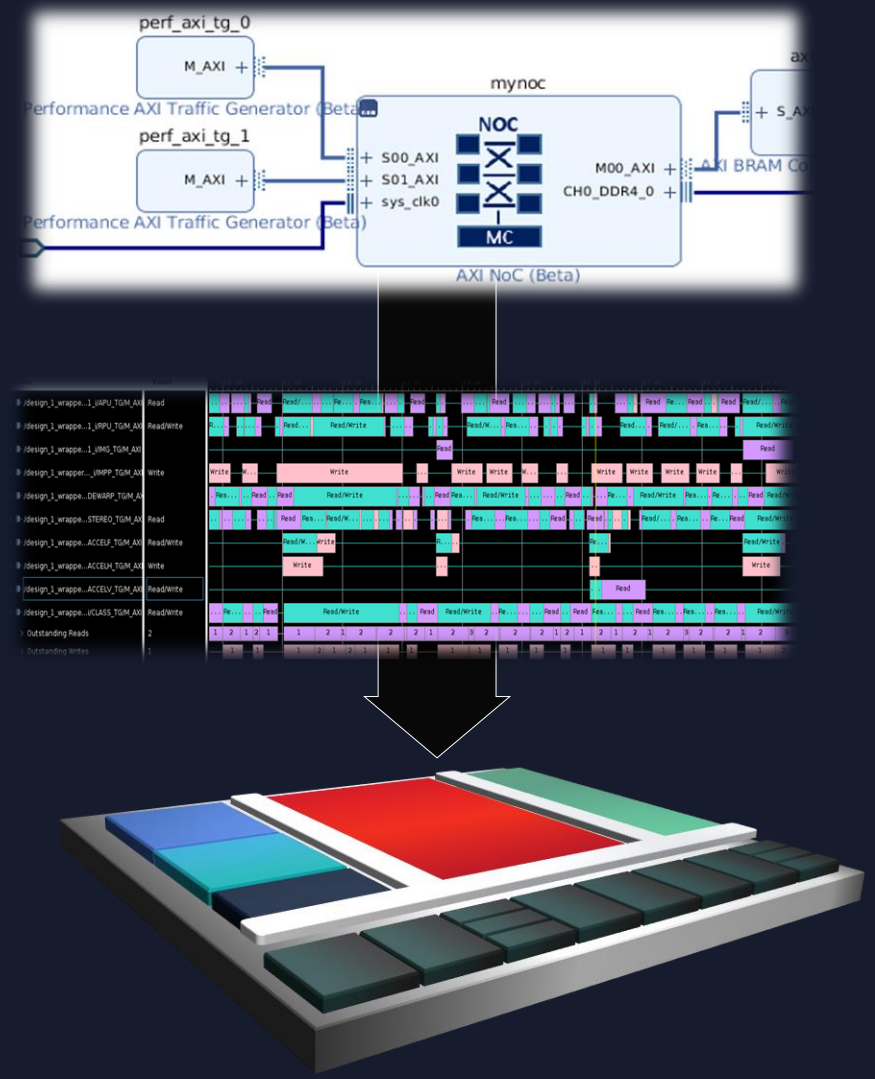
System Design for Versal

IP Integrator design with NoC compiler

System-level traffic analysis

System co-simulation of PS, PL, AI Engine

Implementation & Hardware Debug



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Xilinx App Store

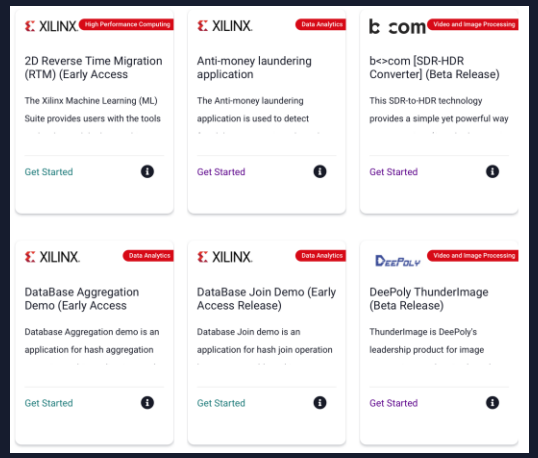
Accelerate Everything.

View App Catalog

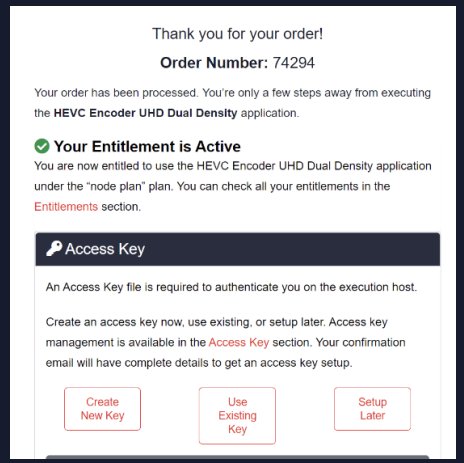
Xilinx.com/AppStore

Three-Step, Ten-mins to Evaluation on Alveo or Cloud

Step 1: Select an app

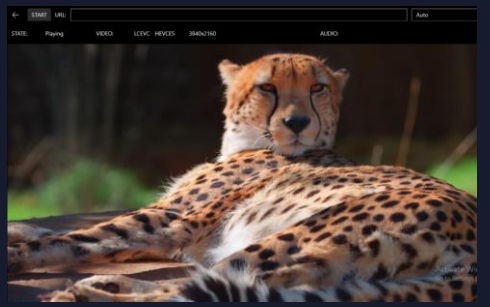


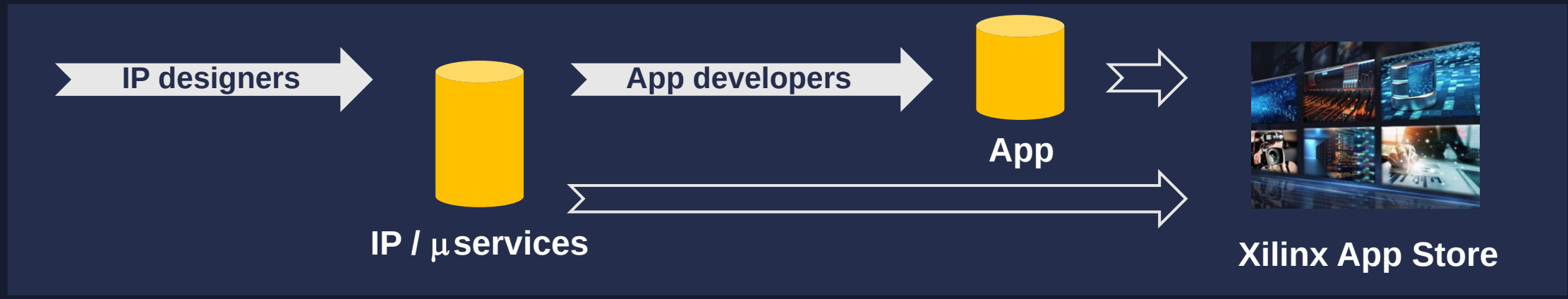
Step 2: Entitlement



Step 3: Download & Run

```
docker pull hubxilinx/vnova_pplus_alveo_u200:ppxde-demo
docker run -v /tmp/cred.json:/vnova_pplus/cred.json:Z
```





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Call to Actions

- Adopt Vivado methodologies & latest features
  I^2 Flow, Abstract Shell, DFX

- Try out new tutorials on GitHub

- Contribute to the Xilinx App Store
  Monetize you IP or Application

Thank You