IBIS-AMI Modeling of Asynchronous High Speed Link Systems

Speakers

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SPEAKERS

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received his Ph.D. degree in Electrical and Computer Engineering from University of California, San Diego in 2006. He joined Xilinx in 2013 and is now a senior staff Design Engineer, working on SerDes architecture development and circuit design. From 2010 to 2013, he was with SerDes design team at Oracle Corporation, where he worked on circuit design and architecture modeling. Prior to that, he worked on SerDes characterization at Texas Instruments, Dallas. His current interests are SerDes architecture development and modeling, high speed mixed-signal circuit design and optimization, and system level modeling.

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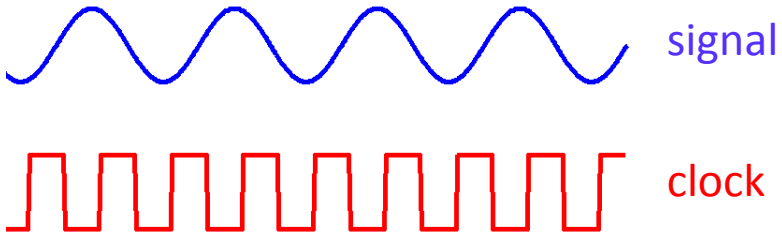
is a master R&D engineer at Keysight Technologies. He received his Ph.D. degree in theoretical physics from Northwestern University. He joined Agilent/Keysight EEsoft in 2006 and works on Analog/RF and SI simulation technologies in ADS. From 2003 to 2006 he was with Cadence Design Systems, where he developed SpectreRF Harmonic Balance technology and perturbation analysis of nonlinear circuits. Prior to 2003 he worked in the areas of EM simulation, nonlinear device modeling, and medical imaging.

Outline

- **Synchronous and Asynchronous Systems**
  - Synchronous and Asynchronous Definition
  - Embedded clocks in SerDes systems
  - Clock Data Recovery (CDR)
  - CDR Architecture Example
- **IBIS-AMI Modeling Overview**
- **IBIS-AMI Simulation for Asynchronous Systems**
- **Asynchronous System Simulation and Measurement**
  - CDR Tracking, eye diagram and bathtub curves
  - Frequency offset tolerance
  - Jitter tolerance
- **Conclusions and Future Work**

Synchronous and Asynchronous Systems

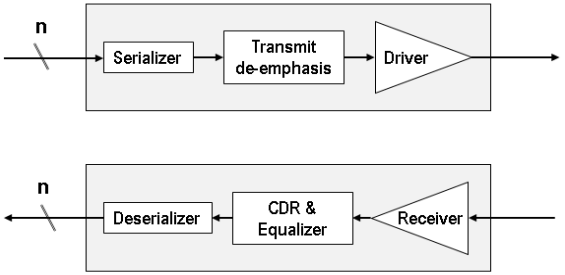
- Synchronous System
  - Signal has the same frequency as the local clock and has a fixed phase offset
    - ✓ $\Delta f = 0,\ \Delta\Phi(\mathrm{t}) = \text{constant}$
- Asynchronous System
  - Mesochronous
    - ✓ $\Delta f = 0,\ \Delta\Phi(\mathrm{t})\ \text{is bounded}$
  - Plesiochronous
    - ✓ $\Delta f \neq 0, \text{but very small}$
  - Heterochronous
    - ✓ $\Delta f \neq 0$

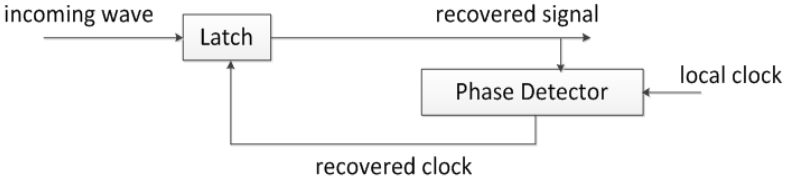


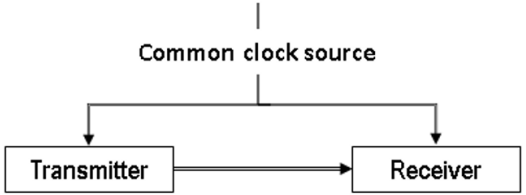
$$\text{Signal Phase} - \text{Clock phase} = \Delta f \times t + \Delta\Phi(\mathrm{t})$$

SerDes Clocking

- Clock in SerDes
  - Clock information is embedded in the serial data
  - RX needs to recover the clock from the incoming waveform and use it to latch the data
  - Common clock – when both the TX and the RX are sharing the same common clock source $\Delta f = 0$
    - ✓ Only phase needs to be recovered
  - Independent clock – the TX and the RX do not share the same clock source (Plesiochronous)
    - ✓ Both the phase and the frequency need to be tracked



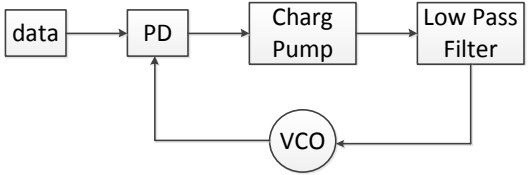




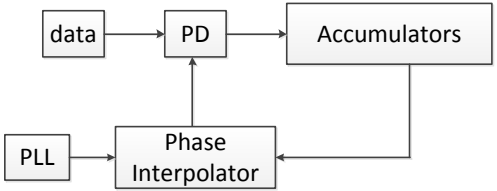
SerDes Clock Data Recovery (CDR)

- Two types of CDR in SerDes Systems
  - Burst mode system (often in a point-to-multipoint applications)
    - ✓ Applications include GPON, EPON and LANs
    - ✓ Commonly used CDR architectures include gated oscillators or oversampling techniques
  - Continuous mode system (often used in a point-to-point applications)
    - ✓ Applications include SONET, Fiber Channel and Gigabit Ethernet
    - ✓ Commonly used CDR architectures include PLL-based or Phase Interpolatro (PI)-based
    - ✓ PLL based clock data recovery does not produce quantized phase error
    - ✓ Phase interpolator from each channel can share the same PLL

PLL based clock data recovery

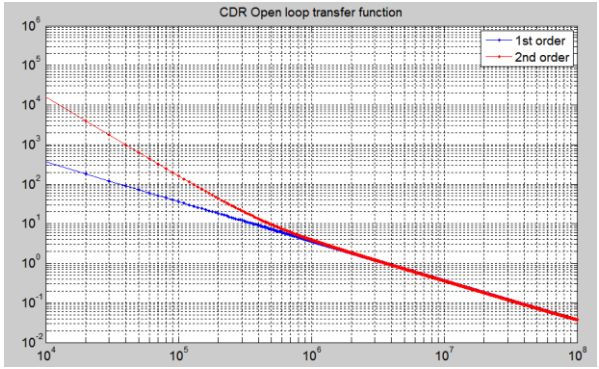


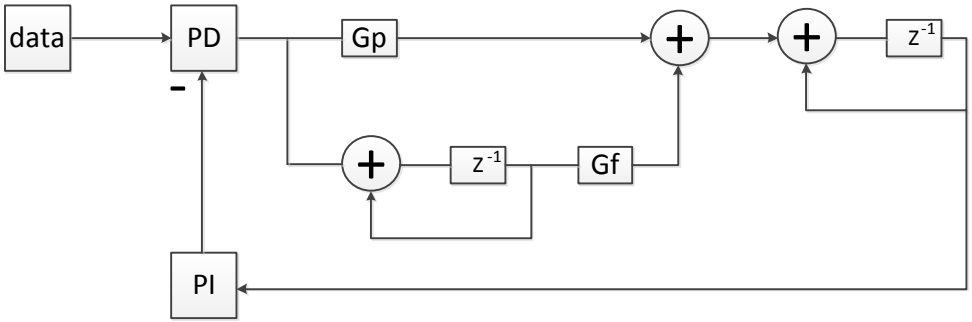
Phase Interpolator based clock data recovery

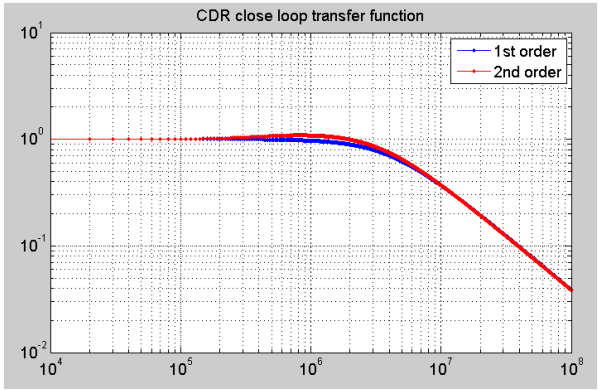


CDR Architecture Example

- PI-based CDR loop can be categorized into
  - 1st order loop, which is inherently stable
  - 2nd order loop, which can track frequency offset





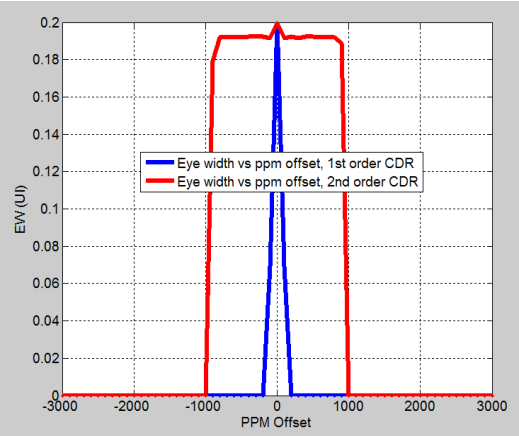


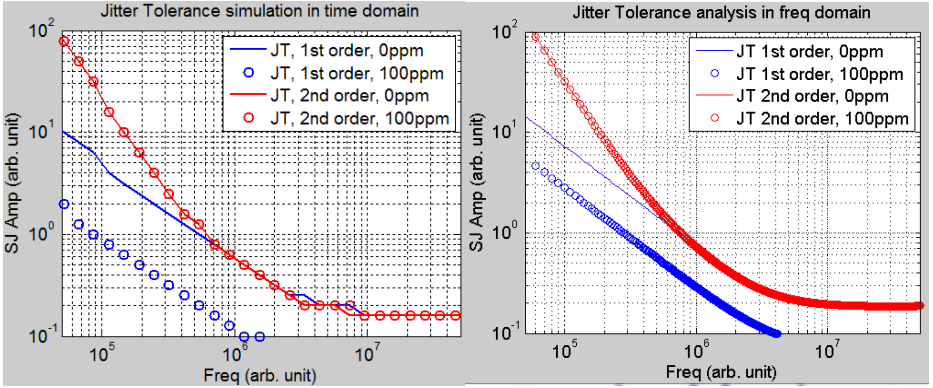
CDR Architecture Example – Cont'd

- With frequency offset present, 1st order CDR would lead to phase tracking error that is proportional to the ppm offset

$$P_e^{1st-order} \sim \frac{\Delta f}{G_{pi} \times G_p}$$

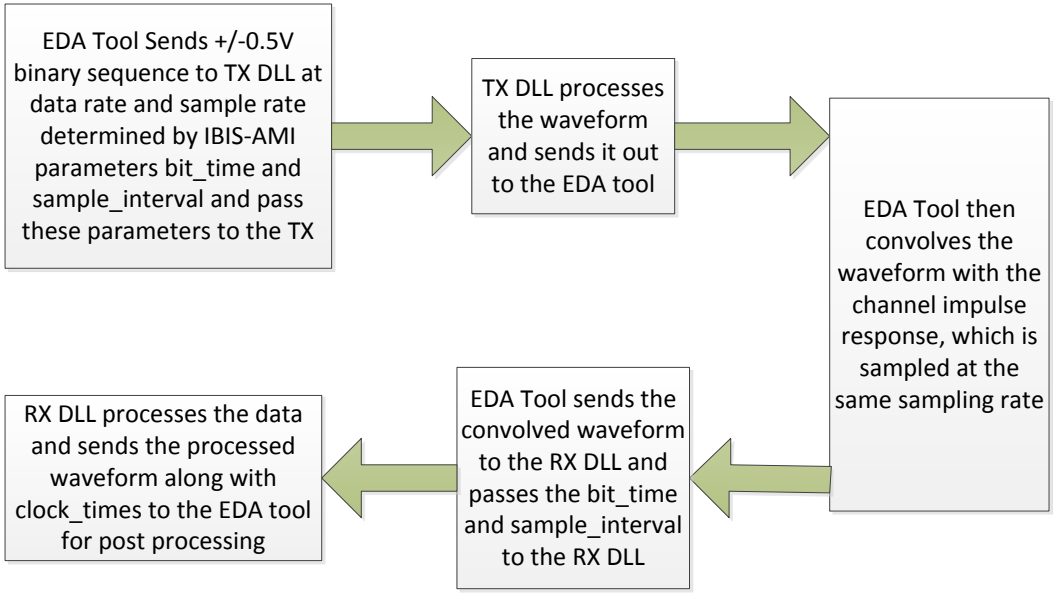
- This will affect the eye margin and jitter tolerance
- Frequency and time domain architecture model can predict the CDR behavior and margin loss
- IBIS-AMI simulation is desired for higher accuracy and to account for the convergence complexities and interactions among various adaptation loop in the SerDes system





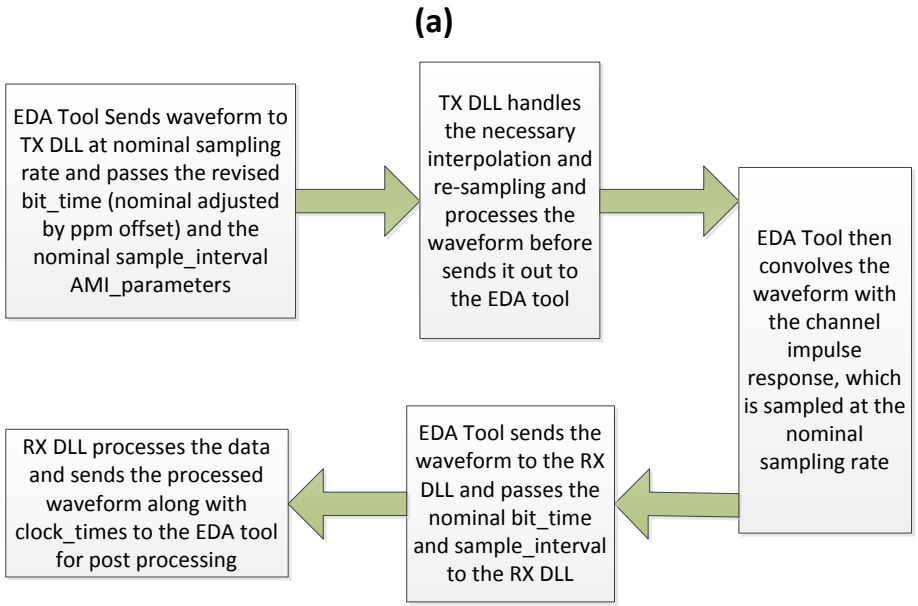
IBIS-AMI Modeling Overview

- TX DLL input is a Binary Sequence switching between 0.5V and -0.5V
- TX output is convolved with channel impulse response
- The convolved waveform is input to the RX DLL
- RX processes the data and sends equalized signal and clock ticks to the simulator for post processing



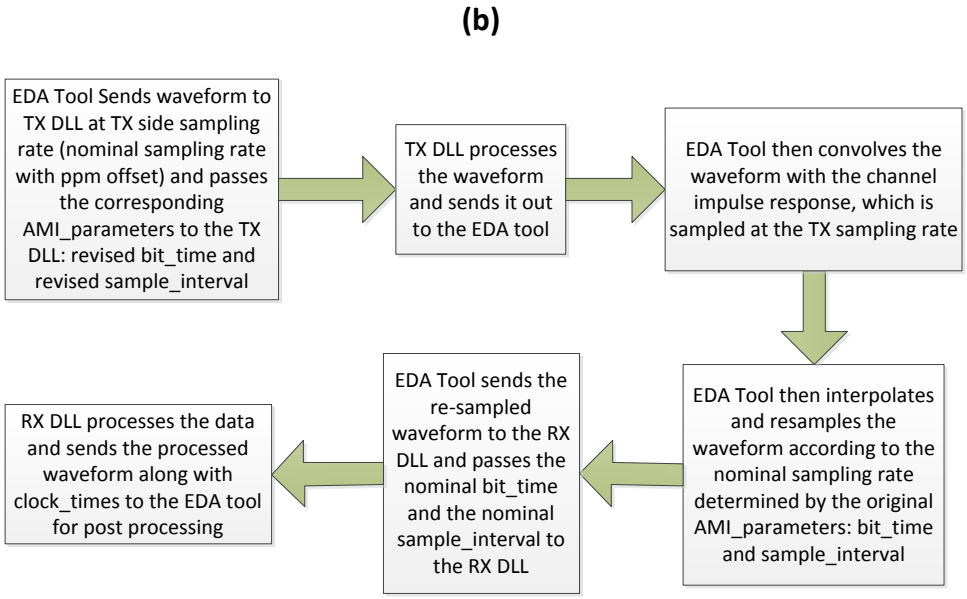
Simulation Approach for Async Systems (a)

- To simulate the asynchronous system
  - The EDA tool needs to send different bit_time (determined by the data rate and the offset) to the RX and the TX
  - The offset can be added either on the TX side or on the RX side
  - The system sample time sample_interval can be kept constant
  - AMI DLL needs to handle any real number bit_time and sample_interval (which may lead to non-integer samples per bit)



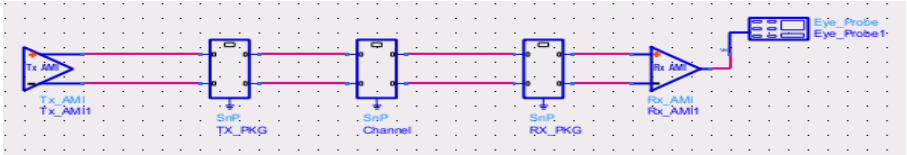
Simulation Approach for Async Systems (b)

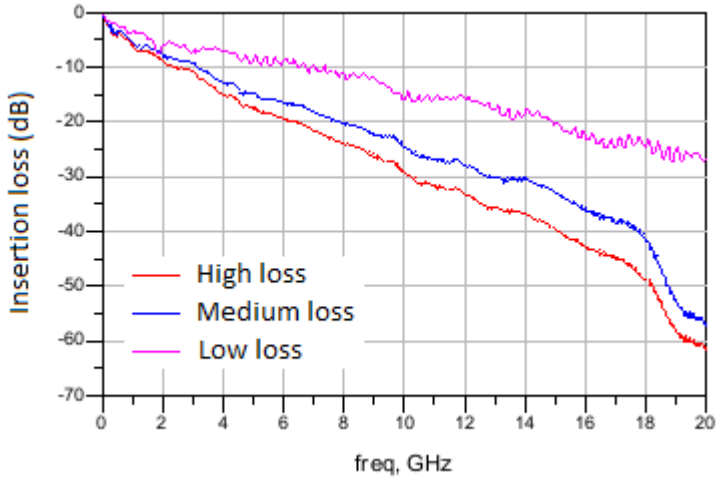
- Alternative approach
  - The EDA tool needs to send different bit_time (determined by the data rate and the offset) and different sample_interval to the RX and the TX
  - The offset can be added either on the TX side or on the RX side
  - The EDA tool needs to do the necessary interpolation and re-sampling between the corresponding blocks

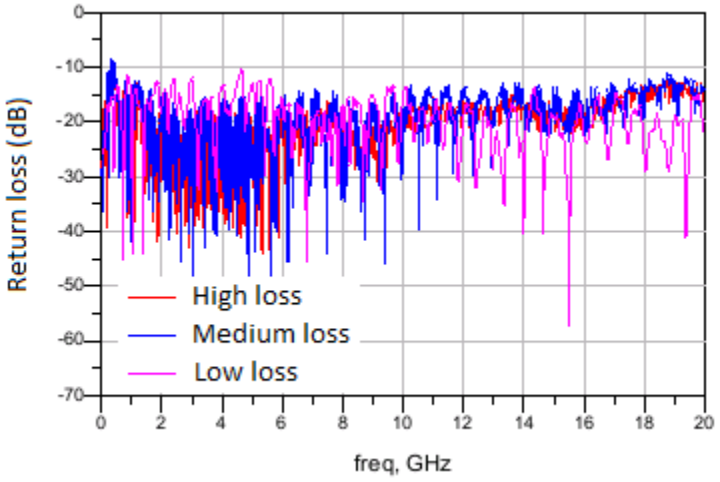


Simulation Setup

- Channel and Simulation Setup
  - Three channels were selected with IL at 36dB, 30dB and 18dB, respectively at 14 GHz
  - Data rate at 28 Gbps
  - PRBS-23 for 2M bits
  - Offset added on the TX side in unit of Δf



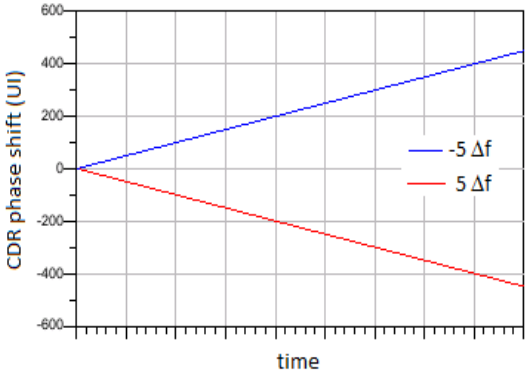


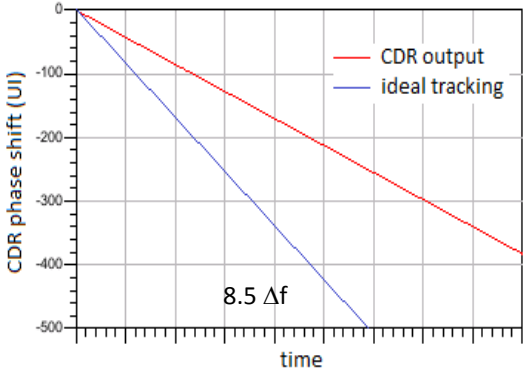


Simulation Results – CDR Phase Shift

- High Loss Channel (36dB)
  - With +/-5Δf offset, the CDR is able to track and the eye is open
  - With 8.5 Δf, the offset is outside of the CDR capture range and the eye is closed
  - Phase shift can be calculated from the clock ticks using the equation below

$$phase\ shift(n) = \frac{t_{clk}(n) - t_{clk}(0)}{T_0} - n$$

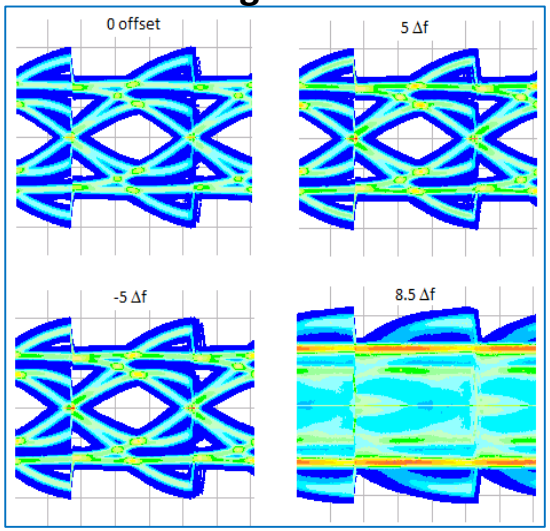




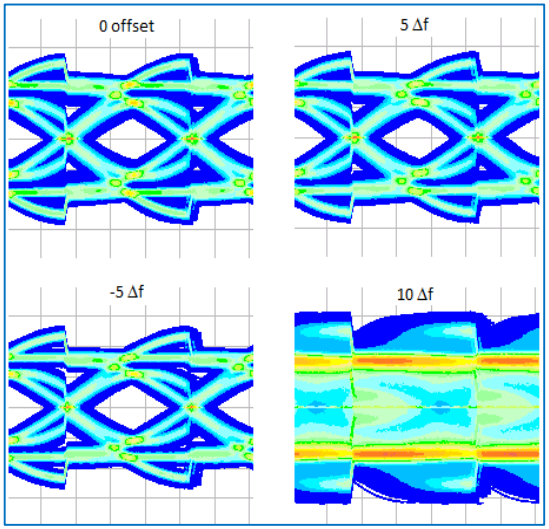
Simulation Results – Eye Diagram

- Eye diagrams
  - Within CDR frequency locking range, eye diagram is negligibly affected
  - Outside of the CDR frequency capture range, eye is completely closed

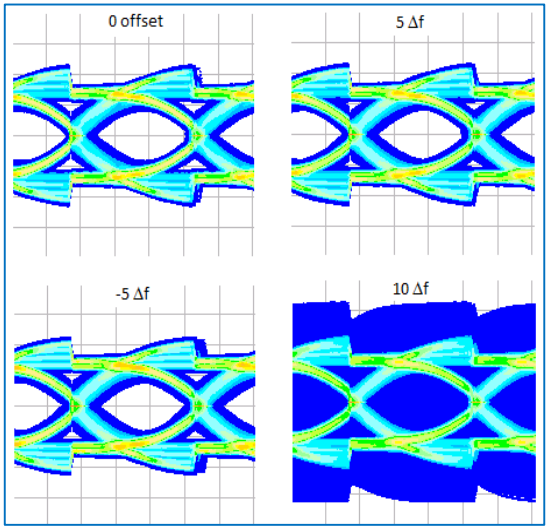
High Loss



Medium Loss



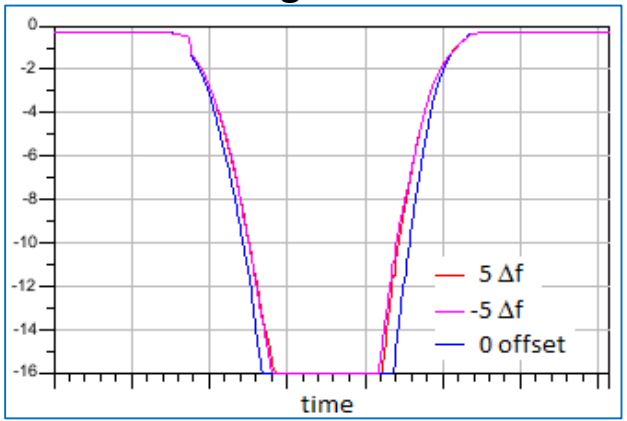
Low Loss



Simulation Results – Bathtub Curves

- Bathtub curves
  - Within CDR frequency locking range, BER is only slightly affected
  - The CDR locking point is not noticeably changed

High Loss



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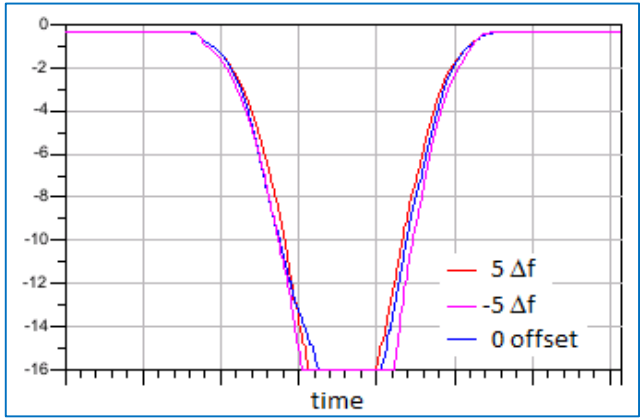

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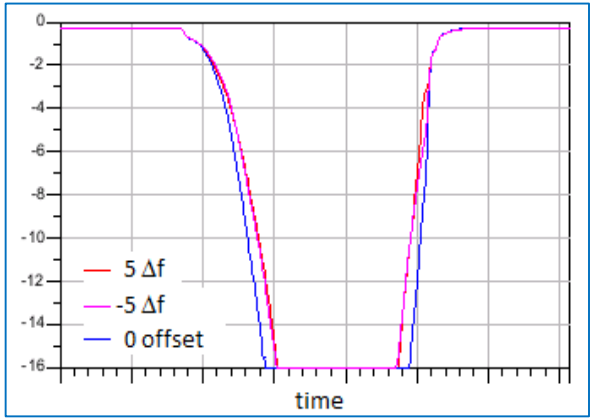
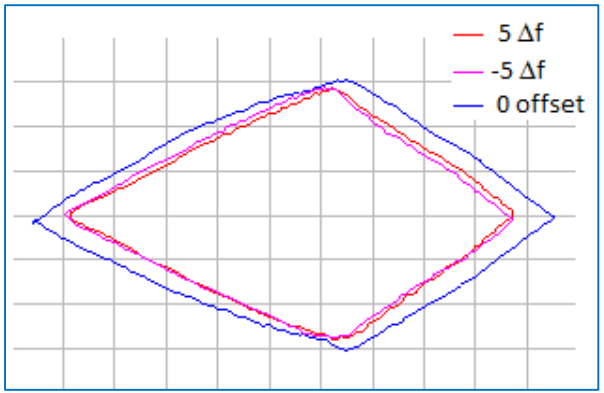


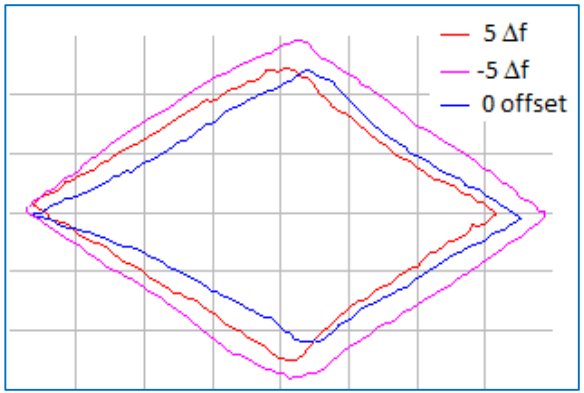
Simulation Results – Eye Contours

- Eye contours
  - Within CDR frequency locking range, eye contour is comparable
  - The eye contour symmetry is largely retained

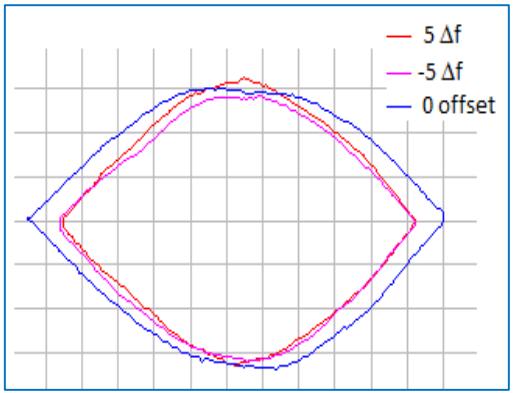
High Loss



Medium Loss

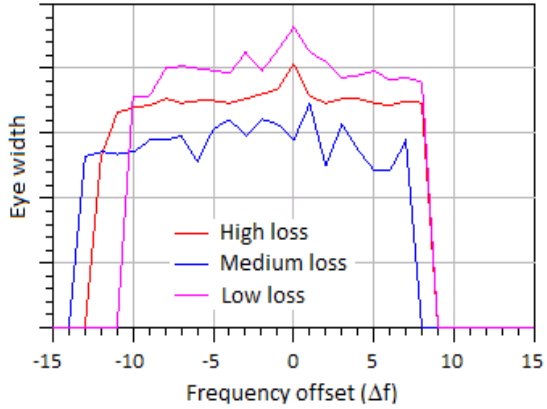


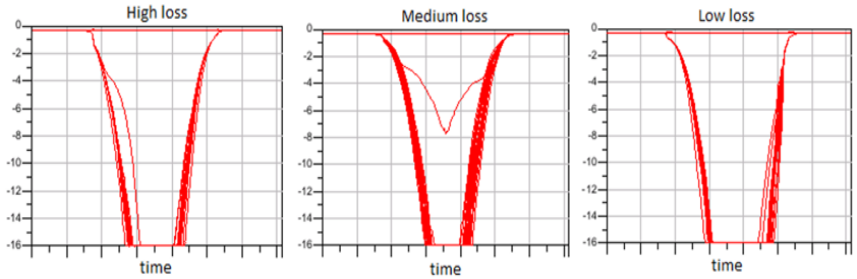
Low Loss

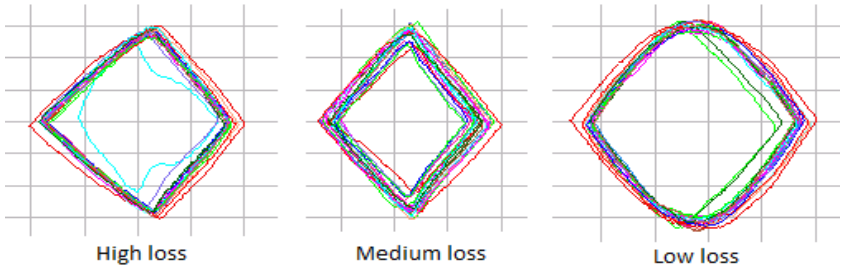


Frequency Offset Impact with 2nd Order CDR

- Eye Width (EW) vs. Frequency Offset with 2nd Order CDR
  - Within the locking range, EW is only slightly affected, regardless of the amount of the frequency offset
  - Within the locking range, the locking point is also largely unaffected
  - The perceived capture range asymmetry is caused by the initial phase difference and the convolved capture process

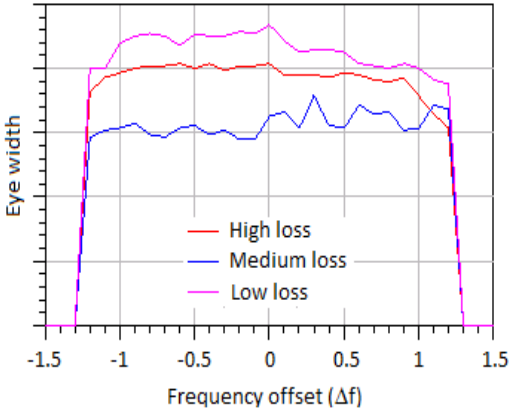


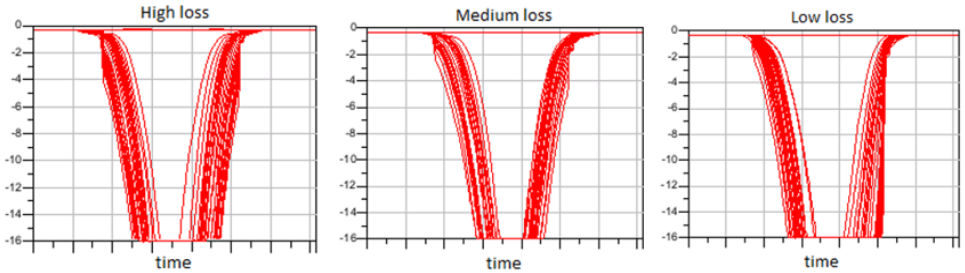


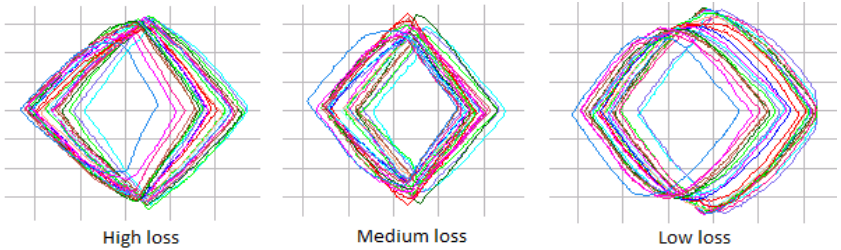


Frequency Offset Impact with 1st Order CDR

- Eye Width (EW) vs. Frequency Offset with 1st Order CDR
  - The locking point is shifted proportionally to the amount of the frequency offset
    - ✓ Positive offset moves the locking point to the right
    - ✓ Negative offset moves the locking point to the left
  - The effective EW (2*min(left half EW, right half EW)) is reduced proportional to the frequency offset, although the perceived EW remains (left half EW + right half EW) roughly constant

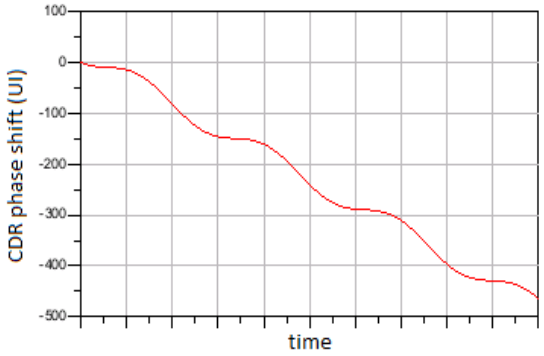


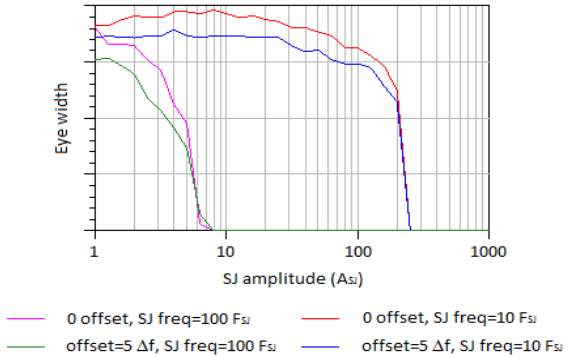


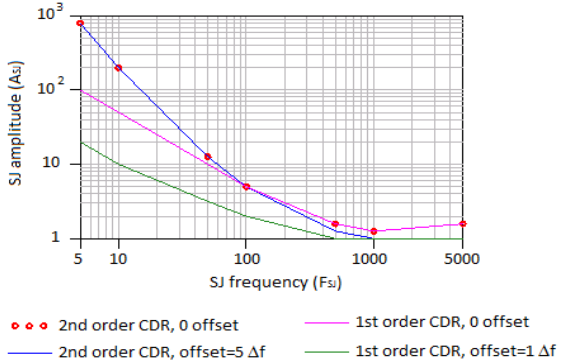


Frequency Offset Impact on Jitter Tolerance

- Frequency Offset Impact on Jitter Tolerance
  - Within the CDR bandwidth, CDR phase follows the data phase (SJ + offset), and the tolerable SJ amplitude and the EW is inversely proportional to the SJ frequency
  - EW is slightly affected when the offset is present
  - 2nd order CDR: freq offset does not affect jitter tolerance if it is within the CDR tracking range
  - 1st order CDR: freq offset reduces the jitter tolerance proportionally to its magnitude







Conclusions and Future Work

- IBIS-AMI simulation flow for asynchronous serial link systems is discussed
- The methodology is demonstrated through IBIS-AMI simulation examples
- With the inclusion of asynchronous simulation, better simulation accuracy can be achieved, which is valuable for system level budgeting
- Following the same principle, we can explore the feasibility of simulating channels with SSC in the future

References

[1] IBIS Specifications 5.0

[2] IEEE P802.3bj™/D3.2, “Draft Standard for Ethernet Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables

[3] David Robert Stauffer, Jeanne Trinko Mechler, Michael A. Sorna, Kent Dramstad, Clarence Rosser Ogilvie, Amanullah Mohammad, James Donald Rockrohr, “High Speed Serdes Devices and Application”, Springer Science & Business Media, 2008

[4] Borivoje Nikolić, “Advanced Digital Integrated Circuits”, http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee241_s04/lectures/Lecture21-Timing.pdf

[5] Ming-ta Hsieh and Gerald E. Sobelman, “Architectures for Multi-Gigabit Wire-Linked Clock and Data Recovery”, IEEE circuits and systems magazine, 4th quarter 2008

Thank you!

QUESTIONS?