DesignCon 2016

Novel Methodology of IBIS-AMI Hardware Correlation using Trend and Distribution Analysis for high-speed SerDes System

Hong Ahn, Xilinx
hong.ahn@xilinx.com

Seungyong(Brian) Baek, Cisco
sebaek@cisco.com

Ivan Madrigal, Xilinx
ivanm@xilinx.com

Hongtao Zhang, Xilinx
hongtao@xilinx.com

Jiali Lai, Cisco
jiallai@cisco.com

Mike Sapozhnikov, Cisco
msapozhn@cisco.com

Geoff Zhang, Xilinx
geoffz@xilinx.com

Alan Wong, Xilinx
alanwon@xilinx.com

Chris Borrelli, Xilinx
cborrelli@xilinx.com

Abstract

This paper proposes a new approach for IBIS-AMI correlation using trend and distribution analysis to overcome the limitation of the current correlation methodology. Trend analysis demonstrates the behavior of the internal eye opening of the RX when varying TX settings and distribution analysis shows where IBIS-AMI simulation results are relative to a volume of measurements. The combination of trend and distribution analysis for IBIS-AMI hardware correlation can give enough level of confidence on the optimized settings from simulation.

We applied this new methodology for IBIS-AMI correlation up to 28Gbps and simulation results agreed well with measurements.

Author(s) Biography

Hong Ahn received his Master degree in Electrical Engineering from Korea University, Seoul, Korea in 1995. He is currently working in SerDes Technology Group in Xilinx. His current interests are transceiver application, transceiver validation, signal integrity and system level architecture with transceiver. Prior to joining Xilinx, he worked on NetLogic, Broadcom and LGIC.

Dr. Seungyong Baek is a Signal Integrity Technical Leader at CISCO in San Jose, USA since 2010, he has responsibility for analyzing SI/PI/EMI issues of CAT3k and CAT4k switching system. He worked 4.5 years for Silicon Image since 2005 and He received Ph.D degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2005. He has been working with next generation high-speed backplane system and leading various switching ASIC program. Moreover his researches include model

development of high-speed serial I/O interfaces, developing improved SI/PI analysis methodology.

Ivan O. Madrigal received his Master's degree in Electrical Engineering from San Jose State University in 2012. He joined Xilinx in 2013 as a SerDes Systems Applications Engineer, working on transceiver end-to-end simulation, high-speed protocol characterization, and silicon verification of industry state-of-the-art transceiver circuits. His current interests are SerDes system level end-to-end simulation, signal integrity, high-speed protocol characterization, and analog mixed-signal circuit design and silicon verification.

Hongtao Zhang received his Ph.D. degree in Electrical and Computer Engineering from University of California, San Diego in 2006. He is currently a senior staff SerDes architect at Xilinx, Inc., developing SerDes architectures for both NRZ and PAM4 signaling. From 2010 to 2013, he was with SerDes design team at Oracle Corporation, where he worked on circuit design and architecture modeling. Prior to that, he worked on SerDes characterization at Texas Instruments, Dallas. His current interests are SerDes architecture development and simulation, analog and digital circuit implementation and optimization, and system level modeling.

Jiali Lai is a Signal Integrity Engineer at Cisco Systems since 2014. She has engaged in signal and power integrity for Catalyst 3K and 4K switching systems. Jiali worked at Qualcomm for 1 year before joining Cisco. She received her Ph.D. in Electrical Engineering from University of California, Davis

Mike Sapozhnikov is a Signal Integrity Manager at Cisco Systems. He is responsible Signal and Power Integrity for Catalyst access switching and ASR9K edge routing for both system and ASIC designs. Mike has over 18 years of experience in various Signal Integrity and HW design roles as a Manager and Individual Contributor. Mike received his B.S. in electrical engineering from SJSU.

Geoff Zhang received his Ph.D. in 1997 in microwave engineering and signal processing from Iowa State University, Ames, Iowa. He joined Xilinx Inc. in 2013 as director of architecture and modeling in the SerDes Technology Group. Prior to joining Xilinx he has employment experiences with HiSilicon, Huawei Technologies, LSI, Agere Systems, Lucent Technologies, and Texas Instruments. His current interest is in transceiver architecture modeling and system level end-to-end simulation, both electrical and optical

Alan Wong is a SerDes Applications Manager at Xilinx SerDes Technology Group. He leads a team responsible for SerDes applications, transceiver electrical compliance, IBIS-AMI hardware correlation, and pre-sales / post-sales support. He earned his BS in Computer Engineering from University of Toronto and MS in Computer Engineering from San Jose State University.

Christopher Borrelli was born in The United States in 1976. He received the B.S. degree in Computer Engineering from Villanova University, U.S., in 1998. He joined

Xilinx in 1998 and has held various positions including Technical Support, RTL Engineer, and SerDes Applications Engineer. He is currently the Director of SerDes System Engineering and Applications at Xilinx.

Introduction

Multi-gigabit serial link channels using Serializer/Deserializer (SERDES) are becoming prevalent, and moving rapidly to 28Gbps and higher. Link simulation is crucial to determine if a multi-gigabit differential link meets the system requirement. SERDES models, the most important element, are traditionally available as transistor level models that are encrypted to protect intellectual property of the vendor. While these transistor level SERDES models provide the most accurate results that include both linear and non-linear effects, due to large simulation time, the user cannot achieve results at the low bit-error-rate (BER) required by most modern standards. As an alternative to reduce simulation time, IBIS-AMI models have been proposed, and primarily used to predict low BER result in a serial link at much faster simulation time. For more accurate simulation results and optimized link, IBIS AMI models needs to be correlated with silicon to reflect the distribution of parts across the variation of process-voltage-temperature (PVT). This correlation between IBIS-AMI model and silicon becomes more critical to achieve and guarantee optimized settings from simulation.

Most of IBIS-AMI correlation is performed under specific settings and small number of silicon parts with little regard to PVT variation. This approach cannot guarantee accurate correlation throughout all other settings under distribution of real parts across PVT. Simulation results need to follow behavioral trends from real hardware measurements with all possible combinations of the controllable settings under reasonable tolerance. Consequently, the results need to reflect the distribution of real measurement across PVT in order to achieve reliable simulation optimization in a mass production system. [5][6]

This paper proposes a new approach for IBIS-AMI correlation using trend and distribution analysis to overcome the limitation of the current correlation methodology.

Proposed Methodology

We have proposed the trend correlation[7] and distribution correlation for IBIS-AMI model correlation instead of the absolute value correlation or simple waveform correlation.

Trend Analysis

The trend correlation means how eye opening that is recovered by RX equalizer is varied when TX equalizer is changed. The trend is able to be verified by the plot of vertical and horizontal opening of RX eye diagram, the plot should be acquired by a lot of combination of TX equalizer such as main cursor, pre cursor and post cursor settings. If the trend between simulation and measurement do not match, the optimized setting from simulation cannot be trusted. However, if the trend would be matched under reasonable tolerance, the optimized transceiver settings from the simulation can give a higher level of confidence with trend-matched simulation.

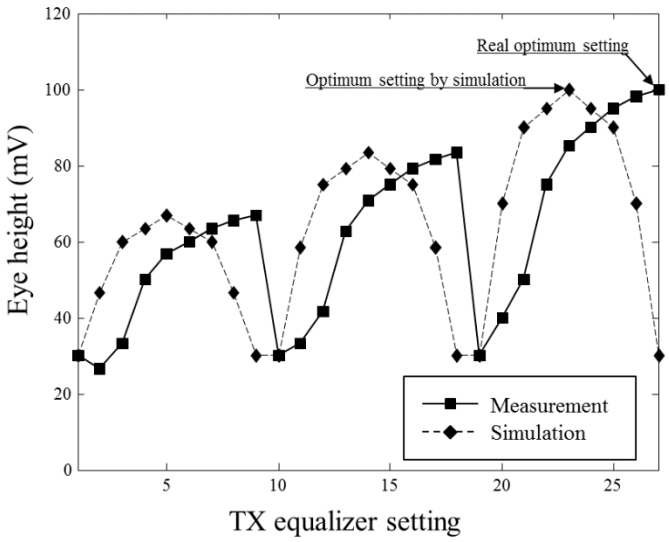

Figure 1 Concept of trend correlation for mismatching case.

Figure1 and 2 show the concept of the trend correlation. As shown in Figure1, if the trend of the simulated eye height doesn't follow the measurement, the optimum TX equalizer setting will be different from real optimum value. But if the trends match like Figure 2, even though the absolute value of eye height is different, the optimum setting will be same.

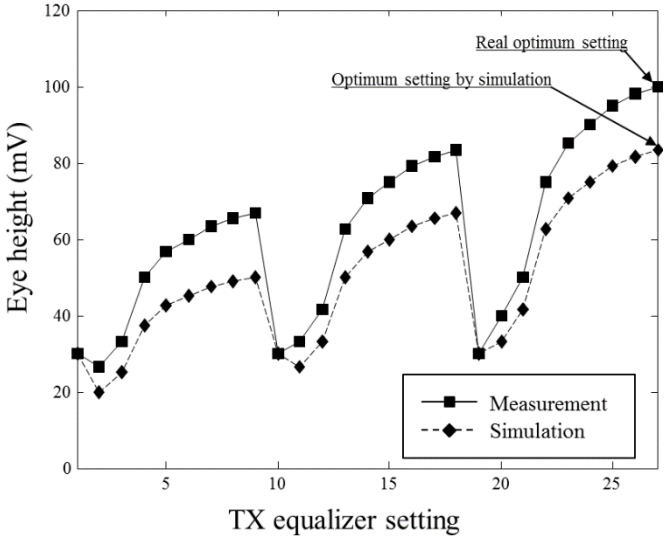

Figure 2 Concept of trend correlation for matching case.

Distribution Analysis

The distribution correlation shows where IBIS-AMI simulation are located inside a volume of measurement across PVT (process-voltage-temperature) variation.
For good distribution correlation, the measurement across PVT variation would be located above the minimum boundary set by the IBIS-AMI simulation. At the same time, the measurement distribution should be sitting beside the simulated boundary as close as possible. If the simulation cannot reflect the distribution of the silicon measurements across PVT adequately, the optimized settings from simulation cannot be trusted across large number of links in mass production system. The combination of trend and distribution analysis for IBIS-AMI hardware correlation can give enough level of confidence on the optimized settings from simulation.

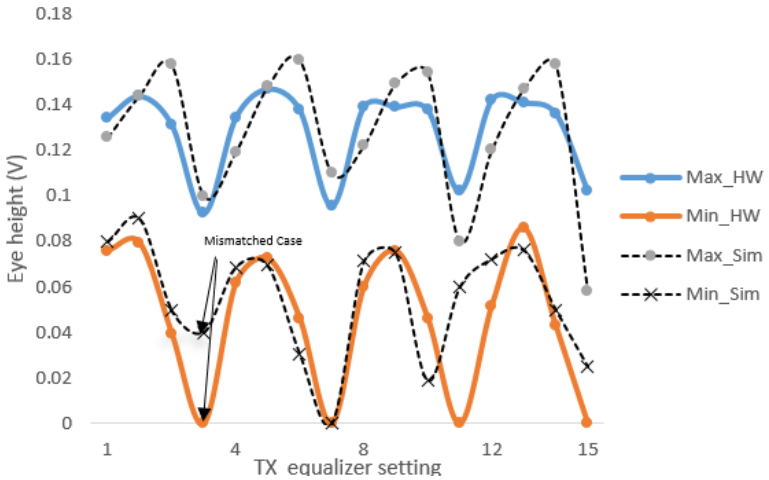

Figure3 Concept of distribution correlation for mismatching case

Figure3 and 4 show the concept of the distribution correlation. As shown in Figure3, if the distribution of the simulated eye heights doesn't locate at the boundary of the distribution of the measurement at specific TX equalizer setting, the simulation result cannot be trusted across the large number of links in real system. But if the distribution of the simulation sits at the one of hardware measurement like Figure 4, the optimization by IBIS-AMI simulation can be much more trustable during future mass production and the link margin can be controllable.

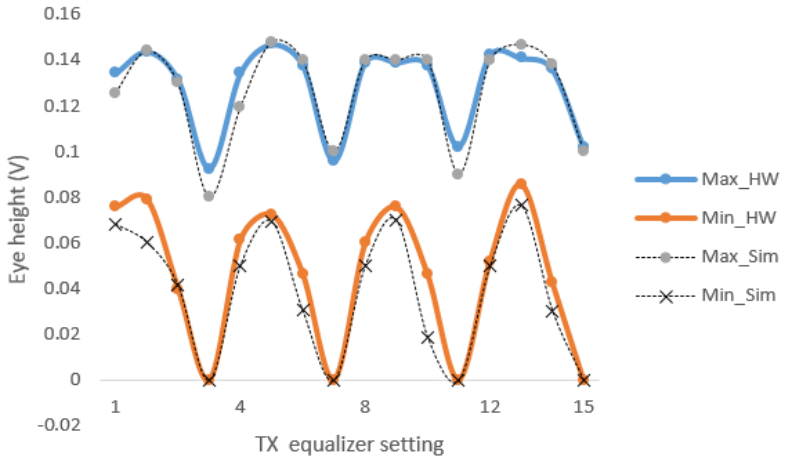

Figure4 Concept of distribution correlation for matching case

Correlation between Hardware and IBIS-AMI Simulation

The following Xilinx transceivers and IBIS-AMI models are used for the correlation.

- Xilinx UltraScale GTH Transceiver
    - 10.3125 Gbps
    - 16.325 Gbps
    - IBIS-AMI Model v3.1
- Xilinx UltraScale GTY Transceiver
    - 28.0 Gpbs
    - IBIS-AMI Model v3.0
    -

Characterization of IBIS-AMI models to hardware require two setups (transmitter measurements, and receiver measurements) to cover all parameters of interests. IBIS-AMI hardware correlation uses a volume characterization system containing the following silicon PVT corners:

- Silicon Process Corners:
    - SS, FF and TT parts
- Voltage Corners:
    - Nominal voltage level
    - -3% of nominal voltage level
    - +3% of nominal voltage level
- Temperature Corners:
    - 70C
    - -40C
    - 100C

In IBIS-AMI simulation, we cover silicon variations mentioned above with three PVT corner settings for the transmitter and receiver models, respectively. Please refer to the

UltraScale GTH/GTY IBIS-AMI User Guide for more information of PVT corner parameters. [1][2][3][4]

Measurement Setup

Setup for the transmitter:

Figure 5 shows the bench setup for transmitter hardware measurements.

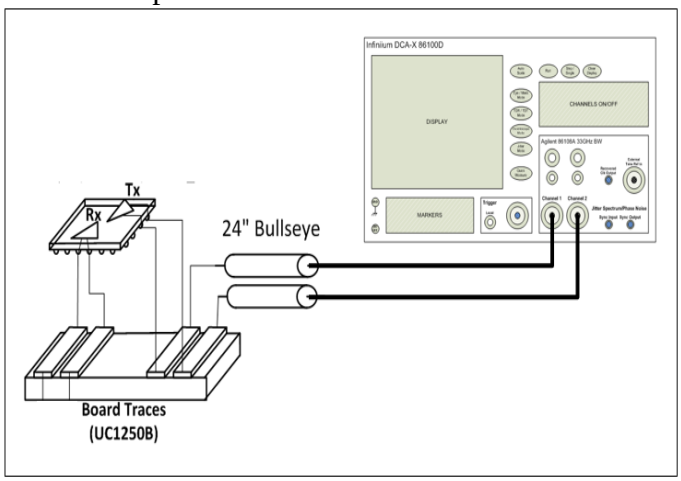

Figure 5 Test Bench Setup for Transmitter Measurements

The transmitter distribution analysis is to measure the TX differential amplitude range. The TX transmits 4Gbps, 20'b0 20'b1 patterns and the differential signal amplitude is measured for each TXDIFFCTRL settings from 0 to 15 using an Infinitum DCA-X 86100D.

For de-emphasis distribution analysis, the TX transmit signal is 10.3125Gbps, 20'b0 20'b1 patter and the pre-emphasis and post-emphasis are swept and recorded from its minimum to maximum value, independently at a given TXDIFFCTRL setting. The de-emphasis measurement is recorded in hardware using an Infinitum DCA-X 86100D

Setup for the receiver:

Figure 6 shows the test bench setup for hardware measurements, and Figure 9 shows the IBIS-AMI test bench setup for simulation. The non-destructive Eye Scan feature in Vivado® is used to capture internal eye width and height using a total bit count of 1E10 bits.

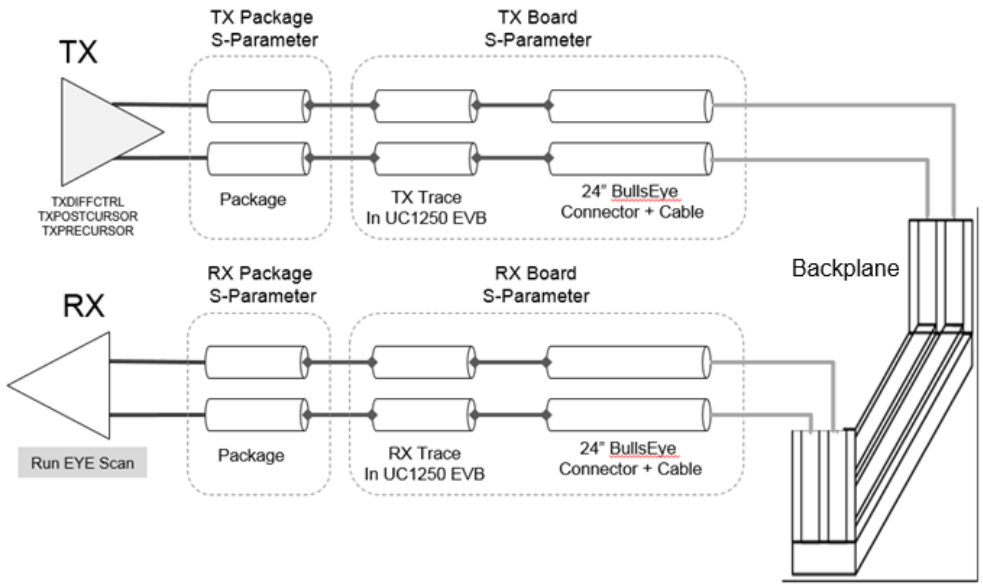

Figure6 Measurement setup for the receiver correlation

Receiver distribution and trend analysis is performed by sweeping discrete transmitter settings using a PRBS31 signal at 10.3125Gbps, 16.375Gbps and 28.0Gbps in a medium and high loss link. In each test case, the internal eye width and height is recorded and compared with the simulation result. The inner eye contour measurements are recorded at BER 1e-10.

Table 1 summarizes the differential loss of backplane channel of each tests.

Case	Line Rate	Xilinx Transceiver	EQ mode	ISI Channel Loss	Diff Insertion Loss
1	16.375Gbps	UltraScale GTH	DFE	High Loss	23dB @ 8GHz
2	16.375Gbps	UltraScale GTH	DFE	Med Loss	19dB @ 8GHz
3	10.3125Gbps	UltraScale GTH	DFE	High Loss	24dB @ 5GHz
4	10.3125Gbps	UltraScale GTH	DFE	Med Loss	18dB @ 5GHz
5	28.0Gbps	UltraScale GTY	DFE	High Loss	28dB @ 14GHz

Table 1 - Test Cases for Receiver Trend and Distribution Analysis

Table 2 summarizes TX equalizer setting to find the trend and distribution. All combinations of TX equalizer setting cannot be swept because of too much time. This paper picks TXPOSTCTRL setting with 4 different categories, [No TX EQ, Small TX EQ, High TX EQ, Over TX EQ], to find the behavior of transceivers.

Case	TXDIFFCTRL	TXPOSTCTRL	TXPRECTRL
1	[B, D, E, F]	[00, 0E, 16, 1F]	[00]
2	[9, B, D, F]	[00, 0E, 16, 1F]	[00]
3	[9, B, D, F]	[00, 0E, 16, 1F]	[00]
4	[6, 7, 9, A]	[00, 0A, 12, 16]	[00]
5	[12,13,14,15]	[00, 0C, 12, 1B]	[00]

Table 2 - Transmitter Settings for Receiver Trend and Distribution Analysis

Channel Model

Most important requirement is the accurate channel model, the correlation errors are frequently happened due to the lack of the model accuracy. Basically, the channel model should be correlated with measurement first before achieving IBIS-AMI correlation.

Xilinx evaluation board coupled with Samtec's Bulls Eye connector are used to connect the transceiver to external equipment. One 24" Bulls Eye cable is included in the evaluation board s-parameter model as Figure 7 shows.

Figure 7 shows the differential insertion loss and return loss of UltraScale GTH evaluation board. This s-parameter is extracted by post-processing the evaluation board measurement.

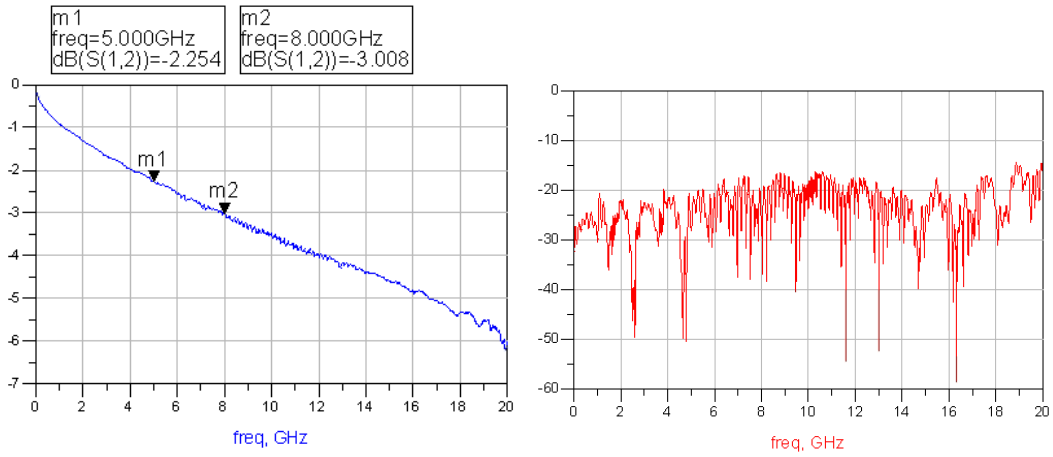

Figure 7 (a) Differential Insertion Loss (b) Differential Return Loss of Evaluation board and 24" cables

Figure 8 shows the correlation of converted TDR from the S-parameter of the evaluation board and hardware TDR measurement of actual board trace. The two TDR graphs are matched well, meaning that the s-parameter models can be trustable for time domain IBIS-AMI simulation.

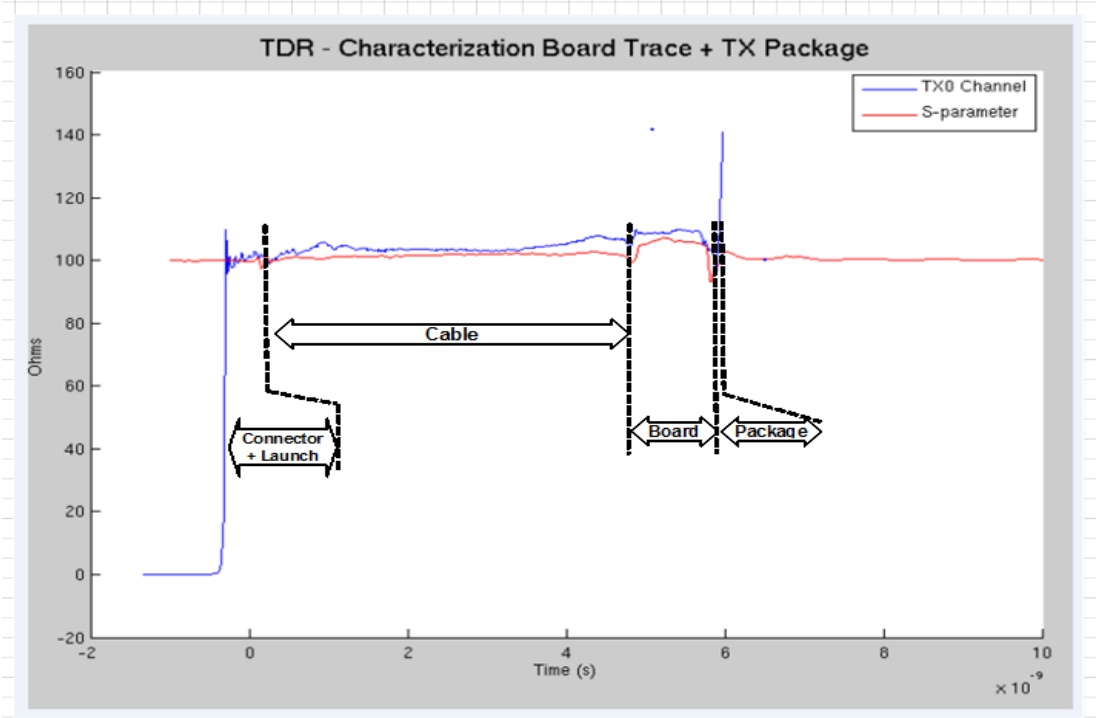

Figure 8 TDR Comparison between converted TDR of S-parameter and measured TDR

Transmitter Correlation

Transmitter correlation is one of important factor to achieve good trend and distribution correlation. The transmitter waveform has been characterized across PVT and compared with IBIS-AMI simulation.

Transmitter Waveform Correlation:
Figure 9 and 10 show the superimposed TX simulation and hardware waveform with PRBS7 pattern which is one of the traditional correlation methodology.

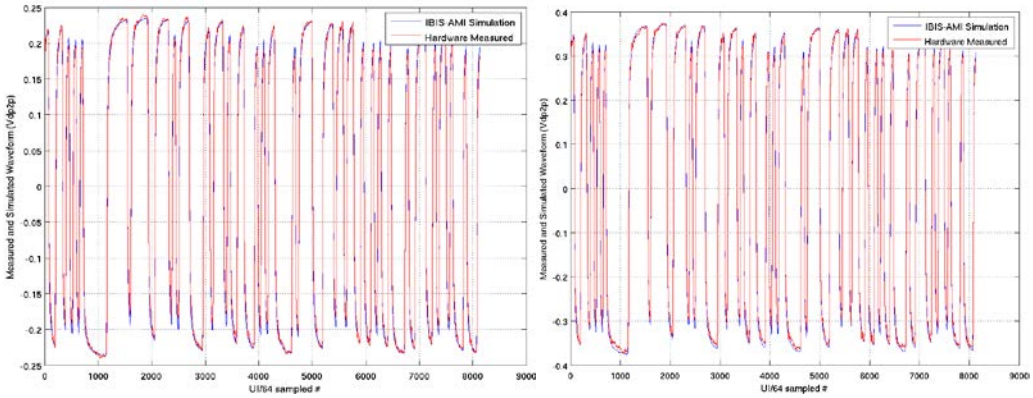

Figure 9 Transmitter Waveform Capture for (a) TXDIFFCTRL=4 (b)TXDIFFCTRL=8 at 6.6Gbps

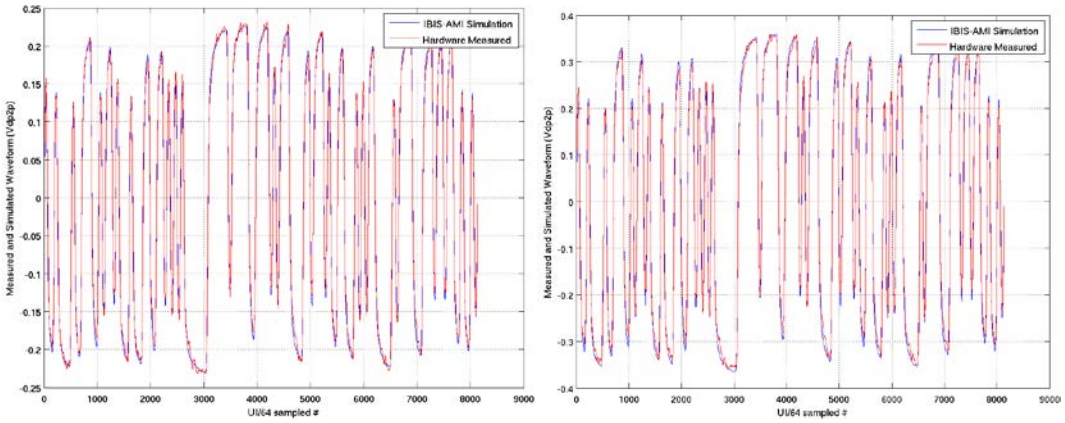

Figure 10 Transmitter Waveform Capture for (a) TXDIFFCTRL=4 (b)TXDIFFCTRL=8 at 16.3Gbps

Transmitter Distribution Correlation:

Xilinx IBIS-AMI model has 3 different PVT corner cases for both TX and RX to represent the distribution of hardware. Figure11 shows the distribution of the transmitter differential swing level at each TXDIFFCTRL setting with UltraScale GTH. The black dotted lines are from the each corner case of IBIS-AMI simulation and the colored lines are from the measurements. It shows the distribution between simulation and high volume hardware data is well matched.

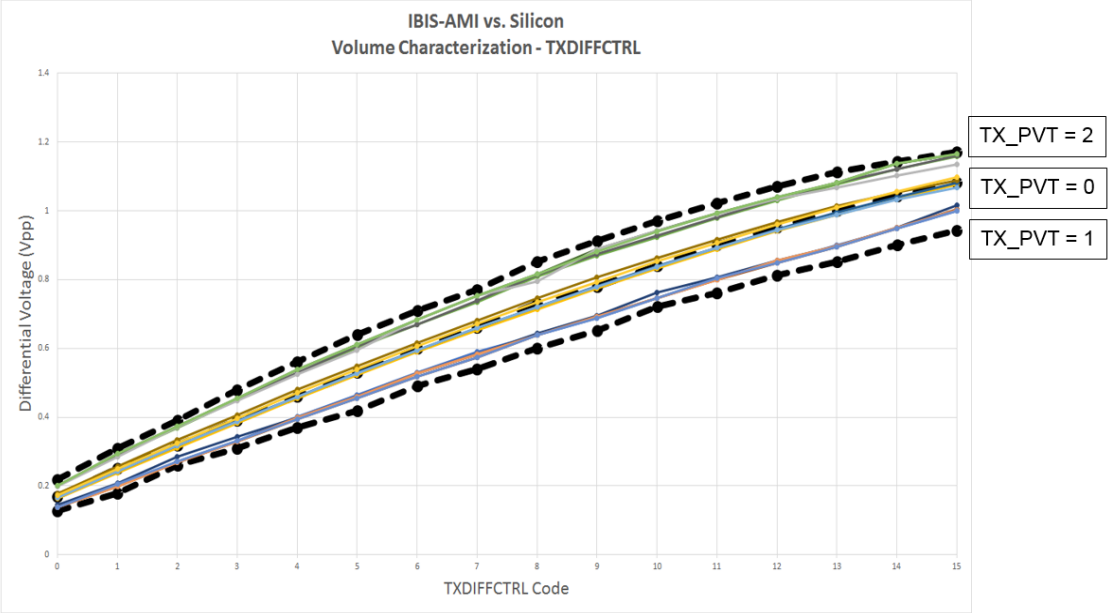

Figure 11. Distribution of Transmitter Differential Output Swing at UltraScale GTH

Figure 12 shows the distribution of the transmitter differential swing level at each TXDIFFCTRL setting in UltraScale GTY. The 3 black lines are from each PVT corner case of the simulation and colored dots represent actual measurement value at given TX DIFFCTRL setting. It shows the distribution of hardware measurements are located between boundaries set by IBIS-AMI simulation.

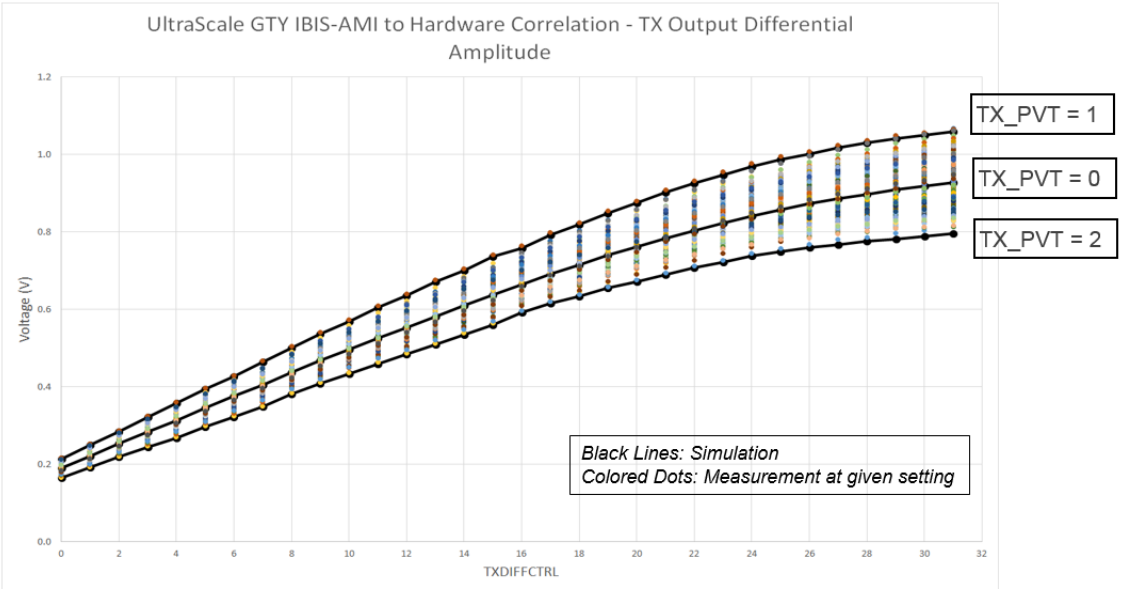

Figure 12. Distribution of Transmitter Differential Output Swing with UltraScale GTY

Figure 13 shows the distribution of de-emphasis level with UltraScale GTH transmitter by post-cursor at TXDIFFCTRL = 6 and pre-cursor at TXDIFFCTRL = 13. The de-emphasis level from IBIS-AMI simulation is located within the distribution of hardware measurement.

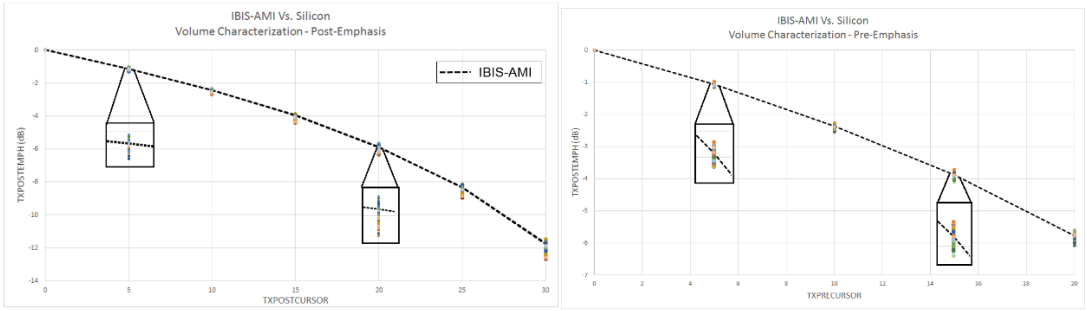

Figure 13. The distribution of de-emphasis of UltraScale GTH Transmitter by (a) Post-Cursor (b) Pre-Cursor

Figure 14 shows the distribution of de-emphasis level with UltraScale GTY transmitter by post-cursor and pre-cursor at TXDIFFCTRL = 12. The de-emphasis level from IBIS-AMI simulation is located within the distribution of hardware measurement.

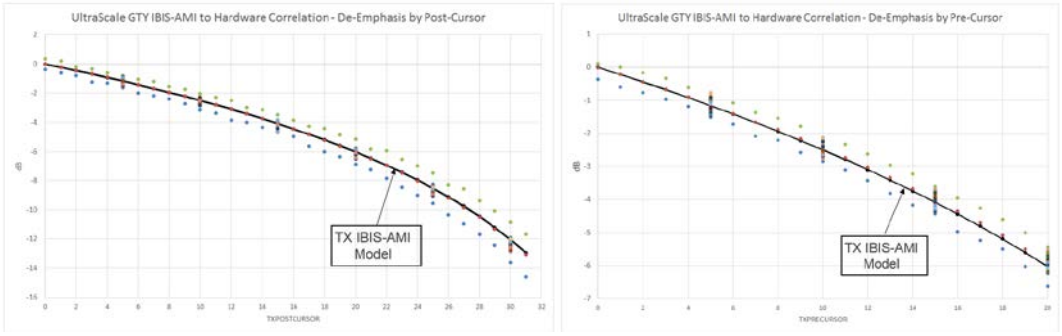

Figure 14. The distribution of de-emphasis of UltraScale GTY Transmitter by (a) Post-Cursor (b) Pre-Cursor

Receiver Correlation

Figure 15 shows the topology of channel which is being used for the receiver correlation. The different backplane has been used to give the corresponding differential loss for each test case.

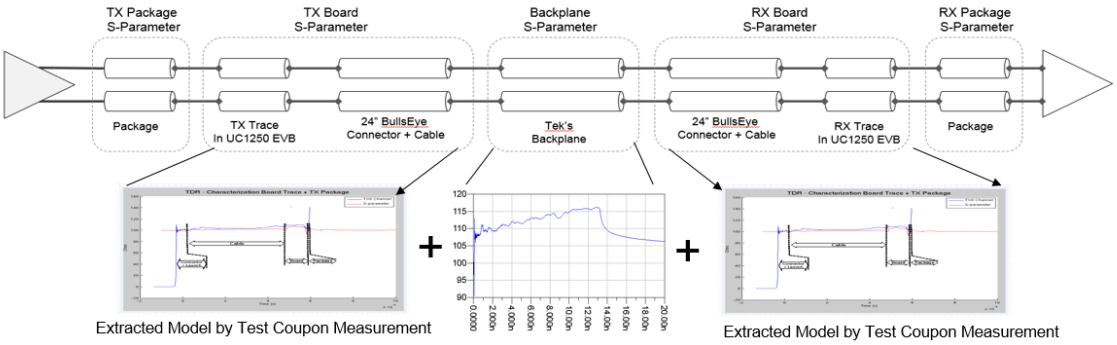

Figure 15. The channel topology for RX Test

Case1: 10G Medium Loss DFE Mode:

The differential insertion loss of the channel for the medium loss DFE is around -18dB at 5GHz. This loss includes backplane, TX evaluation board, RX evaluation board and cables.

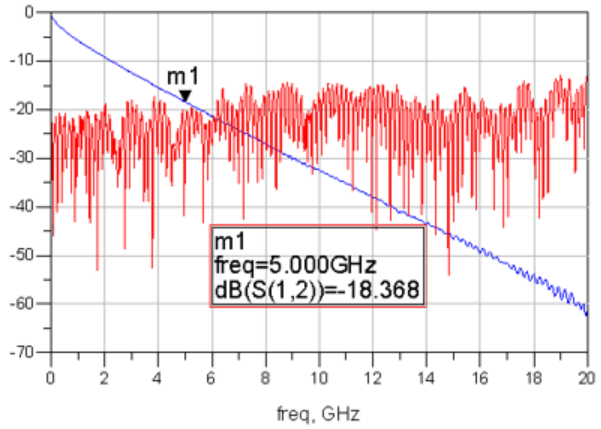

Figure 16. The differential insertion loss and return loss for medium loss at 10.3125Gbps

The non-desruptive internal 2D eye scan is performed through above channel and collected eye height and eye width in order to compare it by IBIS-AMI simulation result.

Figure 17 shows the trend analysis between typical corner case in IBIS-AMI model and typical device / typical temperature / typical voltage. The trend between simulation and hardware measurement at given condition is well matched.

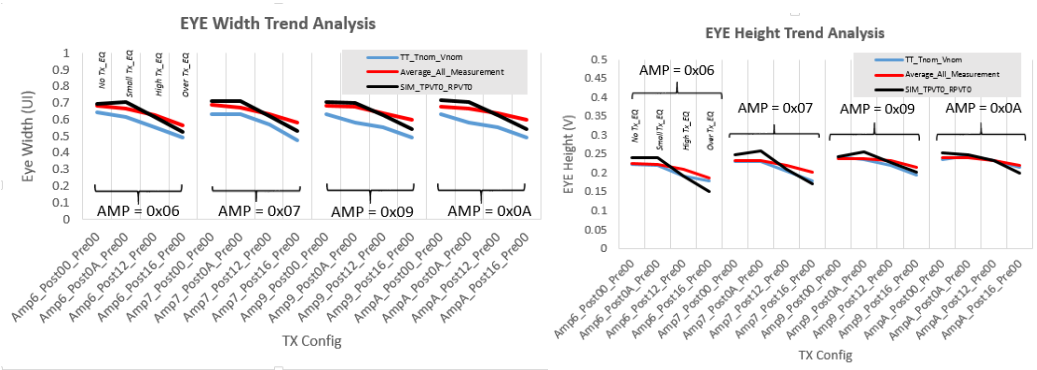

Figure 17. The trend correlation of Typical PVT case (a) Eye Width (b) Eye Height

Figure18 shows the distribution correlation of this case. . The black dotted lines represent the minimum and maximum simulation values of IBIS-AMI simulations, the solid lines represent the hardware minimum and maximum measurements across PVT. The graph shows that the IBIS-AMI transceiver models can represent very well the margin boundaries of silicon PVT variation.

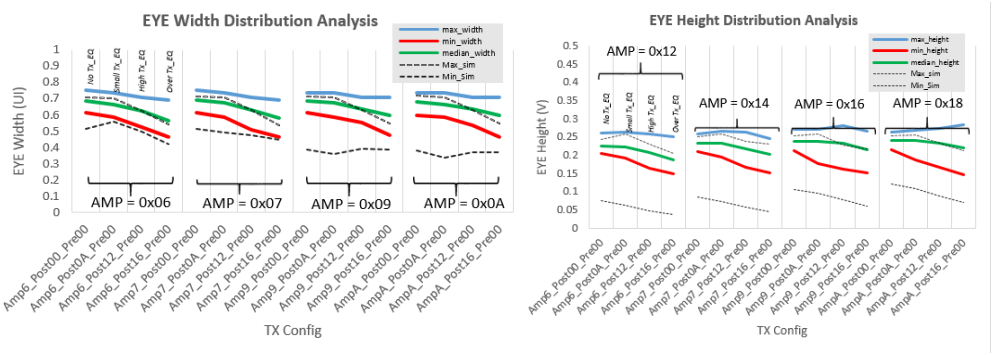

Figure 18. Distribution Correlation of medium loss DFE at 10G (a) Eye width (b) Eye Height

Figure 19 shows histogram plots that shows in more detail the receiver distribution at specific TX equalizer configuration, AMP=0x09 and POST=0x0A.

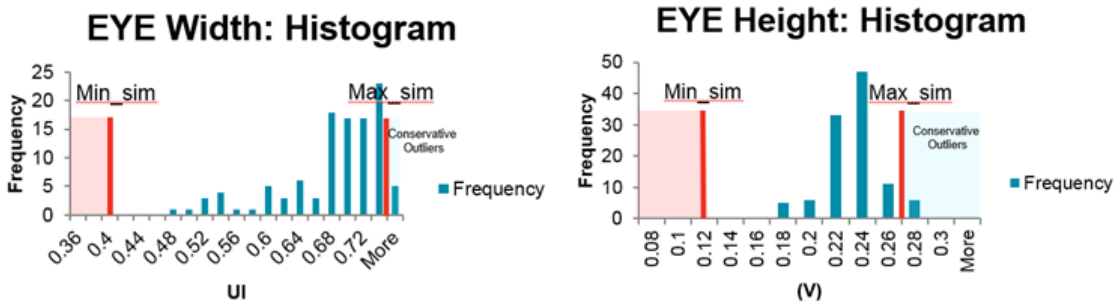

Figure 19. Spot Check at given TX equalizer setting (a) Eye Width Histogram (b) Eye Height Histogram

There can be outliers of hardware measurement which lower than “MIN_SIM” or bigger than “MAX_SIM” by the distribution of jitter or noise in real silicon. The bigger outliers bigger than “MAX_SIM” are usually acceptable because it makes the model more conservative. Figure 19 shows there is only acceptable outliers of hardware distribution which is bigger than “MAX_SIM”.

Case2: 10G High Loss DFE Mode:

The differential insertion loss of the channel for the medium loss DFE is around -24dB at 5GHz and -29dB at 6GHz. This loss includes backplane, TX evaluation board, RX evaluation board and cables.

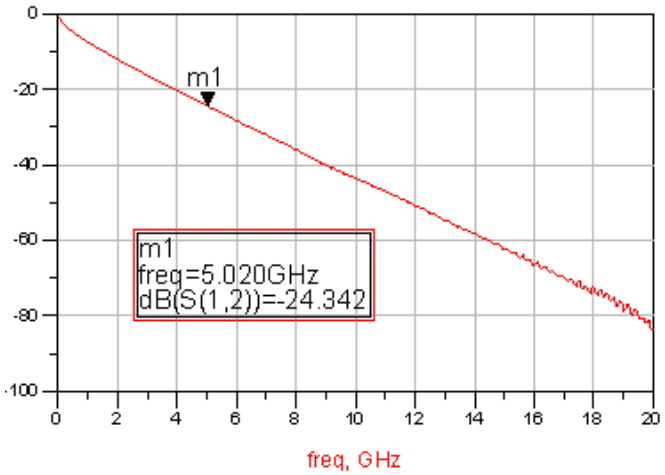

Figure 20. The differential insertion loss and return loss for medium loss at 10.3125Gbps

Figure 21 shows the trend analysis between typical corner case in IBIS-AMI model and typical device / typical temperature / typical voltage. The trend between simulation and hardware measurement at given condition is well matched.

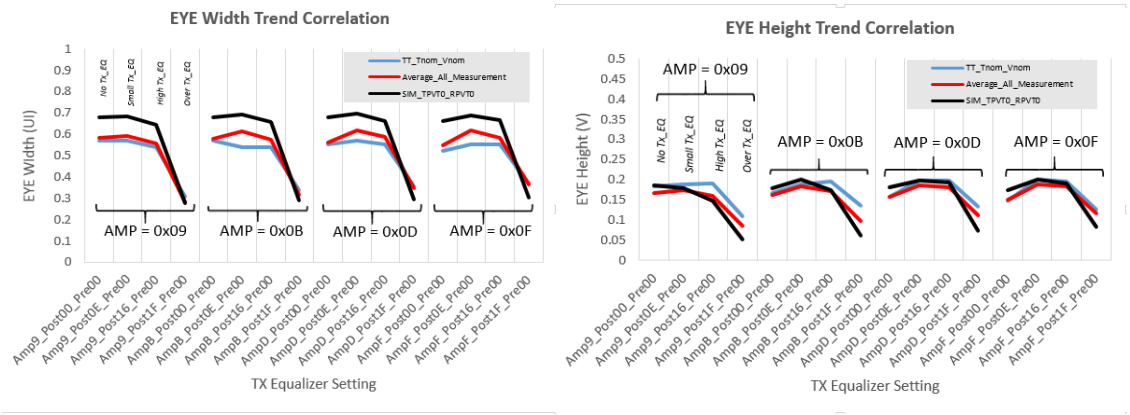

Figure 21. The trend correlation of Typical PVT case (a) Eye Width (b) Eye Height

Figure 22 shows the distribution correlation of this case. . The black dotted lines represent the minimum and maximum simulation values of IBIS-AMI simulations, the solid lines represent the hardware minimum and maximum measurements across PVT. The graph shows that the IBIS-AMI transceiver models can represent well the margin boundaries of silicon PVT variation. There are little bad outliers which is smaller than “MIN_SIM” at few TX equalizer settings, but it is small distribution compared to overall distribution. This bad outliers may be caused by the jitter and noise distribution of real silicon parts across PVT.

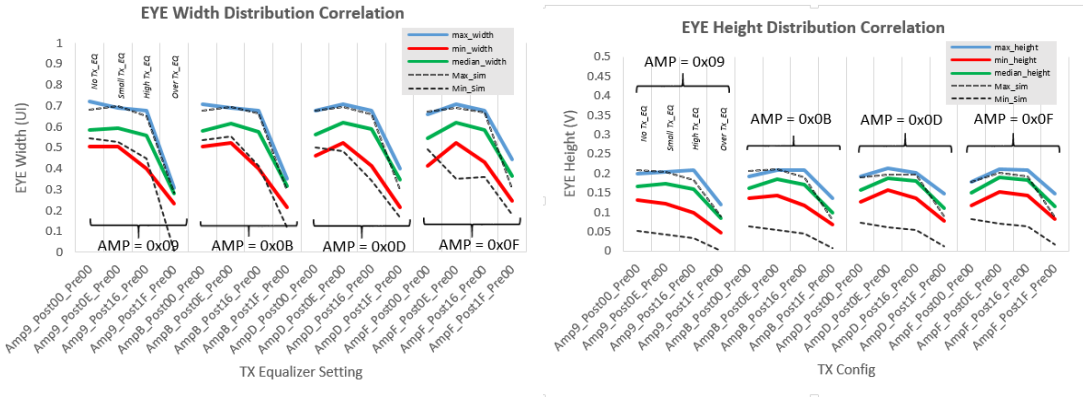

Figure 22. Distribution Correlation of high loss DFE at 10G (a) Eye width (b) Eye Height

Figure 23 shows histogram plots that shows in more detail the receiver distribution at specific TX equalizer configuration, AMP=0x0F and POST=0x0E.

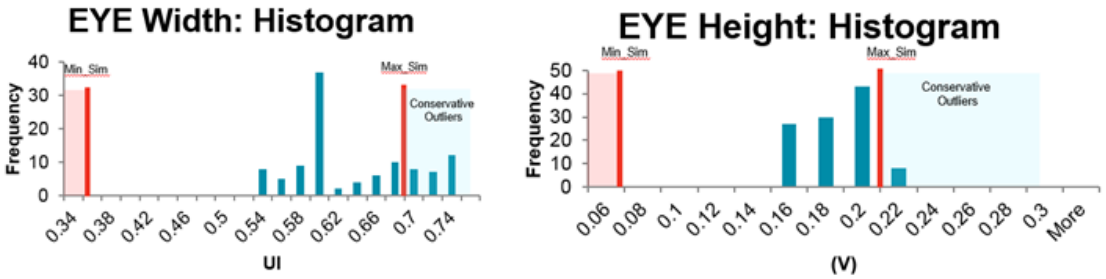

Figure 23. Spot Check at given TX equalizer setting (a) Eye Width Histogram (b) Eye Height Histogram

There can be outliers of hardware measurement which lower than “MIN_SIM” or bigger than “MAX_SIM” by the distribution of jitter or noise in real silicon. The bigger outliers bigger than “MAX_SIM” are usually acceptable because it makes the model more conservative. Figure 23 shows there is only acceptable outliers of hardware distribution which is bigger than “MAX_SIM”.

Case3: 16.3G Med Loss DFE Mode:

The differential insertion loss of the channel for the medium loss DFE is around -19dB at 8GHz. This loss includes backplane, TX evaluation board, RX evaluation board and cables.

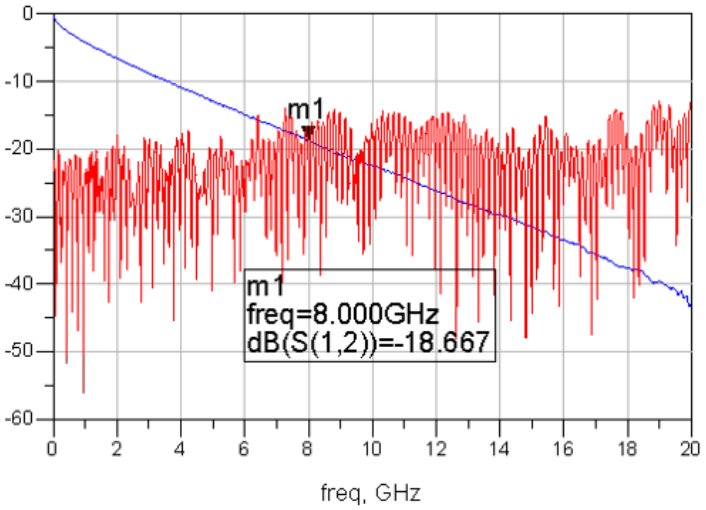

Figure 24. The differential insertion loss and return loss for medium loss at 16.325Gbps

Figure 25 shows the trend analysis between typical corner case in IBIS-AMI model and typical device / typical temperature / typical voltage. The trend between simulation and hardware measurement at given condition is well matched.

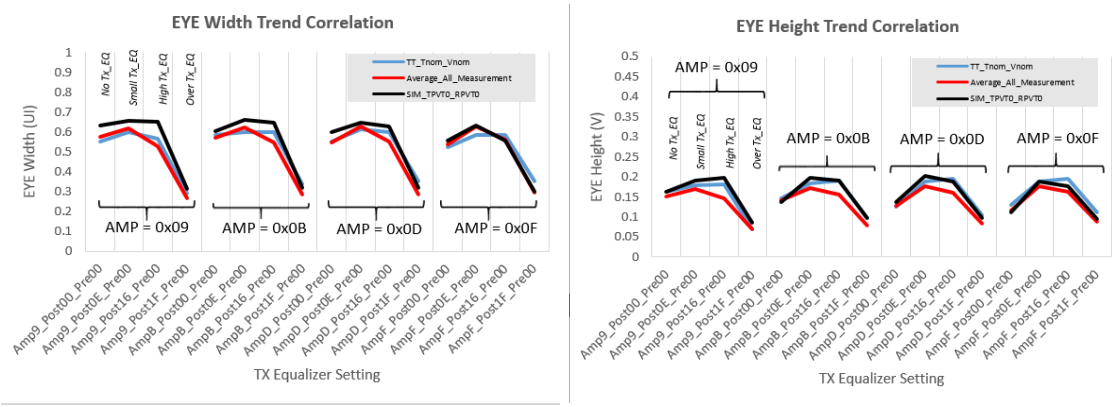

Figure 25. The trend correlation of Typical PVT case (a) Eye Width (b) Eye Height

Figure 26 shows the distribution correlation of this case. . The black dotted lines represent the minimum and maximum simulation values of IBIS-AMI simulations, the solid lines represent the hardware minimum and maximum measurements across PVT. The graph shows that the IBIS-AMI transceiver models can represent very well the margin boundaries of silicon PVT variation.

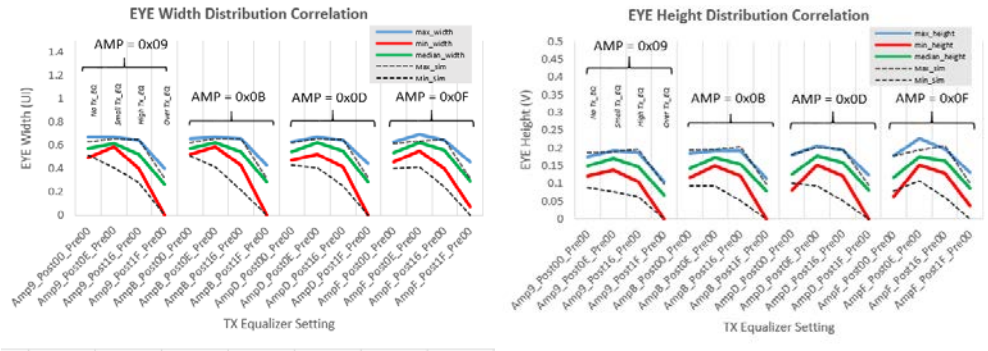

Figure 26. Distribution Correlation of medium loss DFE at 16G (a) Eye width (b) Eye Height

Figure 23 shows histogram plots that shows in more detail the receiver distribution at specific TX equalizer configuration, AMP=0x0F and POST=0x0E.

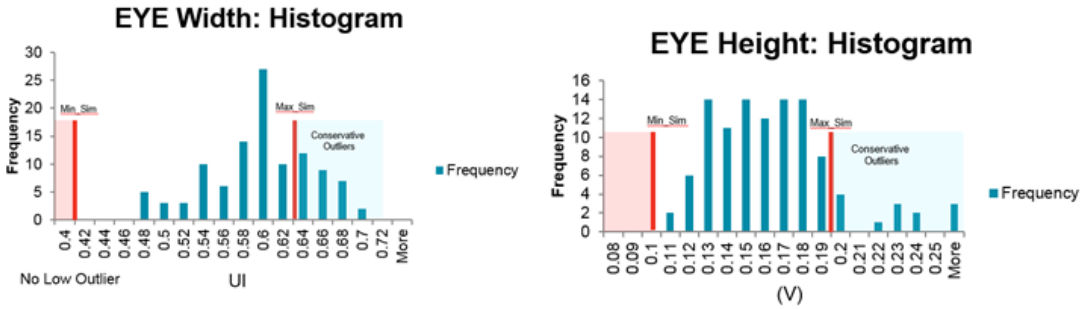

Figure 27. Spot Check at given TX equalizer setting (a) Eye Width Histogram (b) Eye Height Histogram

There can be outliers of hardware measurement which lower than “MIN_SIM” or bigger than “MAX_SIM” by the distribution of jitter or noise in real silicon. The bigger outliers bigger than “MAX_SIM” are usually acceptable because it makes the model more conservative. Figure 23 shows there is only acceptable outliers of hardware distribution which is bigger than “MAX_SIM”.

Case4: 16.3G High Loss DFE Mode:

The differential insertion loss of the channel for the medium loss DFE is around -23dB at 8GHz. This loss includes backplane, TX evaluation board, RX evaluation board and cables.

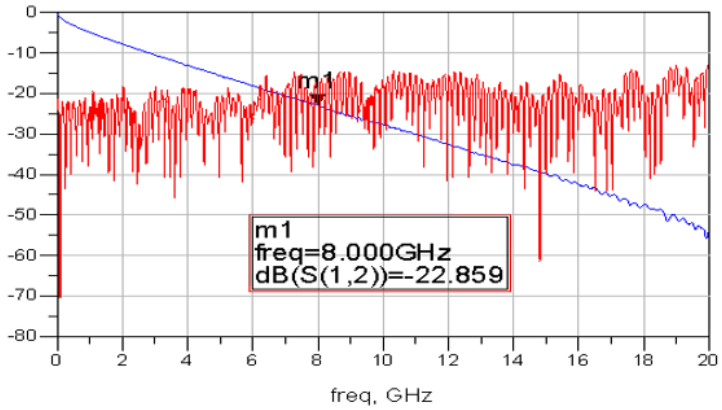

Figure 28. The differential insertion loss and return loss for medium loss at 16.325Gbps

Figure 29 shows the trend analysis between typical corner case in IBIS-AMI model and typical device / typical temperature / typical voltage. The trend between simulation and hardware measurement at given condition is well matched.

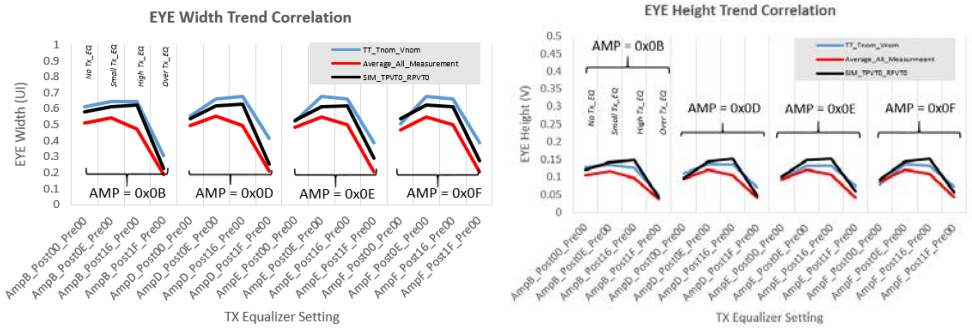

Figure 29. The trend correlation of Typical PVT case (a) Eye Width (b) Eye Height

Figure 30 shows the distribution correlation of this case. . The black dotted lines represent the minimum and maximum simulation values of IBIS-AMI simulations, the solid lines represent the hardware minimum and maximum measurements across PVT. The graph shows that the IBIS-AMI transceiver models can represent very well the margin boundaries of silicon PVT variation.

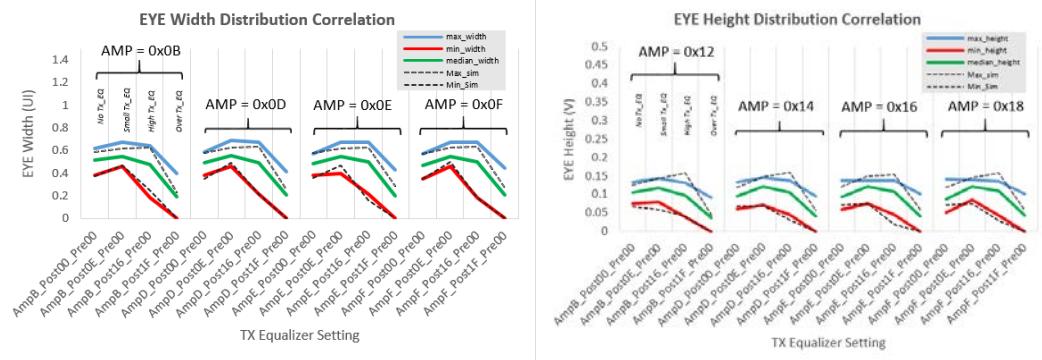

Figure 30. Distribution Correlation of high loss DFE at 16G (a) Eye width (b) Eye Height

Figure 31 shows histogram plots that shows in more detail the receiver distribution at specific TX equalizer configuration, AMP=0x0F and POST=0x0E.

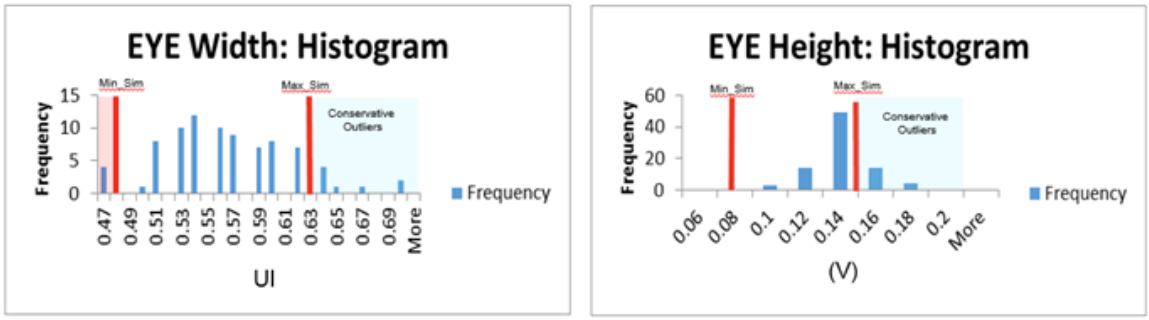

Figure 31. Spot Check at given TX equalizer setting (a) Eye Width Histogram (b) Eye Height Histogram

There can be outliers of hardware measurement which lower than “MIN_SIM” or bigger than “MAX_SIM” by the distribution of jitter or noise in real silicon. The bigger outliers bigger than “MAX_SIM” are usually acceptable because it makes the model more conservative. Figure 31 shows there is only acceptable outliers of hardware distribution which is bigger than “MAX_SIM”.

Case5: 28G High Loss DFE Mode:

The differential insertion loss of the channel for the medium loss DFE is around -29dB at 14GHz. This loss includes backplane, TX evaluation board, RX evaluation board and cables.

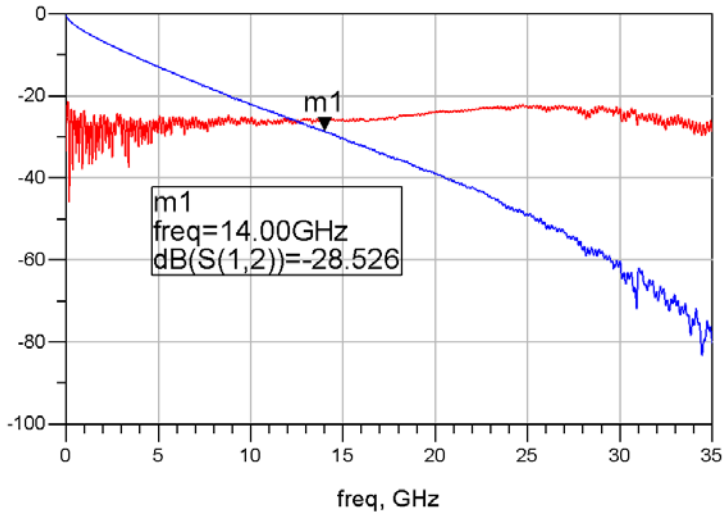

Figure 32. The differential insertion loss and return loss for medium loss at 14GHz

Figure 33 shows the trend analysis between typical corner case in IBIS-AMI model and typical device / typical temperature / typical voltage. The trend between simulation and hardware measurement at given condition is well matched.

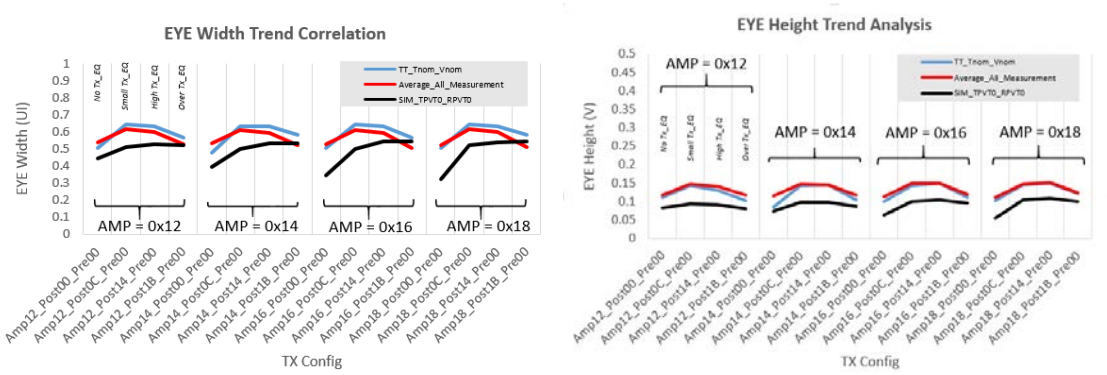

Figure 33. The trend correlation of Typical PVT case (a) Eye Width (b) Eye Height

Figure 34 shows the distribution correlation of this case. . The black dotted lines represent the minimum and maximum simulation values of IBIS-AMI simulations, the solid lines represent the hardware minimum and maximum measurements across PVT. The graph shows that the IBIS-AMI transceiver models can represent very well the margin boundaries of silicon PVT variation.

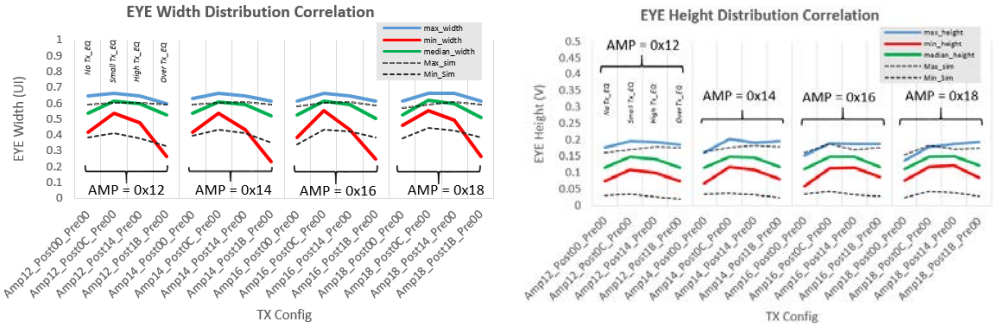

Figure 34. Distribution Correlation of high loss DFE at 16G (a) Eye width (b) Eye Height

Conclusion

In this paper we proposed a new methodology for the correlation between IBIS-AMI simulation and real hardware in order to design the high speed SerDes links up to 28Gbps. This new methodology includes the trend and distribution correlation and the correlated IBIS-AMI model can give more confidence for the designed link with IBIS-AMI simulation. We applied this methodology to Xilinx UltraScale GTH and GTY device at 10.3125Gbps, 16.325Gbps and 28.0Gbps and showed the trends are matched well and the distributions of real circuits are described well by IBIS-AMI simulations.

The proposed methodology can contribute to achieving better design process of high speed link using SerDes up to 28Gbps with IBIS-AMI model which is replacing SPICE simulation.[5][6]

Reference

[1] Xilinx, UltraScale GTH Userguide
[2] Xilinx, UltraScale GTY Userguide
[3] Xilinx, UltraScale GTH IBIS-AMI Userguide
[4] Xilinx, UltraScale GTY IBIS-AMI Userguide
[5] Michael Steinberger, Todd Westerhoff and Christopher White, “Demonstration of SerDes Modeling using the Algorithmic Model Interface (AMI) Standard,” Designcon 2008.
[6] Anil Lingambudi, Greg Edlund, Anand Haridass and Dale Becker “A Case Study of High-Speed Serial Interface Simulation With IBIS-AMI Models,” IEEE EDPAS 2012, pp. 145-148.
[7] Seungyong Baek, Amendra Koul and Mike Sapozhnikov, “Effective Methodology for Correlation Measurement to Simulation for IBIS-AMI Models.” EMCSI 2015