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25G Long Reach Cable Link System Equalization Optimization

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Abstract

CTLE in various standards, both IEEE and OIF, has been proposed as a high frequency peaking filter, whose peaking location is placed around the Nyquist frequency of the data rate. Cable channels are different from PCB backplane channels in terms of insertion loss profiles, due to different contributions from dielectric loss and skin-effect loss. An addition of a mid-frequency CTLE could noticeably reduce channel ISI at data slicers, mitigating the burden on DFE, and enhancing link margin.

Both theoretical analysis and silicon model simulation of cable channels are provided in this paper, together with lab measurements. The results are compared with IEEE P802.3bj CR4 standards to show that DFE taps are more reasonably distributed when a mid-frequency CTLE stage is included.

Authors Biography

Yu Liao received his Ph.D. in 2005 in Electrical Engineering from University of Minnesota, Twin Cities. He joined Xilinx in 2014 as SerDes architect, SerDes Technology Group. Prior to joining Xilinx he has employment experiences with LSI, STMicroelectronics, and Agere. His current interest is in signal processing, FEC, and system architecture for high speed SerDes applications.

Echo Ma received her master's degree in measurement and control technology and instrument from Chongqing University, China, in 2012. She joined Luxshare-ICT as a SI engineer. Prior to joining Luxshare-ICT, she worked for O-net Communications and Source Photonics. Her current interest is in signal integrity analysis and simulation of passive interconnect products.

Jinhua Chen received his Ph.D. in 1996 in experimental nuclear physics from University of Massachusetts, Lowell. Currently, Jinhua holds the role of senior director at Luxshare-ICT. He has over 20 years of experience in electronic hardware research and development, with proven technical, managerial and leadership experience in engineering and consulting services. Prior to joining Luxshare-ICT, Jinhua held different roles in TE Connectivity, EMC Corp, and North East Systems Associates.

Geoff Zhang received his Ph.D. in 1997 in microwave engineering and signal processing from Iowa State University, Ames, Iowa. He joined Xilinx Inc. in 2013 as director of architecture and modeling in the SerDes Technology Group. Prior to joining Xilinx he has employment experiences with HiSilicon, Huawei Technologies, LSI, Agere Systems, Lucent Technologies, and Texas Instruments. His current interest is in transceiver architecture modeling and system level end-to-end simulation, both electrical and optical.

1. Introduction

CTLE in various standards, both IEEE and OIF, has been proposed as a high-frequency peaking filter, whose peaking location is placed around the Nyquist frequency for the intended data rate. For example, in COM (channel operating margin) a Nyquist peaking filter is proposed for channel margin computation as will be discussed more in details in later sections. Usually, for wide data rate range applications the CTLE needs to compromise its optimal peaking frequency locations.

Cable channels are different from PCB backplane channels in terms of insertion loss profiles, due to differently weighted contributions from dielectric loss and skin-effect loss. In general, skin-effect loss is proportional to the square root of frequency, while dielectric loss is directly proportional to frequency. At low and mid band frequencies skin-effect loss dominates while at high frequencies dielectric loss takes over. The demarcation frequency for a cable channel is higher than that for a PCB backplane channel.

The problem with the high-frequency peaking only filter is that the "long-tail" effect may not be handled effectively. As it will be shown in this paper an addition of a mid-frequency CTLE could noticeably reduce channel ISI at the data slicer, mitigating the burden on DFE while at the same time improving link margin.

Both theoretical analysis and silicon model simulation of a cable channel are provided, together with some lab data targeting IEEE P802.3bj CR4 standards. Simulations, based on a 20nm 28G-LR SerDes IP, are compared with COM computations. As COM only has the high-frequency peaking CTLE (HFCTLE) stage, its result tends to be more pessimistic than the silicon used for the evaluation, which has the additional mid-frequency CTLE (MFCTLE) stage.

In Section 2 channel loss mechanisms are discussed. High speed link basics can be found in [1-3]. Channel equalization is briefly covered in Section 3. COM is used in Section 4 as the performance bench mark. NFCTLE is introduced in Section 5. In Sections 6 and 7 cable link simulations and lab setup and measurements are presented and observation discussed.

2. High Speed Channel Loss Mechanisms

As mentioned above, the characteristics of insertion loss of a cable channel are different from that of a PCB backplane. The difference calls for an improved equalization design to optimize the link performance. In this section, we take a brief look at cable loss mechanisms before discussing link equalization schemes.

2.1 TwinAx Cables and Loss Mechanism

As shown in Figure 1, the TwinAx differential cables are bundled by the metal braid and the jacket. There are three types of shielded TwinAx (Twin Axial) differential cables: (1) TwinAx cable with two drain wires, (2) TwinAx cable with one drain wire, and (3) TwinAx cable with copper foil. They are shown in Figure 2 through Figure 4.

Different cable structures present different challenges for cable assembly manufacturing, which in turn impact cable performance. The pros and cons are summarized in Table 1. It is noted that although the TwinAx differential cable with copper foil has the best high frequency performance,

the performance could be worse if the copper foil is not in good contact with the ground; this potentially could cause production issues. Hence, the TwinAx differential cable with two drain wires is used for performance analysis in this paper.

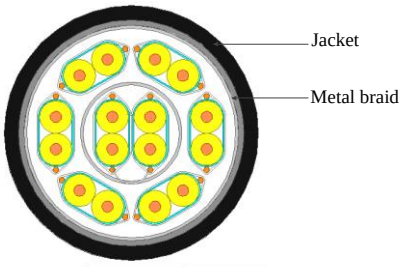


Figure 1. TwinAx differential cables covered by metal braid and jacket

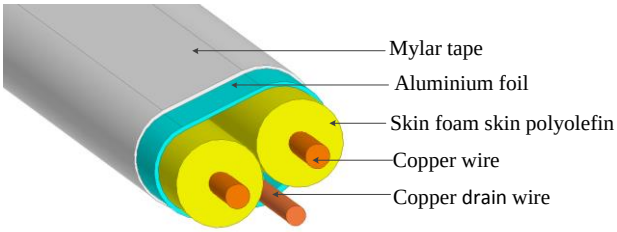


Figure 3. TwinAx differential Cable with one drain wire

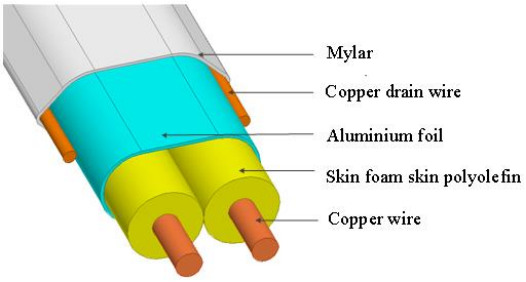


Figure 2. TwinAx differential Cable with two drain wires

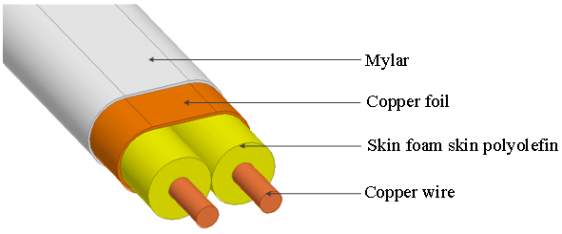


Figure 4. TwinAx differential Cable with copper foil

Table 1. Pros and cons of three types of TwinAx differential cable assemblies

TwinAx Cable Type	High Frequency Performance	Production	Cost
With two drain wires	Middle	Easy	Middle
With one drain wire	Poor	Middle	Low
With copper foil	Good	Hard	High

Channel loss is composed of two main mechanisms. First, the dielectric loss, proportional to frequency, occurs between the two metals separated by insulation material. The dielectric loss is caused by the conversion of electrical energy to other domains of energy between the two conductors in the cable, mainly as a consequence of dielectric polarization and relaxation.

Second, the skin-effect loss, proportional to the square root of frequency, is the phenomenon that the penetration depth of electromagnetic (EM) waves into a conductor is dependent on the frequency, leading to a frequency dependent series resistance and inductance. As a result, high-frequency current flows only near the skin of the conductor. The reduced EM wave penetration depth reduces the effective usable conductor area, while it also decreases the internal inductance (internal to the wire) and the magnetic field caused by this current.

The skin effect dominates at low frequencies, and dielectric loss dominates at high frequencies. This is illustrated in Figure 5. In cable channels skin effect dominance extends to a wider range than in PCB backplane channels. A crossover frequency can be estimated.

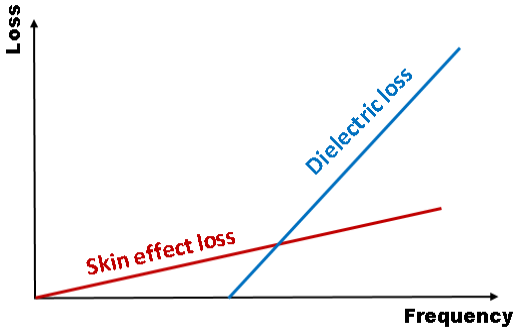


Figure 5. Channel loss at low and high frequencies

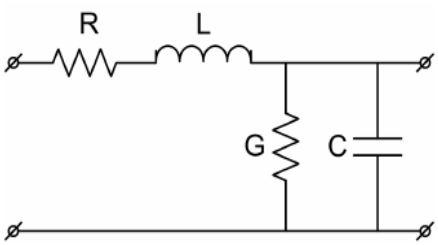


Figure 6. RLGC representation of an infinitesimally small section of TL

The TwinAx cable is one kind of the transmission line that can be modeled as shown in Figure 6. It can be derived that the complex transmission constant, $\gamma = \alpha + j\beta$, can be expressed as [4]

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{1}$$

Where R is the series resistance per unit length, L is the series inductance per unit length, C is the shunt capacitance per unit length, G is shunt conductance per unit length, and ω is the frequency in rad/s.

For ultra-low loss cables, it can be reasonably assumed that $R \ll \omega L$ and $G \ll \omega C$. Thus, by Taylor expansion approximation, γ is simplified to

$$\gamma \approx j\omega\sqrt{LC}\left[1 - \frac{j}{2}\left(\frac{R}{\omega L} + \frac{G}{\omega C}\right)\right] \tag{2}$$

The attenuation constant α and the phase constant β can be expressed as

$$\alpha \approx \frac{1}{2}\left(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}}\right) = \frac{1}{2}\left(\frac{R}{Z_0} + GZ_0\right) \tag{3}$$

$$\beta = \omega\sqrt{LC} \tag{4}$$

Where $Z_0 = \sqrt{\frac{L}{C}}$, which is the familiar lossless line characteristic impedance.

The series resistance R is given by

$$R = R_{DC} + R_{AC} \tag{5}$$

Where R_{DC} is the transmission line (TL) DC resistance. R_{AC} is the transmission line AC resistance which is caused by the skin effect loss of the conductor wire. At high frequencies, R_{AC} is much larger than R_{DC}.

The shunt conductance G is given by [5]

$$\mathrm{G} = G_{DC} + G_{AC} \tag{6}$$

Where G_{DC} is the DC shunt conductance. G_{AC} is the AC shunt conductance caused by dielectric loss. Typically, G_{DC} is much smaller than G_{AC} in the high frequency range.

The skin-effect loss and dielectric loss can be described by

$$\alpha_{Skin} = \frac{1}{2}\frac{R_{AC}}{Z_0} \tag{7}$$

$$\alpha_{Dielectric} = \frac{1}{2}G_{AC}Z_0 \tag{8}$$

2.2 Loss Decomposition for a 5M Bulk Cable

Now, the Keysight PLTS is used to extract the RLGC model for the coupled differential line from the measured S-parameter of a 5M 26AWG bulk cable. The skin-effect loss, dielectric loss and total loss calculated by the RLGC are plotted in Figure 7.

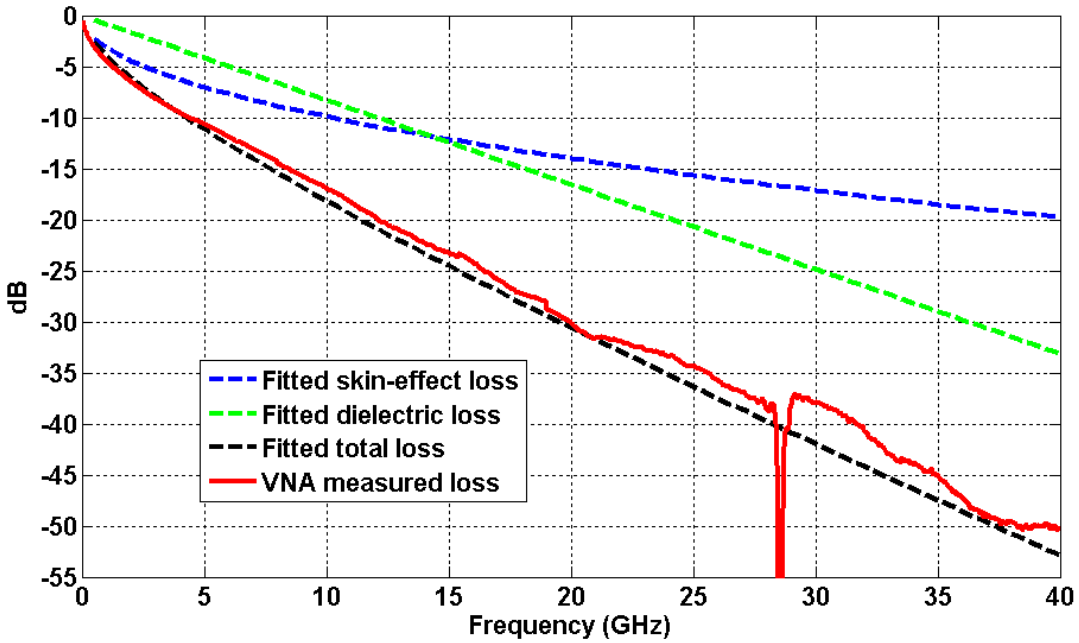


Figure 7. The 5M 26AWG cable loss decomposition

The crossover frequency, where the skin-effect loss is equal to the dielectric loss, is around 14GHz, which is much larger than the demarcation frequency for a PCB channel. This analysis showed

that the cable loss is dominated by skin-effect loss in the frequency range up to 12.9 GHz, the Nyquist frequency of CR4 data rate. For smaller gauge wires, the crossover frequency would be even higher. This posts challenges to the design of SerDes equalization, which will be discussed in later sections.

For pure PCB, the crossover frequency is much lower, as shown in Figure 8 as an example for FR4 material [6]. In this case it is below 1GHz (Note that conductor loss in the figure is equivalent to skin-effect loss in the context). The dielectric in FR4, made from glass fiber and epoxy, has much higher loss than the polyethylene or specially designed low-loss (foamed or air) dielectric in cables.

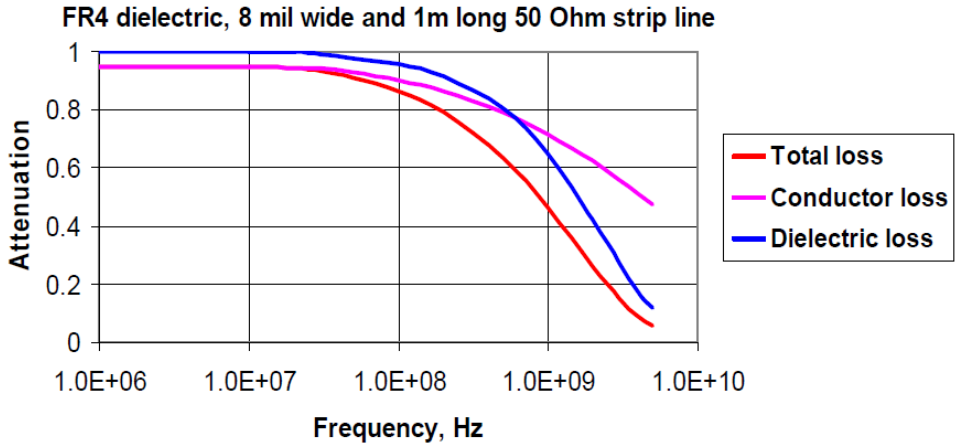


Figure 8. Pure PCB channel decomposition of skin-effect loss and dielectric loss

2.3 Measurement of a 5M Bulk Cable

Figure 9 shows the insertion loss measured from the 5M 26AWG cable. It is plotted together with a PCB backplane channel made of Megtron-6 material [7], for side-by-side comparison. The total for the bulk cable, loss includes the test fixtures as shown in Figure 10. The zoomed-in view of the insertion loss (right side of Figure 9) clearly shows the difference between the two after about 3GHz. Also note that the cable channel also has some PCB trace and connector losses.

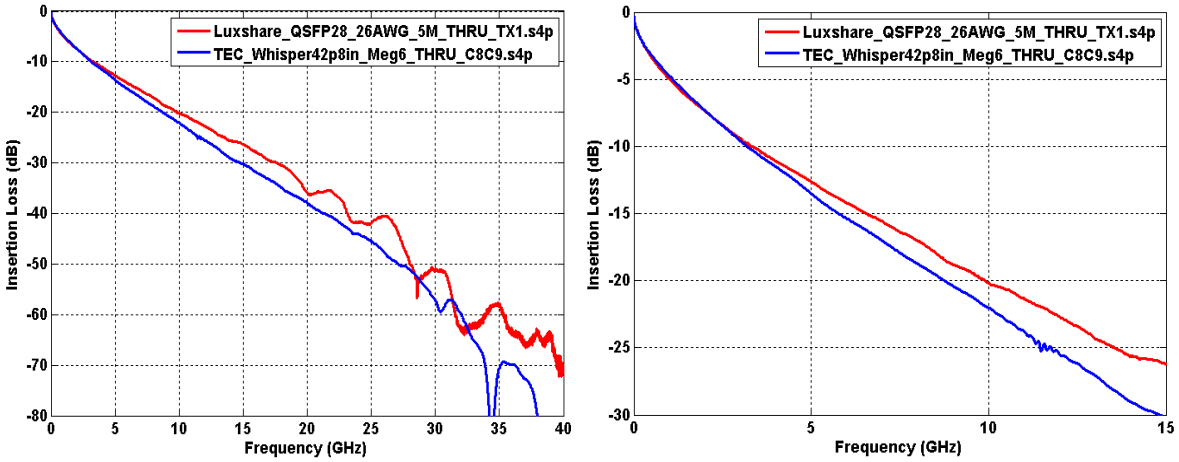
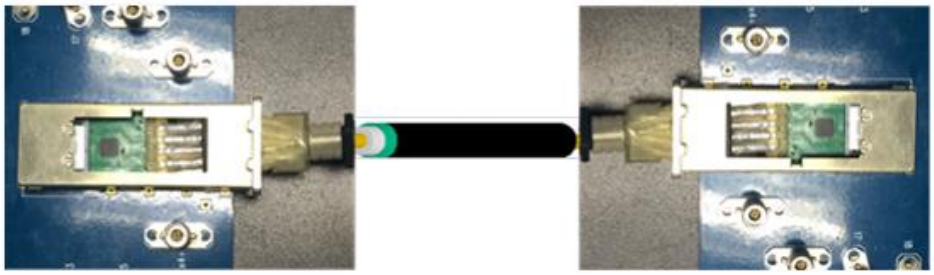


Figure 9. The 5M 26AWG cable with fixture vs. a PCB backplane channel



Paddle card PCB + connector --- Cable --- Paddle card PCB + connector

Figure 10. Test fixture for cable measurement

3. Channel Equalization Overview

The most commonly used equalization schemes, for both effectiveness in reducing ISI and efficiency in power consumption and silicon implementation, are TX side FFE, RX side CTLE and DFE. RX side FFE usually comes at a more expensive cost. At the 25G data rate node, RX side FFE is much less implemented.

A brief review of TX side FFE, RX side CTLE and DFE is given in this section.

3.1 TX FFE

TX FFE, usually implemented in FIR, is very effective in mitigating channel ISI. A commonly used 3-tap FFE (one pre cursor, one main cursor, and one post cursor) is shown in Figure 11.

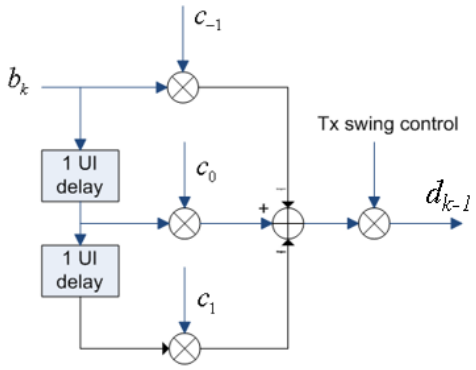


Figure 11. A 3-tap TX FIR filter

Typically, there is constraint to the three coefficients such that $C_{-1} + C_0 + C_1 = 1$, and $C_0 - C_{-1} - C_1 > 0$. This implementation is often referred as de-emphasis, as low frequency energy is attenuated. An example is provided in Figure 12 to show the TX FFE effect in equalizing the channel and opening up the eye.

The disadvantage of TX FFE includes the difficulty to make the filter coefficients adaptive. TX amplitude is constrained; too much equalization would make the signal after the channel too small, degrading SNR at RX input. Usually, some kind of RX side equalization is also needed to work together with TX side EQ. RX side equalizer parameters can be made adaptive much more easily.

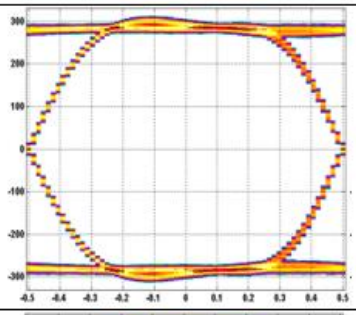
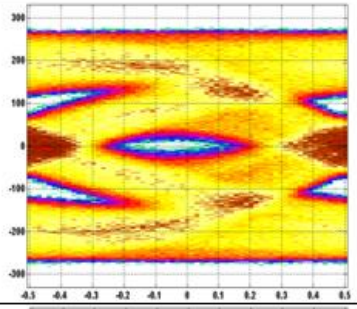
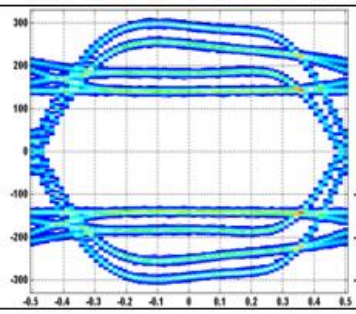
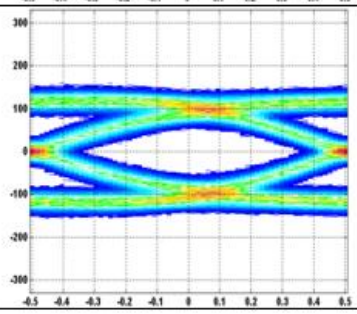
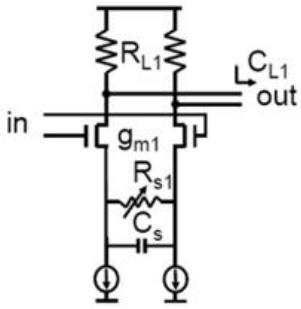
TX FFE	Eye at TX output	Eye at channel output
$\{c_{-1}, c_0, c_1\} =$ $\{0, 1, 0\}$		
$\{c_{-1}, c_0, c_1\} =$ $\{0.075, 0.75, 0.175\}$		

Figure 12. TX de-emphasis effect in opening up the eye after the channel

3.2 RX CTLE

CTLE, a.k.a. linear equalizer, filters RX input signal by either boosting high frequency content attenuated through the channel or relatively attenuating the low frequency content. It introduces zeros to offset the frequency-dependent channel loss. The CTLE is generally preceded and/or followed by an AGC circuit to bring the signal to the appropriate level to achieve adequate SNR and to not amplify the signal too much to go too much beyond the nonlinear range.

An example of high-frequency CTLE (HFCTLE) implementation is shown in Figure 13. This is a one-zero and two-pole stage. One can design zero/pole locations to achieve desired channel equalization effect. Typically, it is difficult to design enough peaking gain in one stage. In practice, multiple stages could be implemented.



$$f_z \approx -\frac{1}{2\pi R_{S1} C_S}$$

$$f_{p1} \approx -\frac{1}{2\pi R_{L1} C_{L1}}$$

$$f_{p2} \approx -\frac{1+g_{m1}R_{S1}}{2\pi R_{S1} C_S}$$

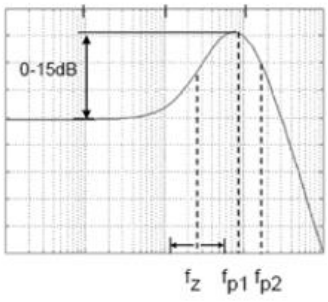


Figure 13. HFCTLE implementation

An example of CTLE effect in reducing channel ISI is illustrated in Figure 14 [8].

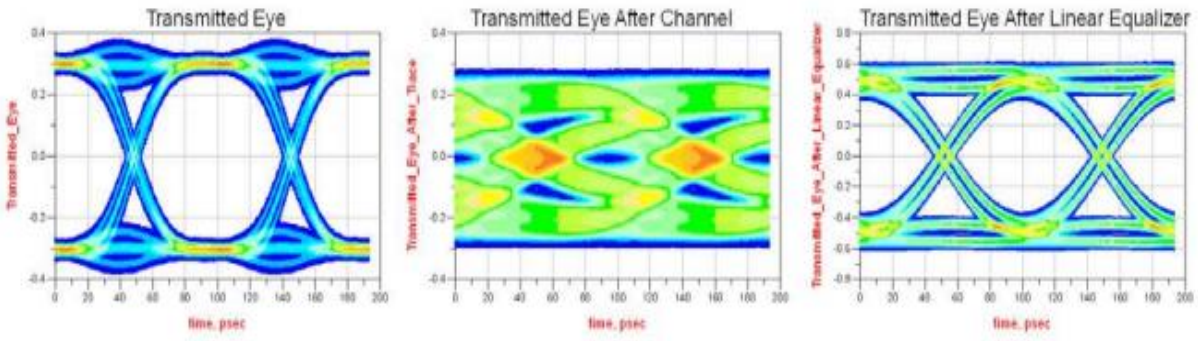


Figure 14. CTLE effect illustration

While boosting high frequency signal, CTLE could potentially amplify noise and crosstalk depending on the required CTLE/AGC settings. This calls for more precautions in using CTLE for certain applications, for example, when the environment is noisy.

3.3 RX DFE

DFE (decision feedback equalization) works by subtracting out channel impulse responses from previous data bits to zero out ISI contributions on the current bit. If the DFE has n taps, symbol spaced, then the previous n-bits induced ISI can be largely removed. The DFE working mechanism is depicted in Figure 15, although implementation-wise there are several variations.

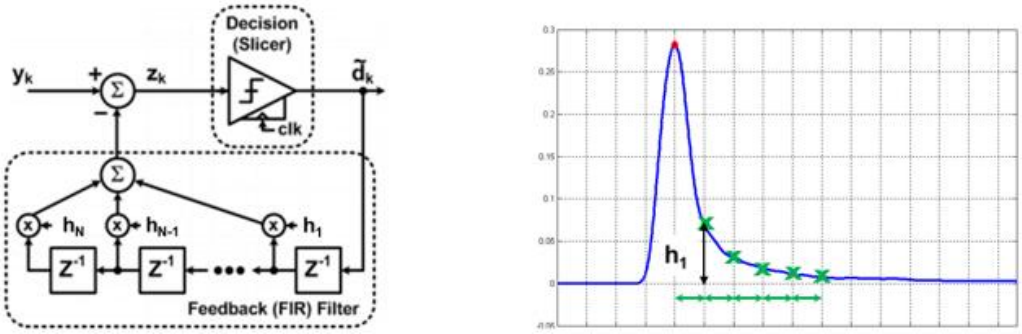


Figure 15. DFE to remove post-cursor ISI

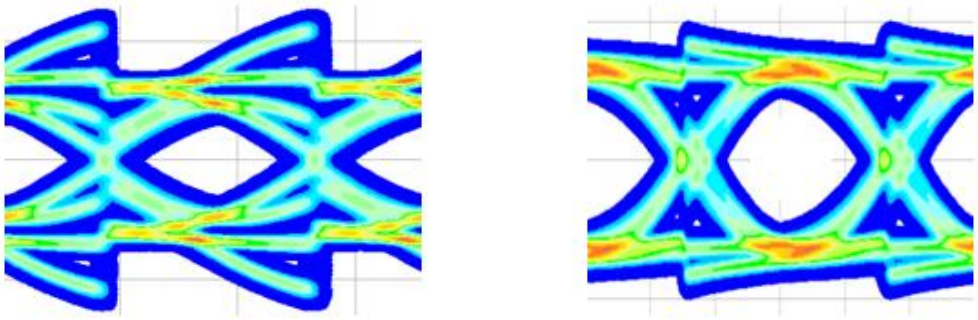


Figure 16. Typical eye diagrams after DFE summer

Figure 16 shows two typical DFE corrected data eyes. On the left is for the case when the dominant post-cursor ISI is positive, while on the right negative. The former implies the congregated equalization before DFE is not enough, or under-equalized, while the latter indicates the congregated equalization is excessive, or over-equalized.

Although DFE does not boost noise, if too much work is expected from it error propagation could become an issue in the system. On the other hand, if low to mid frequency channel equalization work is assigned to DFE, many taps are usually required to cover the "long tail".

3.4 Channel Equalization Goals

The preliminary goal of channel equalization can be perceived either in the frequency domain or in the time domain, as shown in Figure 17. Since DFE is essentially a non-linear process, its effect does not directly fit into the view.

The ultimate goal of channel equalization is to ensure that the system works within the BER target plus adequate amount of margin. In other words, the system is designed to be "good enough".

- In f-domain: to flatten the response within the frequency of interest.
- In t-domain: to remove pre- & post-cursor ISI and restrict energy.

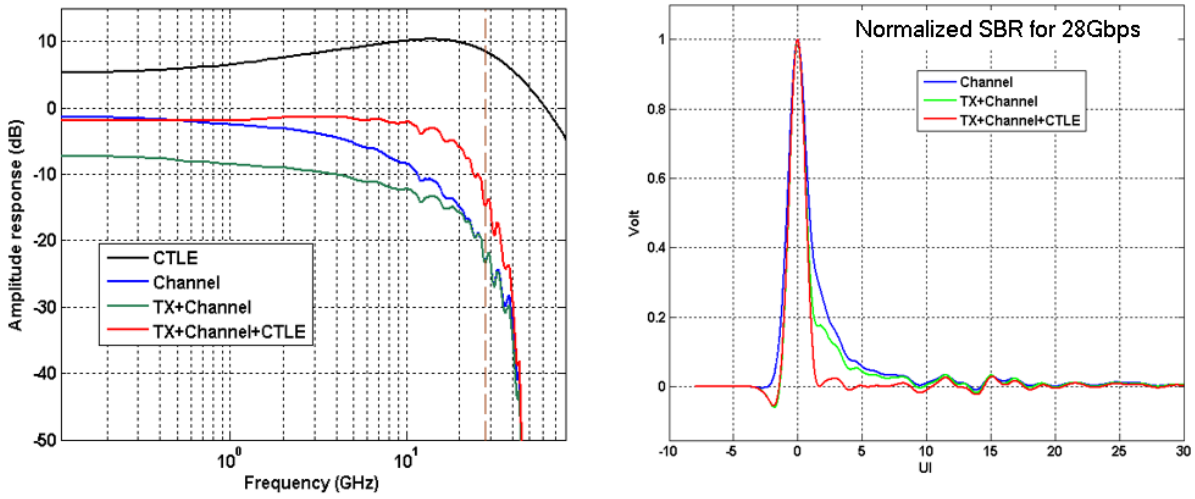


Figure 17. Illustrations of equalization purpose in frequency- and time- domain

4. Channel Operating Margin (COM) Analysis

The IEEE P802.3bj Task Force put together 100GBASE-KP4 for PAM4 signaling, 100GBASE-KR4 for NRZ, and the cabled version of the standard in NRZ, 100GBASE-CR4. COM is introduced to estimate link margin. A good tutorial on COM can be found in [9, 10].

In this section we directly use COM to analyze the cable channel performance. The COM scripts are downloaded from [11], with minor modifications. Before the computation, the cable depicted in Figure 9 is pre-cascaded with TX and RX package s-parameter models. The loss profile and crosstalk power sum are shown in Figure 18.

The channel is running at 25.78125Gbps. The changes we made from COM default settings in the file "*config_com_ieee8023_93a=100GBASE-CR4.xls*" include:

- A_v (TX differential peak output voltage, victim) = 0.5
- A_ne (TX differential peak output voltage, far-end aggressor) = 0.5
- A_fe (TX differential peak output voltage, near-end aggressor) = 0.5
- DER_0 (target detector error ratio) is set to 1E-15
- N_b (number of DFE taps) is set to either 1 or 8
- INC_PACKAGE is to set 0, since package models are already cascaded

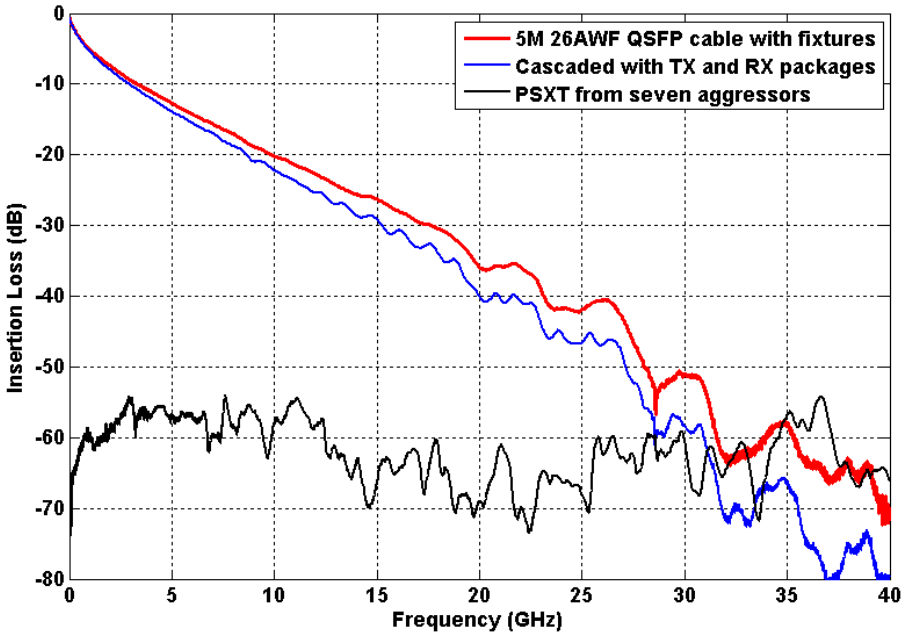


Figure 18. Cascaded cable channel and crosstalk

The prescribed CTLE in COM has the transfer function expressed in (9), where G_{DC} is DC gain in dB, suggested from 0dB to -12dB. This is a one zero and two pole system. The corresponding transfer function is plotted in Figure 19.

$$H_{CTLE}(f) = f_b \frac{j \cdot f + 0.25 \cdot f_b 10^{\frac{G_{DC}}{20}}}{(j \cdot f + 0.25 \cdot f_b) \cdot (j \cdot f + f_b)} \tag{9}$$

The insertion loss (with packages), the PSXT, ICR, and ILD, are plotted in Figure 20.

The COM computed link margin for the desired 1e-15 is summarized in Table 2. Although the computed ICN is only 0.586 mV (implying the crosstalk is moderately small), it is seen that the link cannot achieve 1e-15 with the two configurations of DFE, not to mention work with margin (as COM is negative). It is clear that the CTLE already reached the maximum peaking.

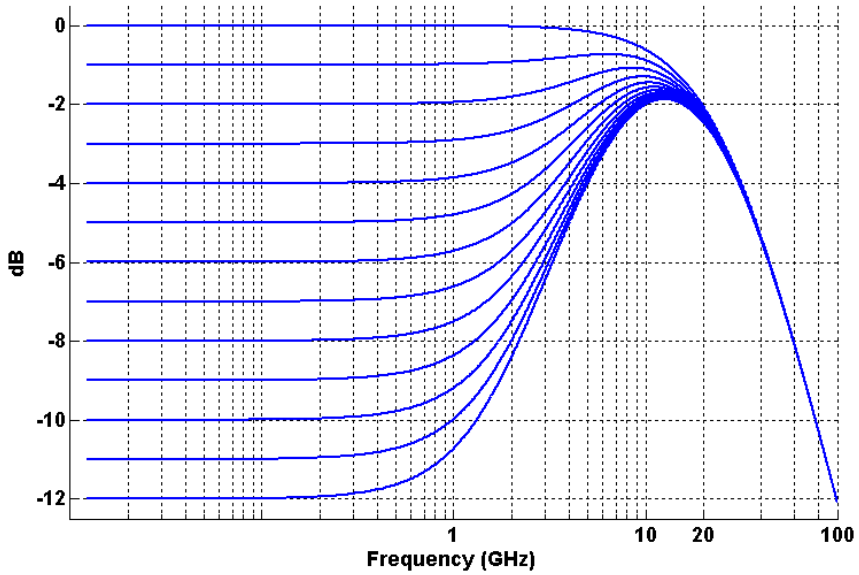


Figure 19. HFCTLE transfer function defined in COM for CR4

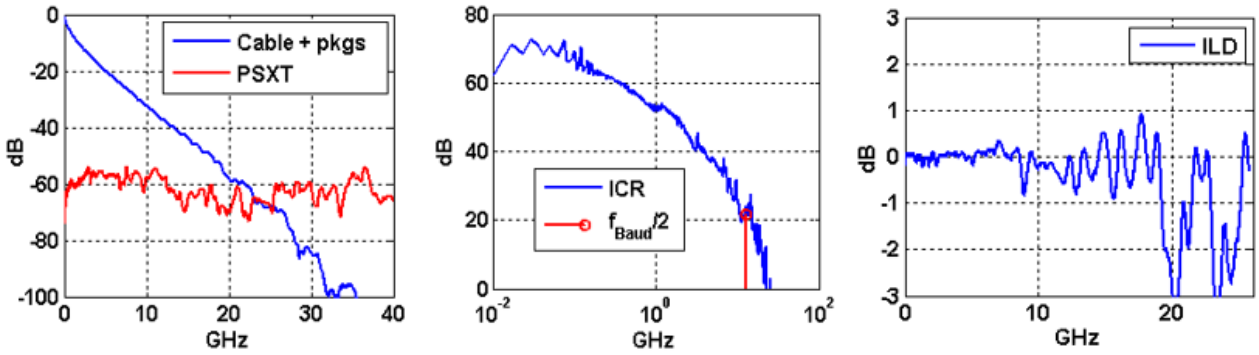


Figure 20. COM computed IL, PSXT, ICR, and ILD

Table 2. COM computed results for the QSFP cable

Input	N_b	1	8
Configured	TX FFE coefficients	[-0.14, 0.62, -0.24]	[-0.14, 0.62, -0.24]
Configured	G_{DC}	-12 dB	
Computed	COM	-2.148 dB	-0.755 dB
Estimated	BER	2.9e-10	1.8e-13

Next, we will study the improvement of CTLE design for copper cable applications by including an additional peaking stage to combat low to mid frequency ISI.

5. Optimal CTLE for Cable Channels

Traditionally, CTLE is designed to have a peaking frequency around the Nyquist frequency. However, CTLE also needs to provide sufficient boosting in low to mid frequency region to shorten and reduce the long in THRU channel impulse response such that the residual ISI at the CTLE output not covered by DFE becomes sufficiently small. In addition, CTLE design needs to consider noise and crosstalk amplification such that adequate amount of the equalization work is assigned to DFE. Thus, the partition of contributions between CTLE and DFE can be affected by the application environment. In general, over boosting near Nyquist frequency causes unnecessary noise/crosstalk enhancement, leaving little work for DFE and degrading the total link BER performance.

The CTLE used above in Equation (9) is essentially the HFCTLE, for boosting around Nyquist frequency. However, in many cases, particularly in cable channels, we also need low to mid frequency range energy boosting.

5.1 Mid-frequency CTLE - MFCTLE

Mid-frequency CTLE (MFCTLE) improves the low to mid frequency losses, by placing a pair of zero and pole closely together. In this manner, the equalizer can better approximate the gentle slope due to skin effect loss. In addition, the amount of peaking is also smaller, typically only several dB's. Reference [12] provided a good description of low frequency CTLE design (Figure 21), which is called mid frequency CTLE in this paper. MFCTLE is also referred to as long-tail cancellation CTLE viewed from the time domain perspective. The mid frequency falls in the multi-giga-Hz range for 25G applications.

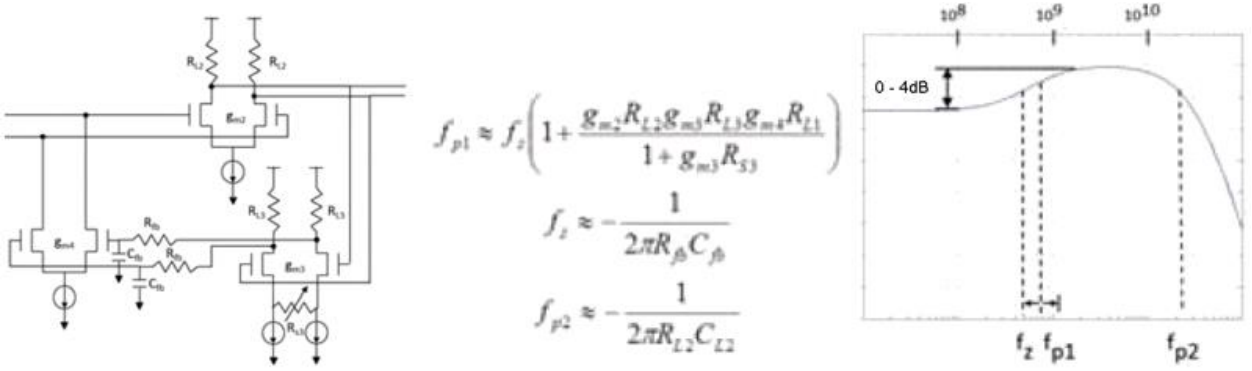


Figure 21. MFCTLE circuit and transfer functions

It is seen that mid-frequency loss has a very gentle slope. On the other hand, conventional equalizers such as HFCTLE and FIR have a 20dB/Dec slope. Thus, the match of these equalizers to the channel insertion loss profile is suboptimal. Consequently, an additional CTLE stage is needed, as will become clear through the remainder of the paper.

Another pair of zero and pole can be added to improve mid-band shaping to better match the channel response, as shown in Figure 22. The difficulty is that different frequency shaping is

required depending on loss mechanisms combined by skin-effect loss and dielectric loss. It is even more challenging to support a wider data rate range.

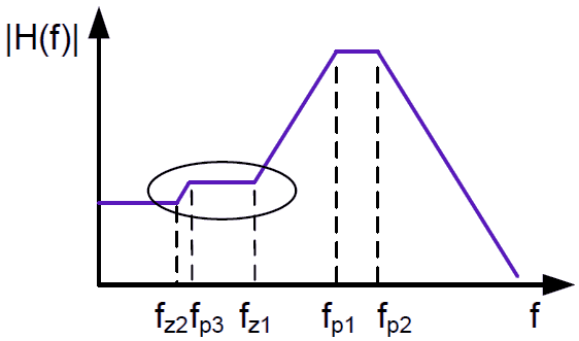
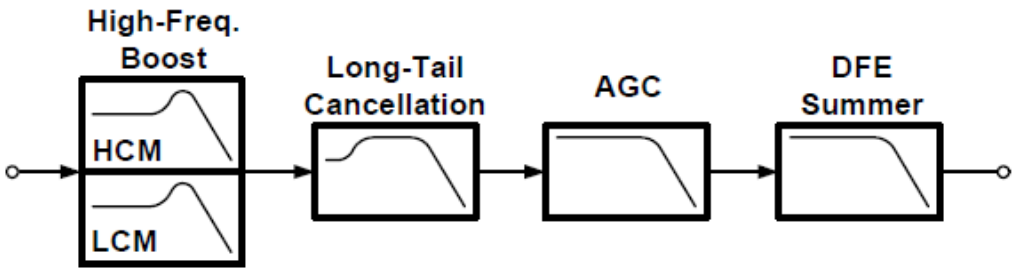


Figure 22. Multiple zero and pole MFCTLE

5.2 The Complete CTLE Block

In paper [13] a 3-stage CTLE block is described. It is duplicated in Figure 23. The CTLE block has three stages, HFCTLE, MFCTLE, and AGC. It is noted that the parameters in the table are designed for lower data rate, up to 13Gbps. For 25G applications (up to 30Gbps), we need to modify the zero and pole locations.



Stage	Zero	Pole	BW	Gain
1(HCM)	1.2GHz	2.4GHz	13.7GHz	2
1(LCM)	1.1GHz	2.4GHz	6.2GHz	1.6
2	120MHz	160MHz	10GHz	2
3	Flat		11.4GHz	2.1
4	Flat		12GHz	1

Figure 23. CTLE block and zero/pole parameters

Reference [14] has a similar proposal as highlighted in Figure 24. Since the conventional CTLE, i.e. the Nyquist frequency peaking CTLE, only concentrates around the Nyquist frequency boosting, mid frequency region is often left under equalized. This becomes more a problem when copper cable is the transmission media.

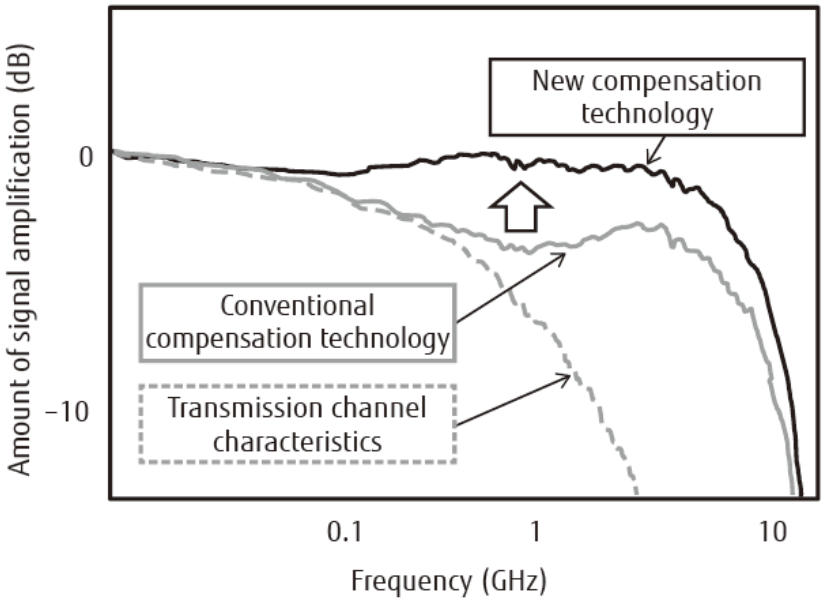
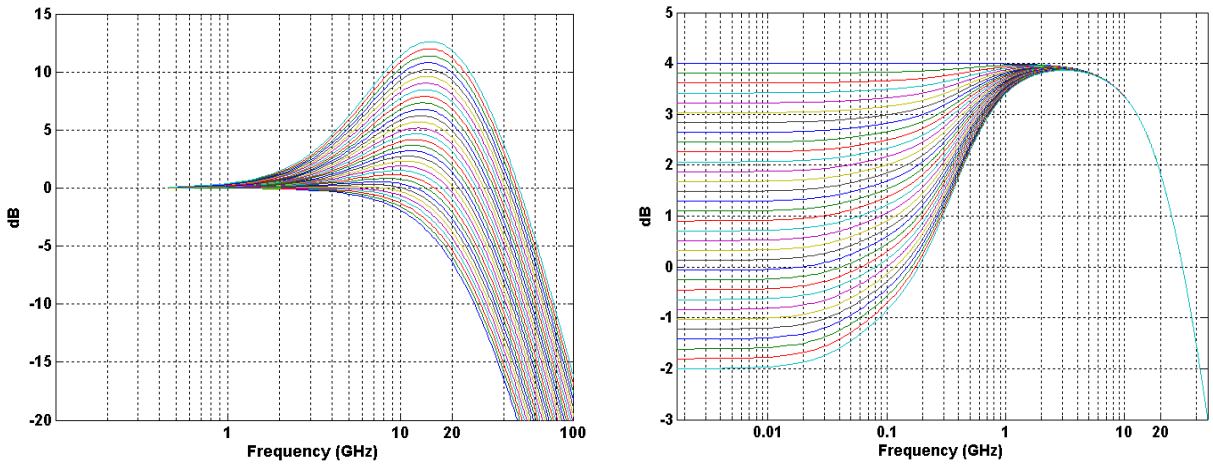


Figure 24. Illustration of the effect of mid-frequency boosting

5.3 CTLE for QSFP Cables

In this section we propose a set of transfer functions, as shown in Figure 25, for both the HFCTLE and the MFCTLE. Then we show the interaction of the CTLE with the channel in study, using the slightly modified TX FIR settings obtained from COM computations above. Each stage has nonlinearity associated with it, but until a later section in which we simulate the total link performance, we choose to ignore the nonlinear effect in this section.



(a) HFCTLE **(b) MFCTLE**

Figure 25. Proposed optimal CTLE transfer functions for QSFP cables

The proposed HFCTLE is compared with the one described in COM. The two are re-plotted for easy comparison in Figure 26. The finer steps for the proposed HF and MF CTLE are required for smooth adaptations. In addition, the proposed HFCTLE is composed of multiple cascaded stages to ease the design requirement, while the CTLE in COM is based on a single stage.

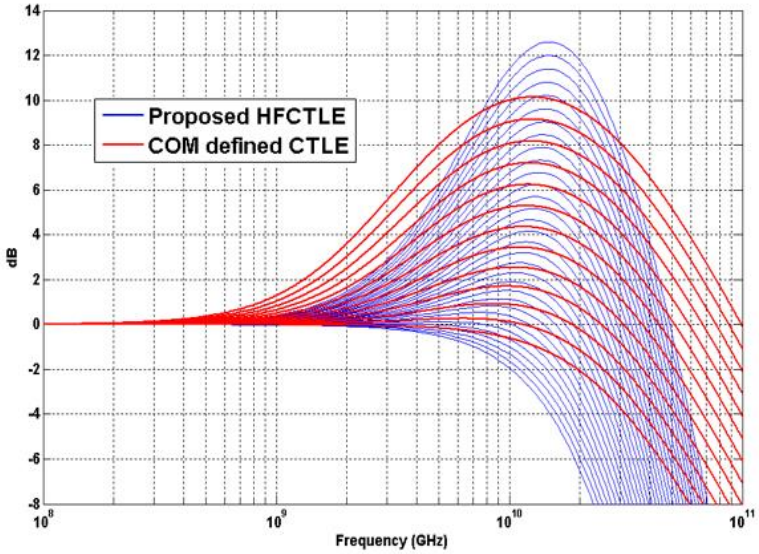


Figure 26. Comparison between the proposed HFCTLE and the CTLE from COM

5.4 Equalization Effect Analysis

We will only look at what TX FIR and CTLE can do for the cable link in the analysis in this section. We will include DFE in later sections.

5.4.1 COM CTLE Working with the Cable Channel

In Table 2 COM obtained the optimal setting for TX FFE as [-0.14, 0.62, -0.24], and for CTLE GDC as -12dB. Thus, we can apply the TX FFE and the defined CTLE to the channel consecutively to obtain the frequency domain response on the left and the normalized single bit response (SBR) on the right, in Figure 27. The DC level for the frequency response can be normalized by applying some kind of broad band gain through AGC, but it is deemed unnecessary for the purpose here.

It is seen that the computed CTLE setting actually over-equalized the channel, such that there are pretty significant amount of residual negative h(2) and h(-2) cursor ISI. This is because a single stage can hardly match the channel loss profile over a large range of frequency of interest.

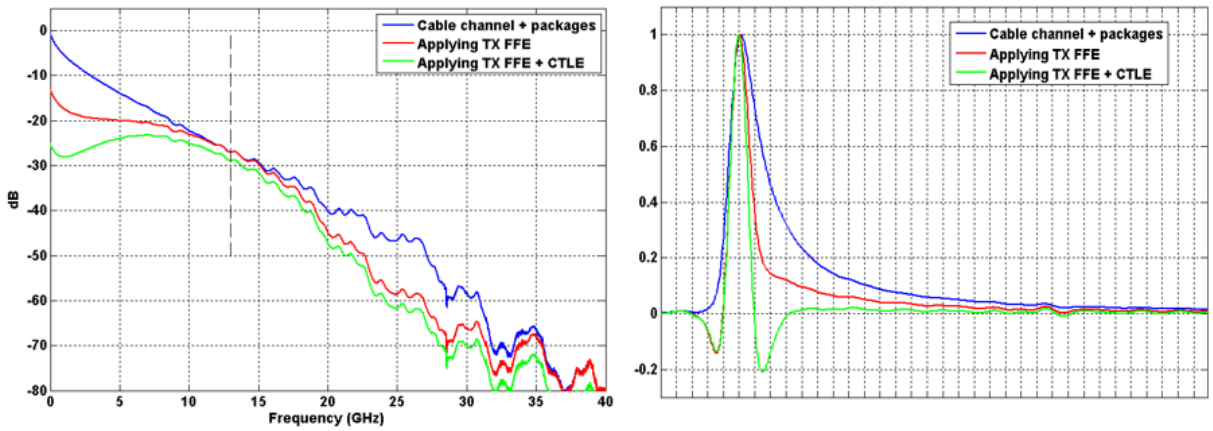


Figure 27. Frequency domain and time domain view of equalization effect

Although the equalized channel yields an open eye, as seen in Figure 28, the trace thickness above and below the eye opening indicated that there is still plenty of residual ISI, requiring more equalization of some kind. As a matter of fact, once impairments, such as jitter, noise, nonlinearity, offset, non-ideal sampling phase, and so on, are included on top of residual ISI, the eye will become much more reduced if it is still open.

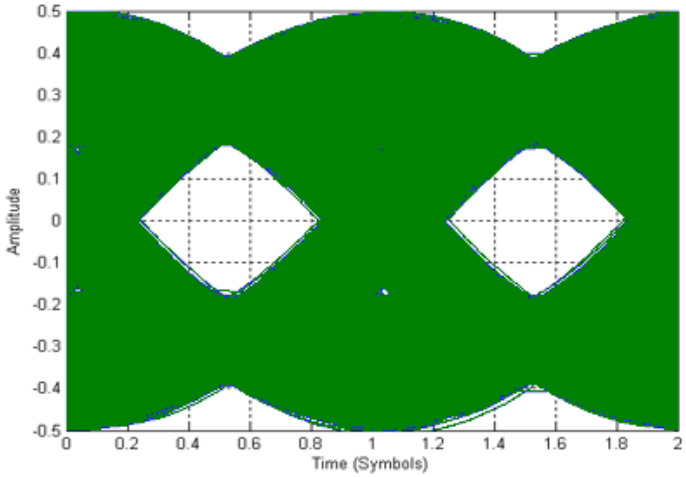


Figure 28. Eye diagram after the channel is equalized by TX FFE and COM CTLE

Next we study the performance of CTLE composed of high frequency peaking and mid frequency peaking, using the same approach.

5.4.2 Proposed CTLE Working with the Cable Channel

Now, we apply TX FFE as [-0.1375, 0.6375, -0.225], modified only slightly from the COM computed settings. There are 32 settings for both HFCTLE and MFCTLE. We select index 23 for HFCTLE and 20 for MFCTLE. The reason for picking these two settings will become clear after the next section is discussed.

We obtain the frequency domain response (left) and the SBR (right), in Figure 29. Although the green curve (after HFCTLE) and the black curve (after MFCTLE) are only different slightly, the accumulated effect can be overwhelming. In fact, since the difference is predominantly in the long tail region, the MFCTLE equalizer is sometimes also referred to as long-tail canceller.

To accomplish the same task delivered by MFCTLE, a multi-dozen-tap DFE would have been required. Floating tap DFE is one option, but not without its own issues to deal with in real life. The DFE with IIR feedback filtering has been implemented to improve equalization efficiency, but with more design complexity and adaptation challenges.

The equalized channel yields an open eye, although again without other impairments, as shown in Figure 30. It is seen that MFCTLE cleans up the eye left over from HFCTLE very nicely, hard to intuitively perceive from the responses in Figure 29. On the other hand, although the HFCTLE-only eye is smaller than that from the CTLE eye, we purposely did not select (or rather adapt to) a higher setting, considering that MFCTLE stage will also contribute to the ISI removing task.

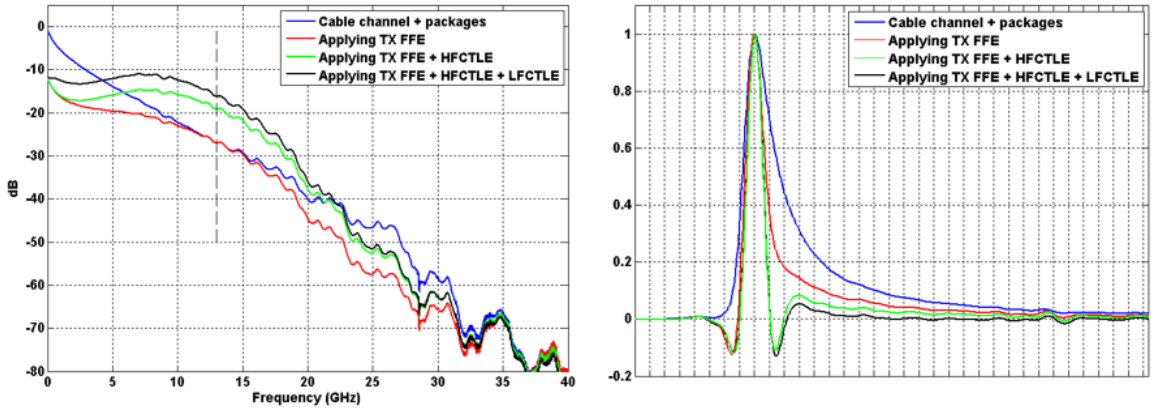
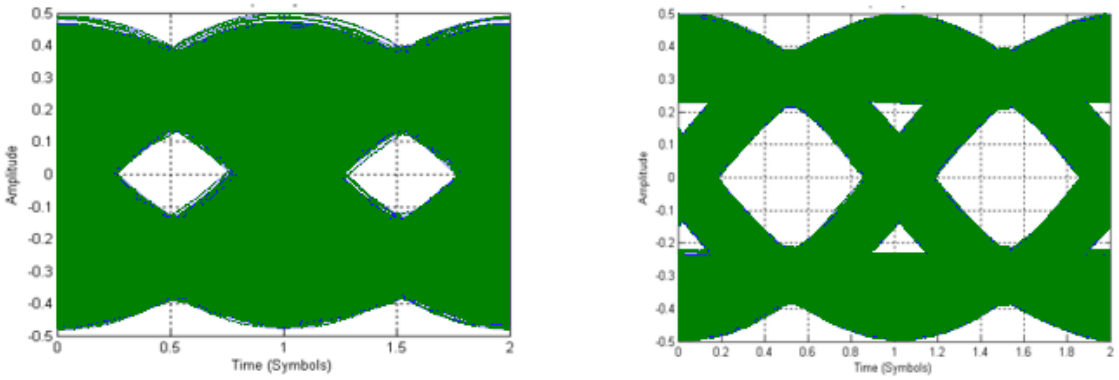


Figure 29. Frequency domain and time domain view of equalization effect



(a) HFCTLE only **(b) HFCTLE and MFCTLE**

Figure 30. Eye diagram with TX FFE and CTLE

In the next section, we will do the full link simulation with all the impairments included. In addition, DFE will be included in the simulations as well.

6. Cable Link Simulations

6.1 Simulation Setup

In this section, we simulate the cable system described in Figure 20, based on the time domain model, aimed at comparing link performance without and with MFCTLE. The simulated data rate is 25.78125Gbps; the test pattern is PRBS-23. All the impairments, such as noise, jitter, bandwidth limitations, and nonlinearities are modeled, based on either circuit design specs or lab data. Crosstalk aggressor sources are modeled by using full TX swing without de-emphasis. This is on the more pessimistic side as the aggressor sources have more energy than the victim channel source.

RX equalizer (CTLE/AGC/DFE) parameters are all adaptively tuned. We chose DFE to have either 1-tap or 8-tap, not to overwhelm the effect of CTLE. TX FFE is set to [-0.1375, 0.6375, -0.225], very close to that obtained from COM computations. TX swing is set to 1Vdpp. 2.5M bits are simulated for each setup, and the last 2M bits are used for post-processing.

6.2 Simulation Results

The simulated eye diagrams and the projected BER are summarized in Table 3. It is obvious that MFCTLE has exhibited tremendous positive impact on the link performance.

Despite this, not to be confused, the HFCTLE is still the primary ISI cancelation equalizer between the two. The MFCTLE works to fine tune the final performance. Or we can understand that it is a joint work between HFCTLE and MFCTLE, and actually also between TX FFE and DFE, that delivers the overall link performance.

Table 3. Performance summary to see the impact of MFCTLE on link performance

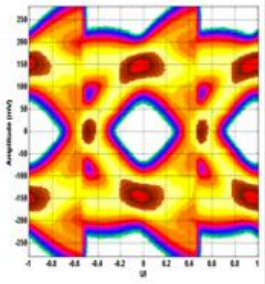
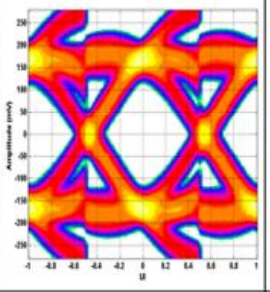
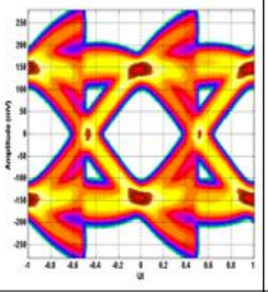
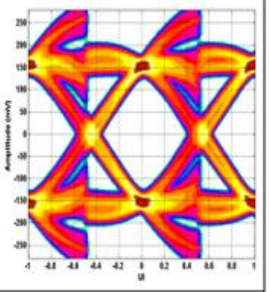
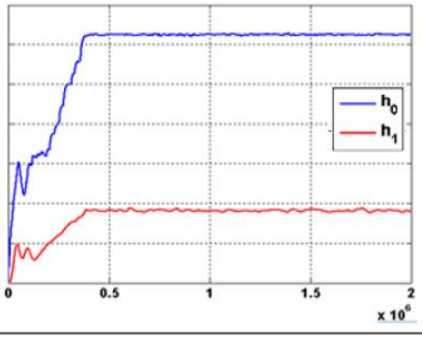
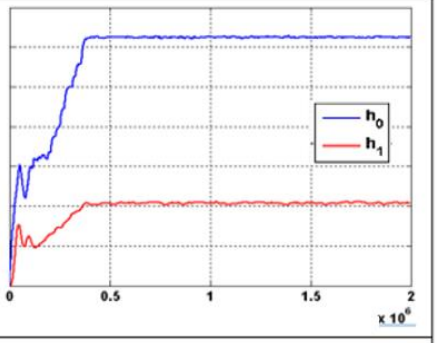
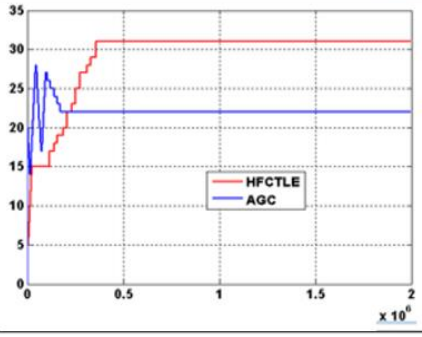
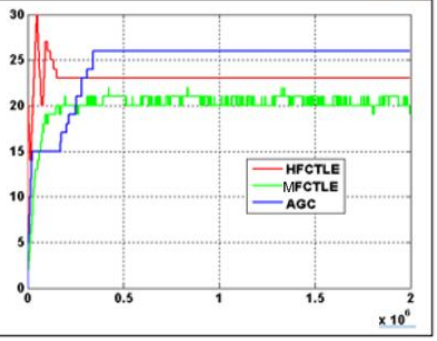
DFE tap = 1		DFE tap = 8	
HF CTLE	HF & MF CTLE	HF CTLE	HF & MF CTLE
			
1.2e-8	6.3e-18	1.4e-23	2.5e-54

Table 4. DFE and CTLE adaptation convergences for 1-tap DFE

	HF CTLE	HF and MF CTLE
h_0 and h_1		
CTLE & AGC		

CTLE, AGC, and DFE convergences are listed for the case in which DFE tap number = 1 in Table 4. What we observed is that with MFCTLE, the demand on HFCTLE is relaxed. For example, HFCTLE is maxed out at 31 when no MFCTLE is used, while HFCTLE = 23 when MFCTLE is applied. MFCTLE itself converges to between 20 and 21.

It is also seen that DFE tap h1 and error slicer h0 changed slightly between the two cases. It is now clear from the adaptation result why we picked the settings for the CTLE analysis in section 5.4.

7. System for 100GBASE-CR4

7.1 100GBASE-CR4 Setup

The 100GBASE-CR4 intended topologies for cable applications are depicted in Annex 92.5. The maximum channel insertion loss is as much as 35 dB at 12.89 GHz, illustrated in Figure 31. In addition, the cable assembly, host, and test fixture insertion loss budgets are detailed in the channel insertion loss budget [15, 16].

When the evaluation board for the TX and RX side are cascaded with the test fixture shown in Figure 10, the total insertion loss at 12.89GHz is about 36dB (Figure 32) for the setup we put together for evaluation. The hardware setup is shown in Figure 33.

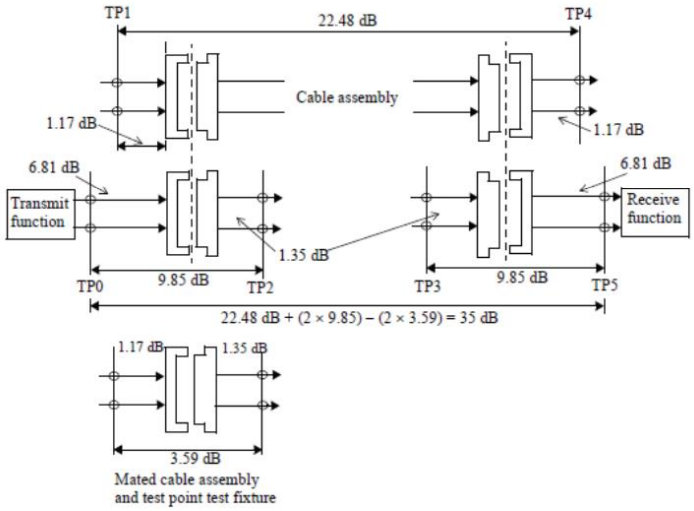


Figure 31. 100GBASE-CR4 test setup.

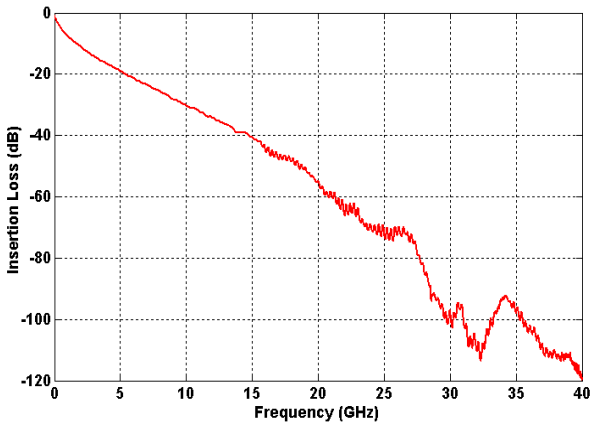


Figure 32. Total link insertion loss for 100GBase-CR4 simulation and measurement

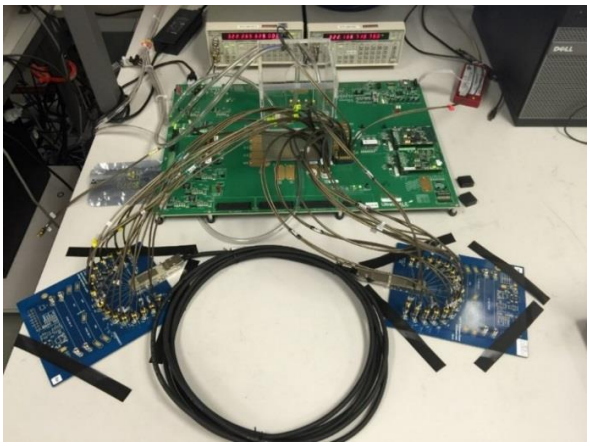
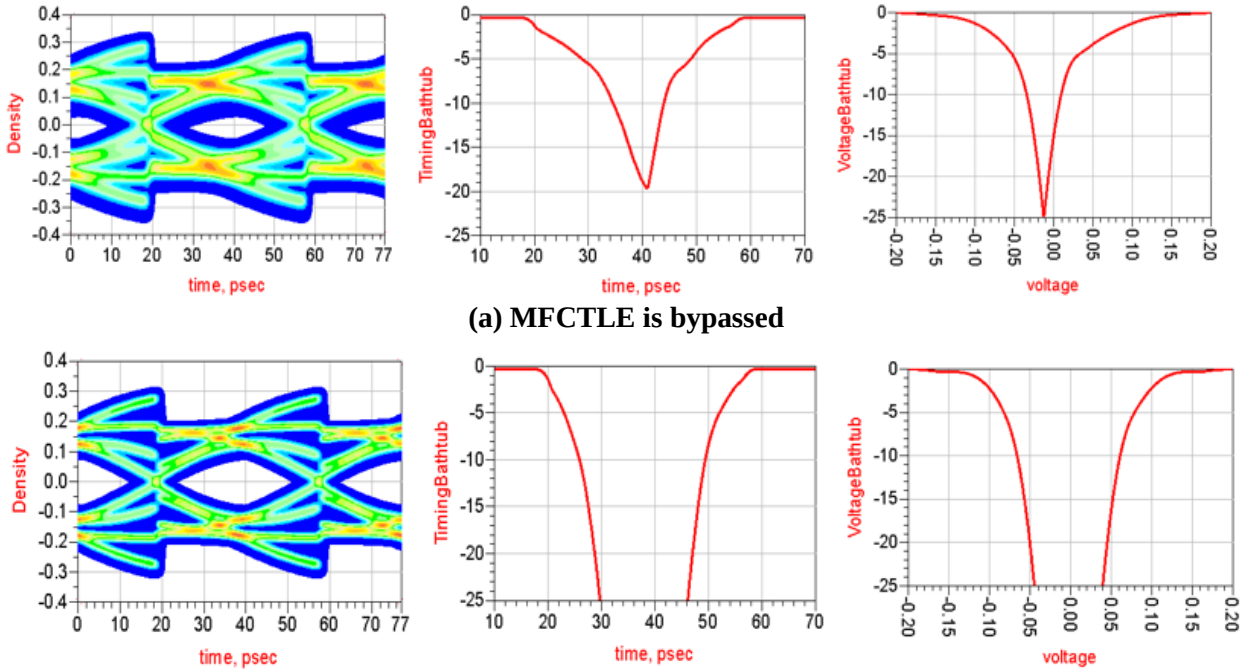


Figure 33. Hardware setup for 100GBase-CR4 measurement

7.2 IBIS-AMI Model Simulations

First, we simulate the link with a 20nm 28G-LR SerDes in the IBIS-AMI environment using Keysight ADS. The summary (eye diagrams, vertical and horizontal bathtub curves) of the simulation is given in Figure 34. It is obvious that without the MFCTLE the link would have required FEC to work below 1e-15. Once MFCTLE is included in the simulation, while in hardware it is always at work, the link shall work to a very low BER without the use of FEC. The verification of the simulation is shown next through lab measurement.



(a) MFCTLE is bypassed

(b) MFCTLE is on

Figure 34. IBIS-AMI model simulation for the setup in Figure 33

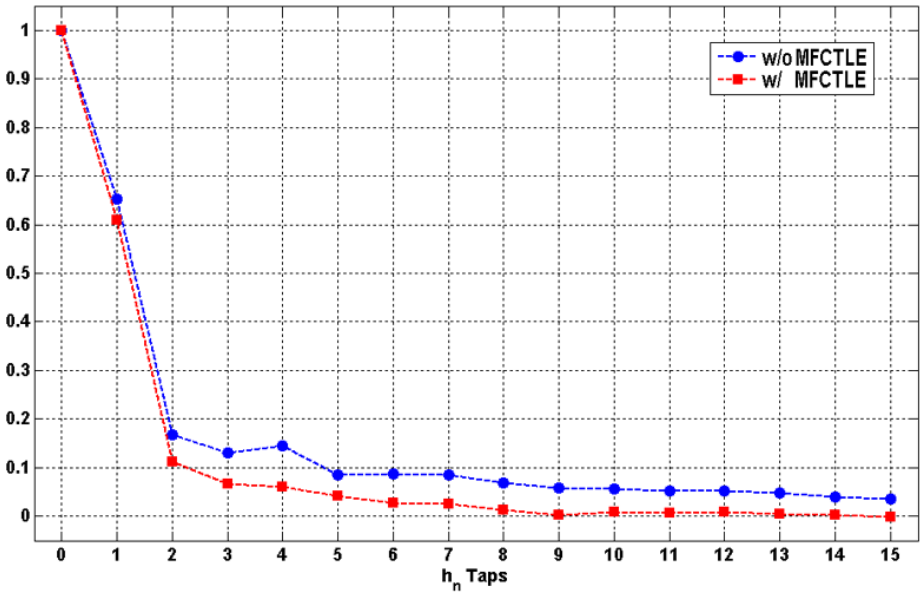


Figure 35. Normalized DFE tap converged values

Figure 35 shows the normalized (to error slicer, h_0) DFE tap converged values. It is clearly seen that (1) residual ISI is overall smaller when MFCTLE is in use, and (2) after tap 8, DFE taps are essentially not needed as the taps values are approaching 0.

7.3 Lab Measurement of 100GBASE-CR4 Setup

The lab test was carried out over 8 channels from 2 quads simultaneously. There is 200ppm frequency offset between the two quads. The crosstalk is naturally included in the setup.

The test showed that all 8 lanes worked error-free, without the use of FEC. The on-die eye scans are displayed in Figure 36 for all 8 channels. The internal eyes are not only wide open, but the variations among the lanes are small, further demonstrating the robustness of the system.

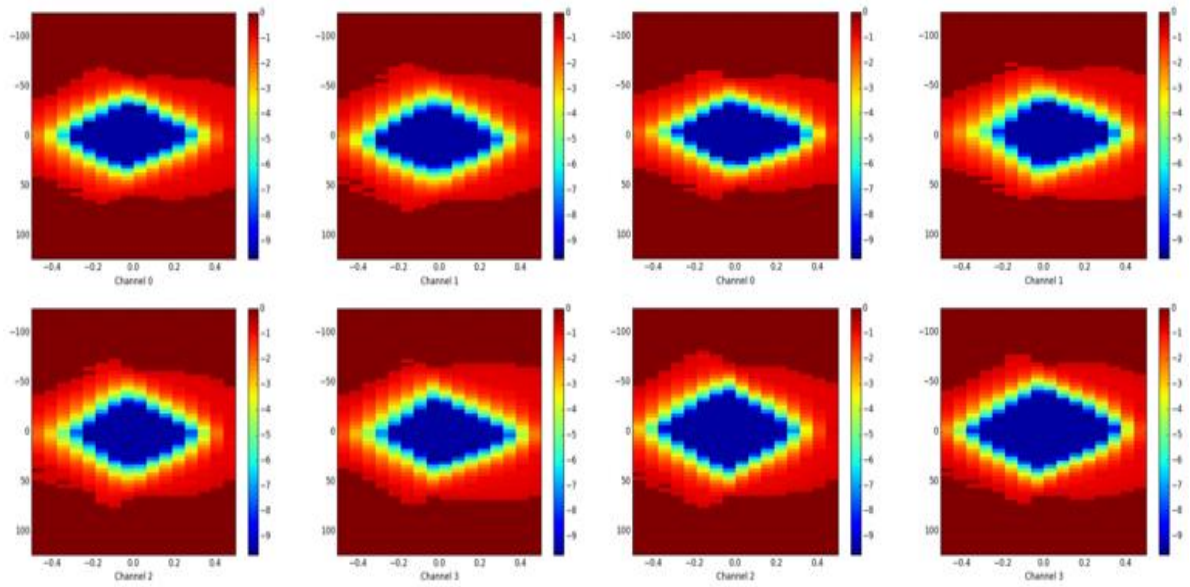


Figure 36. On-die simultaneous eye scans for the 8 channels tested

8. Conclusions

In this paper we have shown that the MFCTLE is a great performance enhancer to the ubiquitous HFCTLE, which in itself plays a big role in equalizing the channel. The MFCTLE is especially valuable for cable channels for 25G cable applications since the loss is more skin-effect dominated up to the Nyquist frequency. Both simulations and lab tests show that the SerDes with MFCTLE is capable of working with a CR4-compliant system without the FEC. Without the MFCTLE one would need to implement more complicated DFE to accomplish the same link margin.

Acknowledgment

The authors wish to thank Sai Lalith Chaitanya Ambatipudi for hardware setup and all the measurement data and Hongtao Zhang for the many insightful discussions.

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