DesignCon 2016

Investigation of Package Crosstalk and Impact to 28Gbps Transceiver Jitter Margin

Hong Shi, Xilinx
hongs@xilinx.com

Siow Chek Tan, Xilinx

Sarajuddin Niazi, Xilinx

Ravindra Gali, Xilinx

Abstract

Jitter margin loss as result of crosstalk impairment emerges as increasing challenge at 28Gbps and beyond. As silicon compensation is known ineffective to crosstalk, package becomes critical path of problem and solution. At this speed, signal coupling needs to be kept at well below -50dB in order to ensure adequate insertion-loss-to-coupling ratio (ICR) for protocol jitter compliance. In this paper, we studied coupling mechanism and design options to achieve -50dB to -70dB coupling for devices used in 28G long reach and mixed long reach and short reach environments. Furthermore, we solved the myth of power-ground co-referencing for high speed transceivers. The investigation is carried out by theoretical analysis, full-wave modeling, link simulation, and hardware measurement validation.

Acknowledgement

The authors sincerely thank **Santiago Asuncion, Sai Lalith Chaitanya Ambatipudi, Chris Borrelli** for their contributions in the specially crafted test setup and measurement. Your measurement data is one of the most critical evidences in demonstration of our theory and model to hardware correlation.

Author(s) Biography

Hong Shi is director of package design at Xilinx, driving architecture and product development along with design methodology for FPGA packaging platforms supporting ultrahigh speed signaling, IO, AMS, fabric and processors. Prior to Xilinx, he was senior manager of package development at Altera, leading product designs for high-end, mid-range and low-cost FPGA from 65nm to 14nm. Previously, he also worked at Hewlett-Packard microwave division and Agilent lightwave division, developing microwave circuits, optical front-end, and Infiniuum DCA 40-70GHz sampling module. Hong is recognized by the industry for his pioneering work in 28-Gbps FPGA package, 3D IC packaging, switching noise theory and simulation methodology, power supply noise to jitter transfer theory, lightwave instrumentation, and femtosecond photonics. Hong Shi holds a Ph.D. in Electrical Engineering from the CREOL School of Optics, University of Central Florida; MSc. in Physics from DePaul University; MSEE, BSEE from Xi'an JiaoTong University. He holds 30 patents and has authored over 60 technical articles and one book chapter in refereed journals and conference proceedings. In recent events, he is co-chair of the high performance high density 3D/2.5D package panel at DesignCon 2014. He is the keynote speaker in SEMICON China/CSTIC 2014 Package and Assembly Symposium, plenary speaker of IoT forum at IEEE EPTC 2014 Singapore, invited speaker in industry section of IEEE EDAPS 2015 Seoul Korea.

Siow Chek Tan is a Staff Package Design Engineer at Xilinx. Her responsibilities include the package development and design methodology for FPGAs. Her areas of interest are signal integrity and high-speed transceiver channel design. Prior to Xilinx, she was with Altera Corporation, working on package development across the wirebond and flip-chip product lines. She obtained BSEE in Telecommunication from University Technology Malaysia.

Sarajuddin Niazi is currently a Staff Signal/Power Integrity Engineer at Xilinx, Inc. At Xilinx Mr. Niazi responsible for developing Package solution for high speed Serdes. Mr. Niazi joined Xilinx four years ago. Prior to joining Xilinx, Mr. Niazi worked at Startup Company specializing in low loss high-speed interconnects design. Mr. Niazi received his Bachelor of Science degree in Electrical Engineering at the University of California at Davis. Mr. Niazi has a patent application in the field of Signal integrity.

Ravindra Gali is currently a Staff Product Applications Engineer focusing on Signal/Power Integrity at Xilinx, Inc. Prior to joining Xilinx, Mr. Gali worked in various roles as a SI/PI Design/Application Engineer at Altera, Intel & Dell focusing on PCB/Package Signal and Power Delivery issues. Mr. Gali has over 10 years of industry experience along with an MSEE and MBA degree from New Mexico State University and San Jose State University respectively. Mr. Gali has a patent application in the field of signal and power integrity as well

Introduction

Dominant crosstalk noise comes from inductive coupling of electromagnetic field inside package and between package and PCB interface. As transceiver density and speed doubling every two silicon nodes, the challenge has grown to one of the most demanding in recent years. For receivers, crosstalk noise behaves as wideband noise that silicon compensation is incapable of or ineffective in equalizing. Moreover, high insertion loss associated with high density package squeezes the margin between insertion loss and cross coupling additionally. As part of total link budget, package is allowed to attenuate no more than 2.5dB at either transmitter or receiver and to couple lower than -50dB noise aggregately among all transmitting lanes.

This paper summarized our investigations to advanced crosstalk mechanisms in 16-32Gbps speed packages and its impact to 28Gbps links. Often the crosstalk presents itself as a prevailing and compound effect to cause excessive jitter in a transmitter device and system. It should be noted that mechanisms investigated in the paper go beyond commonly known causes from narrow line spacing, reference plane cut, to lack of ground shielding. For the first time to our knowledge, this paper identifies the advanced crosstalk categories and peels off precisely individual contribution of each type to jitter margin inside and around very high speed package. For system design engineers, this paper becomes practical to refer to because all crosstalk phenomena and mitigations are studied in real 28Gbps long reach and mixed long/short reach links.

The first type of crosstalk is *package to PCB breakout coupling*. The mechanism is straightforward: inductive coupling among "cylinders" made with BGA balls and extend PCB vias underneath. Its detrimental effect is direct, severe, and indifferent of PCB board optimization. This is detailed in the first section. As mechanism is left with no suspense, our study focuses on quantify coupling to jitter conversion and mitigation strategy validation.

The second type of crosstalk is *vertical structure to horizontal trace coupling*. It is an entirely package internal effect, and can take form of TX via to RX trace (TX-to-RX coupling) and RX via to RX trace (RX-to-RX coupling). The mechanism is a more involved inductive coupling associated with design options and tradeoff. One tradeoff that is known now magnifying the coupling is "skip-layer" transmission line made to balance insertion loss, coupling and lane density. In section two, coupling from skip layer and single layer stripline are compared by coupling efficiency (Sij in dB). Hardware characterization validates clear relationship between compound effect of first and second type coupling and jitter margin loss.

The third type of crosstalk is *power-ground co-referencing* at package to PCB breakout. It is often found in packages where pin efficiency and channel density are of high importance. The mechanism is most intriguing at first but made evident throughout our study. As such, we established effective design rule and rectified power-ground co-reference as a safe, well controlled, and definitive low cost solution for identified high speed applications

Section I: Package to PCB Breakout Coupling

As shown in Figure 1, common BGA pattern of high speed transmitter package has TX and RX pairs diagonally separated and with ground pins surrounding. If the isolation pins consists of mixed power and ground, it is called power-ground co-referencing (Figure 1[b]). The inductive [M]di/dt coupling exists between direct TX-to-RX cylinder loop and between TX-to-Gnd and GX-to-Gnd cylinder loops, where [M] is accumulated mutual inductance and can be minimized by greater spacing. Once the BGA template is set, PCB via will be drilled following the same pattern and same spacing. Usually, inner channels from package edge have longer via length so able to escape beneath outer channels. The longer PCB via the more the accumulated coupling . There is little that PCB engineers can do to increase TX-RX spacing.

A resulting power-sum coupling of Figure 1[a] pattern is shown in Figure 2[a red]. In this chart, PCB via effect is removed to expose the net package effect. It can be seen that couplings at many frequency points are above the virtual -50dB spec. Finite PCB via length at various depths will simply contribute additional coupling. Lab measurement confirms more than 20% jitter margin loss is possible in a 28Gbps LR system setting.

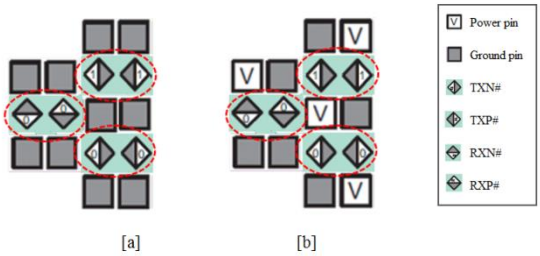

Figure 1. BGA pin-out. [a] All ground. [b] Power and ground co-reference

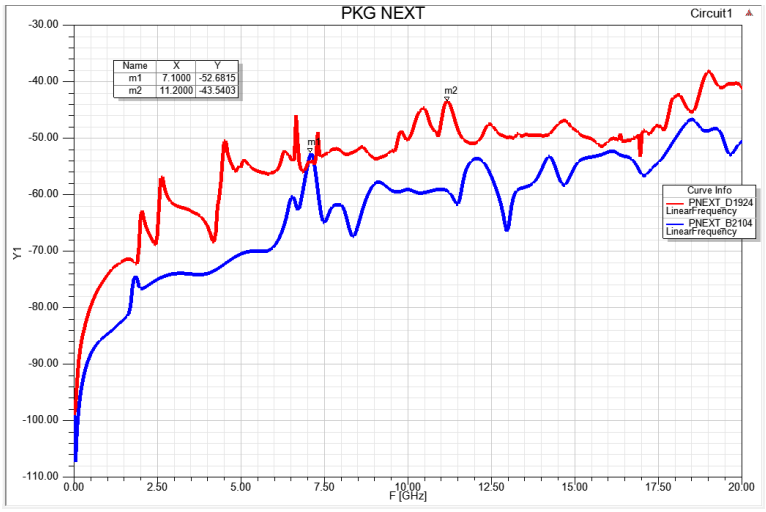

Figure 2. Power sum coupling. [a] diagonal TX-RX, [b] with ground pin wall

In order to meet the -50dB coupling spec, a dedicated ground pin wall is inserted between the closest TX and RX pins. The objective is to increase TX and RX spacing as accumulated mutual inductance [M] is inversely proportional to signal spacing. In 1mm BGA package shown in Figure 3, the new pattern has 2.2mm spacing as opposed to 1.4mm, a factor of 0.63 of that in absence of ground wall. The resulting power-sum coupling of new pattern is shown in Figure 2[b blue]. Lab measurement validates that new pinmap generates less than 10% jitter margin loss in a 28Gbps LR system setting.

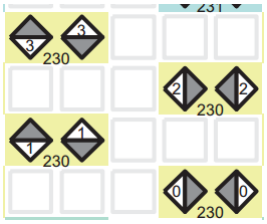

Figure 3. Ground pin wall separating TX and RX pins

It should be mentioned that dedicated ground wall is a deliberate option for 28G Long Reach links. While justified for the most challenging 28G system design, it requires more pins and perhaps larger size package. We are obligated to ask ourselves what else noticeably attributes to coupling and how to minimize.

Section II: Vertical Structure to Horizontal Coupling

From system perspective, the insertion loss to coupling ratio (ICR) is often used to gauge compound effect of practically allowed coupling in associated with system loss. Skip layer is known as a package design choice in mitigating metal loss by using wider trace width and two layers of equivalent substrate thickness for nominal 50/100Ohm characteristic impedance. The net loss reduction is ~0.09dB/mm vs. ~0.11dB/mm single layer. Figure 4 shows sketches of skip layer and single layer stripline. Power planes are often assigned to those skipped layers to harden closely coupled low impedance power distribution network.

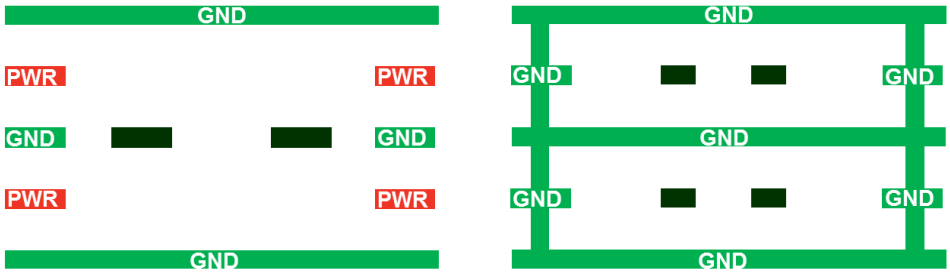

Figure 4. Skip layer (left) vs. single layer stripline structures

In a high density package, the magnetic flux excited in the vertical signal-to-ground loop structure has the in-line direction with horizontal loop formed between stripline transmission line and ground plane. As signal via is made close enough to broad side of stripline, strong inductive coupling occurs between two structures and becomes profound around "skip-layer" stripline. Figure 5 depicts this physic phenomenon for skip layer. Owing to the floating nature of power traces between skip layer striplines, power cavity resonance can be excited by the adjacent vertical signal transition through the stated coupling mechanism. The resonance of power-ground cavity can effectively couple to adjacent skip layer stripline that has tall dielectric height.

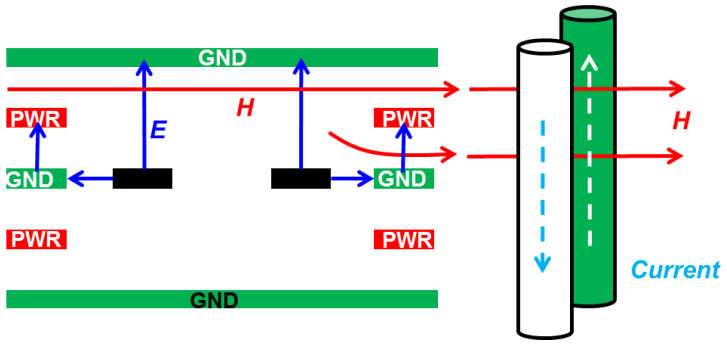

Figure 5. Vertical structure to horizontal trace coupling mechanism

The resulting skip layer coupling is shown in Figure 6 [a, green] and [b, blue]. One can notice the distinct peaks in both coupling curves that manifest resonance happening. In contrast, single layer stripline shows resonant less, smooth, monotonic coupling behavior as in [c, red], because non-existence of power cavity and possible stitched ground via wall if line/spacing allows. The difference between three curves is as following from top to bottom: regular diagonal separated TX-RX BGA and skip layer; ground wall separated TX-RX and skip layer; ground separated TX-RX and single layer. From this chart, the single layer structure is seen most effective in crosstalk reduction.

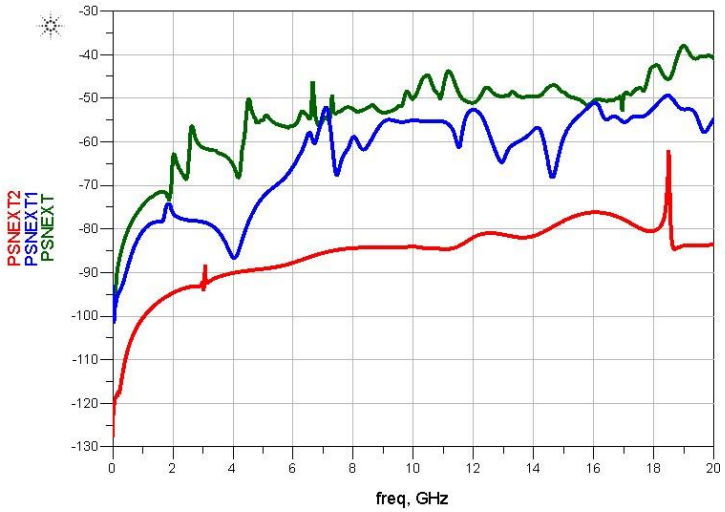

Figure 6. Cross coupling between TX and RX. Top/green: skip layer, diagonal pin separation. Directly lower/blue: skip layer, ground pin wall separation. Bottom/red: single layer, ground pin wall separation

Considering dominant loss is from backplane, skip layer stripline on package is unjustified for its benefit lowering loss while generating crosstalk. An extraordinary of -80dB coupling is achieved by single layer structure together with ground wall pins in very high serdes density, ordinary organic substrate package design as all dominant crosstalk source is removed.

In the next, we will address compound crosstalk (Section I and II) to jitter margin correlation by *link simulation* and *hardware measurement*. Time domain simulations were performed on two different packages designs to study the performance differences. Package A was designed using skip layer approach with wider trace geometries to meet the Tx/Rx characteristic impedance. The package was also designed to optimize the pin count thereby eliminating the ground wall shielding between the TX and RX. Package B was designed using conventional stripline routing along with having a dedicated ground wall of pins to completely shield the TX and RX. The link model is shown in Figure 7.

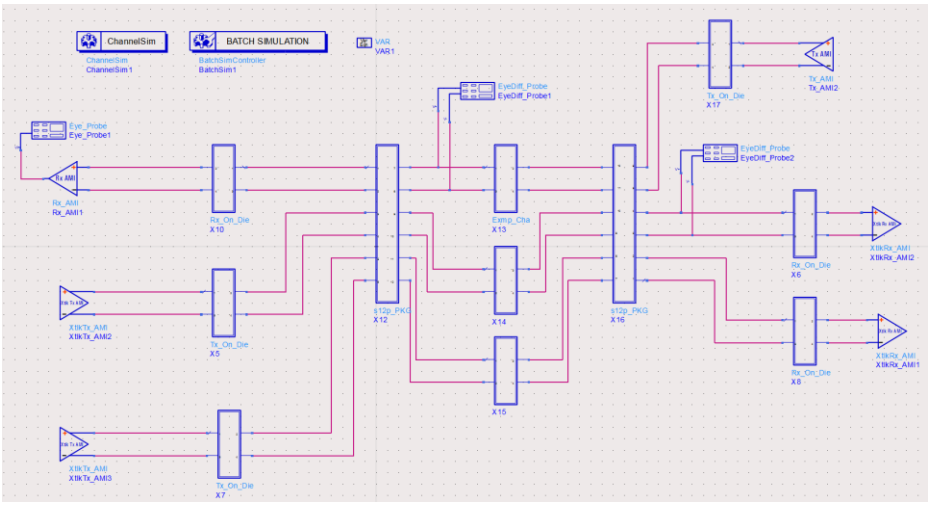

Figure 7. Link simulation to correlate crosstalk to jitter margin loss

The simulation setup consists of 2 GTY TX drivers, 1 GTY RX receiver with the TX buffers acting as aggressors on the Rx victim. The setup consists of .s12p package model that takes into account any coupling that exists between the GTY TX and GTY RX channels on the package. The two TX aggressors are driving a short reach channel with insertion loss of -3dB. The two TX aggressors run an identical PRBS31 pattern operating at 28Gbps with their output differential (pk-pk) swing set to 0.902V. The Rx victim passes through a back plane channel with an insertion loss of -30dB running a PRBS31 pattern that is independent of the aggressor's data pattern.

We deliberately design the simulation to allow aggressor eye edges to sweep through victim in order to capture the worst crosstalk-to-jitter conversion. The data rate on the victim is swept all the way from 20Gbs to 25Gbs in a step size of 0.25Gbs to evaluate any jitter sensitivity. Limiting frequency sweep range is due to time and computing resource constraint. Thus we focus on spectrum where crosstalk is greatest.

All the reported eye width numbers are measured at the die (Eye_Probe1) for a BER of 1E-9 after the CTLE/DFE at the RX victim in the presence/absence of TX aggressors. To minimize the run time of the simulations, the simulation run was limited to 1million bits in a bit-by-bit mode in ADS. The same simulation was repeated using the two different package (Package A, Package B) models to study their effectiveness to crosstalk. The results are shown in Figure 8 in terms of Nyquist frequencies from 20Gbps to 25Gbps. It can be seen that average difference is 3% and most difference is up to 5%. The magnitude trend correlates well with dB crosstalk between structures of skip layer +diagonal separation and single layer + ground wall. The jitter humps does not correlate exactly to resonance peak in terms of frequency. This can be explained with overall less crosstalk in absence of PCB. We believe that only for large (worse) enough crosstalk does the peaks correlate.

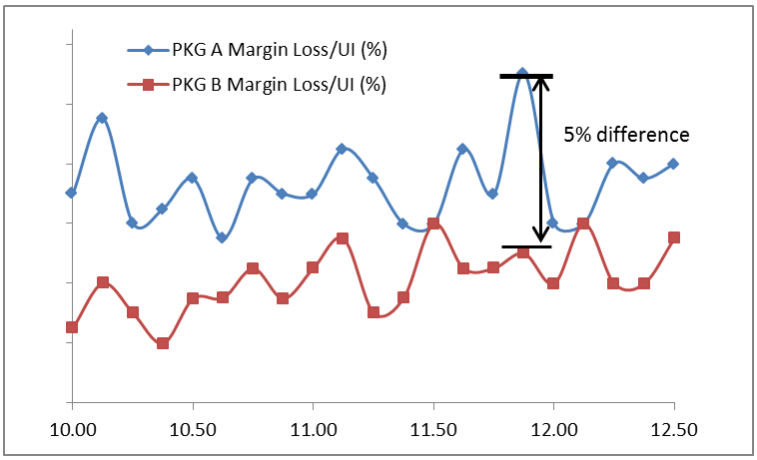

Figure 8. jitter margin loss comparison. Top/blue: skip layer, diagonal separation. Bottom/red: single layer, ground pin wall separation

In order to address the resonance frequency correlation between dB crosstalk and jitter, a special designed measurement was carried out for crosstalk and jitter between two RX lanes. Both RX lanes have skip layer structure and diagonal separation without ground wall. The test fixture includes PCB breakout. Thus, maximum amount of crosstalk (and resonances) and jitter should be expected. Again, here the data rate is swept across 8GHz (16Gbps) to 14.5GHz (29Gbps). The test setup and test conditions are depicted in Figure 9.

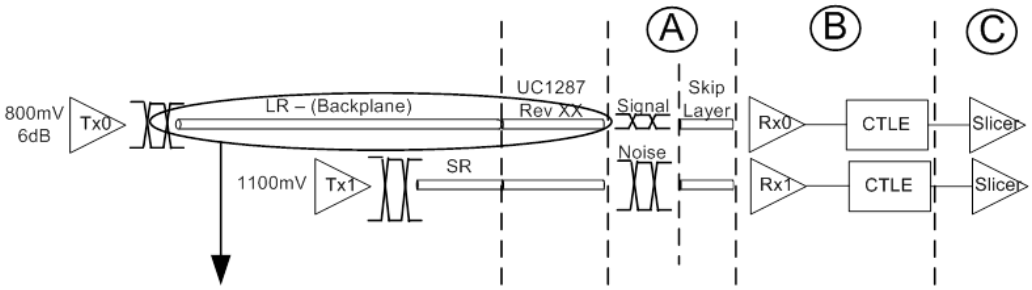

Figure 9. Hardware measurement setup for resonance correlation

Signal amplitude at A will decrease with increasing frequency according to the insertion loss profile. Thus, signal amplitude is not constant across frequency. We choose a linear dB portion on backplane and board insertion loss between 8GHz – 14.5GHz. On the other hand, aggressor noise amplitude is assumed constant across frequency because of the short reach. The jitter margin loss is plotted across 8-14.5GHz as shown in Figure 10. A VNA s-parameter measurement is performance to observe the dB coupling between these two RX lanes. The result is shown in Figure 11.

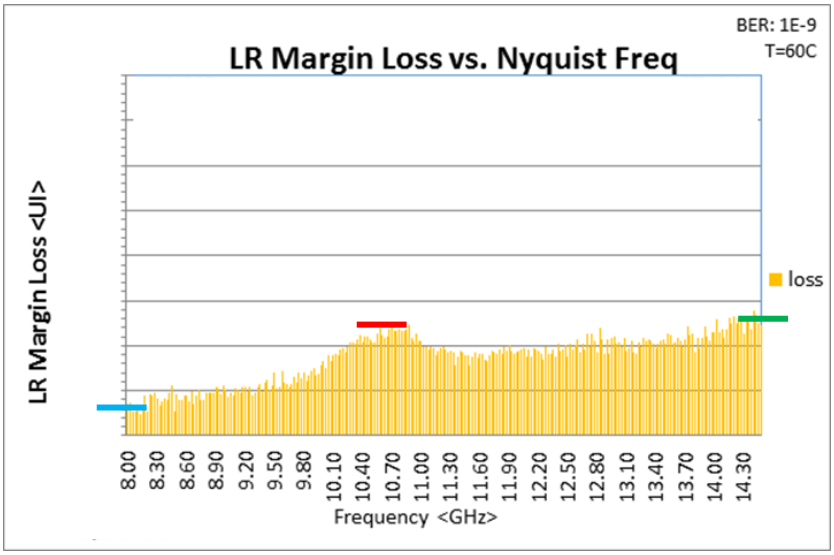

Figure 10. Jitter margin loss as a function of 8-14.5GHz (data rate: 16-29Gbps)

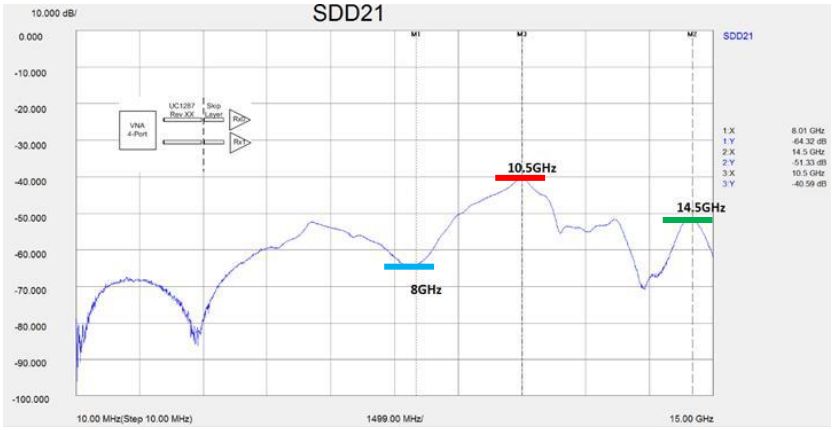

Figure 11. RX-RX coupling s-parameter measurement by VNA

One can notice unambiguously that the crosstalk peaks (troughs) caused by skip layer power resonance correlates accurately with resulting peak jitter margin loss. A maximum at 10.5GHz is observed in both curves, a minimum (lowest point in jitter plot) at 8GHz is observed at both curves. The 14.5GHz local maximum is out of chart in jitter plot, but it is seen returning from low and approaching to a high value.

Section III: Power-Ground Co-Referencing Coupling

The third type of crosstalk is caused by power-ground co-referencing at BGA pins in package to PCB breakout. This type of pinout is often found in packages where pin efficiency and channel density are of high importance. Inside package, all transceivers are referenced solely to ground plane and vias.

With increasing demand of data path bandwidth, the transceiver channels and DDR I/Os have been increased rapidly. The high density requirement drives up package size and BGA ball count. Although many applications accept 0.8mm or smaller ball pitch for additional balls, the mainstream systems in wireline and wireless remain firmly at 1-mm pitch requirement. As such, how to improve channel density with little package footprint expansion becomes one of the toughest industry challenges.

One method is to replace certain numbers of dedicated ground pins with power pins, as such originally reserved power pins can be spared for signals. It is sometimes called power-ground co-referencing. The conventional wisdom behind this approach is that power can be as effective return path as ground, often referred as AC ground. Owing to inductive nature, power pins experience distinct resonances depending on topology and value of LC elements in PDN networks. As the result, signals separated by power pins can couple through power resonances. This effect becomes more profound for transceivers devices operating at 16Gbps and higher data rate.

Recently, several studies have been carried out to understand co-referencing behavior and mechanism. Shi et al. investigates DDR I/O performance in an I/O power-ground referencing [1]. Both simulation and bench measurement are provided to demonstrate the performance difference. Zhang et al. published simulation study for transceiver power-ground co-referencing [2]. It is so far the most in-depth modeling study and observation to crosstalk arising from transceiver power as co-reference. However, both studies are insufficient in explaining fundamental physics and deterministic behavior. As such, both papers are left inconclusive in terms of whether power as co-referencing can be used in very high speed transceiver designs.

The study is carried out on a multi-layer flip-chip FBGA package. Transceiver channels are escaped and routed on layers above core layer. Then it is directly connected to BGA balls through micro vias and plated-thru-hole vias (PTH). For the vertical transition, signal vias are properly coupled to ground vias to ensure accurate characteristic impedance and adequate separation from other signals. Inside the substrate, the signal is solely referenced to ground. The PCB is also assumed to have ground only reference. Only at BGA pinout and at PCB via breakout does power-ground co-referencing exist. As shown in Figure 12, a typical single lane pinout consists of one TX differential pair and one RX pair separated diagonally, as indicated by the diamond symbols. This is the same as Figure 1[a].

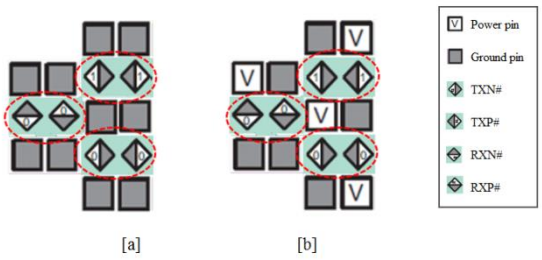

Figure 12. Power-ground co-referencing pinout [b]

For repetitive patterning, each TX (or RX) has two ground pins associated. As the pattern panned out, each TX (or RX) is surrounded and isolated by all ground pins except at diagonal direction. Now replace ground pins with power pins in locations labeled with square embedded with letter V. One can see half of ground pins per lane are now in place of by power pins (except one case at lower left side). It can accumulate significant pin saving as channel count explodes. Another observation is that power and ground pins are kept adjacent to ensure low inductance.

With the power co-referencing, the initial observation is a different crosstalk behavior and significant magnitude in the frequency range of 15GHz to 20GHz, right at neighborhood of Nyquist (clock) frequency of 28-32Gbps. As expected for all-ground referencing, the TX to RX crosstalk is a smooth curve with coupling efficiency (Sij in dB) monotonically increasing with frequency. In Figure 13, the green curve represents all-ground, and the red curve represents power-ground co-referencing. It can be clearly seen that power-ground co-referencing creates 20dB crosstalk hump at ~17GHz.

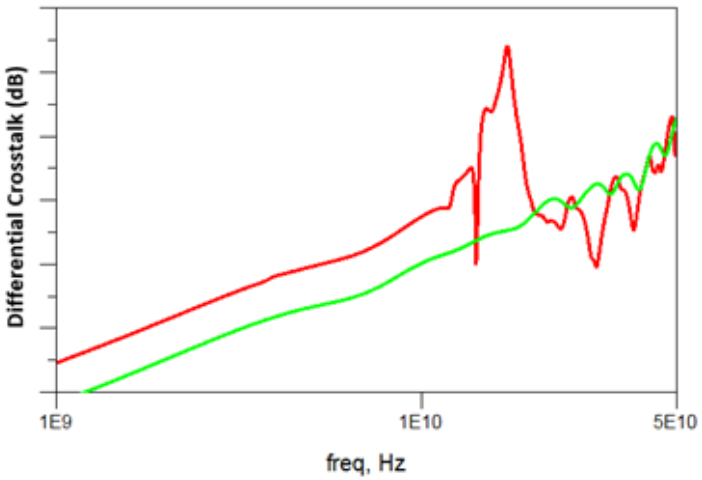

Figure 13. Differential crosstalk. Top/red: Power-ground-co-referencing pinout. Bottom/green: all-ground pinout

Here we provide the fundamental physical mechanism to explain the abnormal crosstalk behavior. At the pinout interface, PDN network behaves as inductively coupled resonator coupled equally to TX and RX pairs. The intrinsic PDN impedance resonances are the Eigen-modes supported by geometry of a specific PDN network. The transfer function from TX (or RX) to PDN is a multi-notch bandpass filter with dominant passbands in frequencies where PDN experiences the least impedance.

Figure 14 shows the schematics of inductively coupled resonator (top), and modeled intrinsic PDN impedance resonance and transfer functions for each TX0, TX1, and RX0 respectively (bottom). It can be seen that all three transfer functions have the common highest passband overlapped around 17GHz to transfer signal spectral energy maximally through the PDN network. The PDN has the lowest local low at 17GHz. The

resulting TX to RX coupling is also modeled and plotted in Figure15. Because the dominant passband magnitude is 20dB higher than the rest peaks, TX and RX transfer spectral energy mostly at passband frequencies.

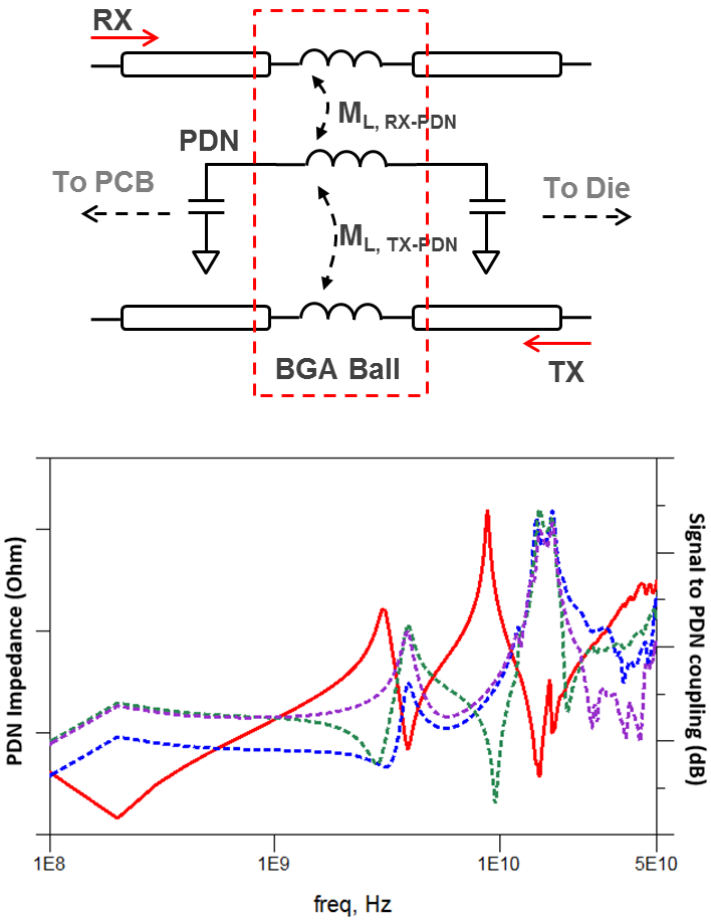

Figure 14. Schematics of inductively coupled resonator (top). Modeled intrinsic PDN impedance resonance and transfer functions from each TX0, TX1, and RX0 to PDN respectively (bottom)

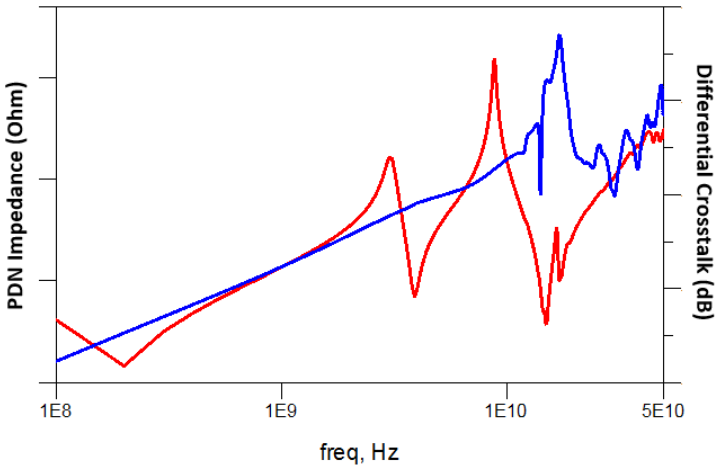

Figure 15. TX to RX coupling in relative to PDN resonance

Now that it is known that PDN plays coupling media role, design mitigation will focus on engineering the PDN network. Our goal is to reduce high-Q resonant peaks to minimize signal spectrum transfer. Figure 16 is a typical PDN network equivalent circuit. It consists of multiple LC elements. Each L is representative of vertical via transition. Each C represents coupled power and ground plane pair.

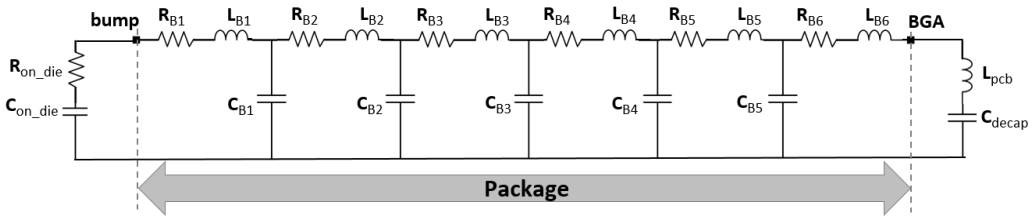

Figure 16. Package PDN equivalent circuit. Here the focus is around BGA pins

The original PDN that creates resonances has three LC sections with a dominant L as result of power via transition directly from top layer near die to BGA ball. It creates strong lump effect characterized with a high-Q resonance following the equation at below:

$$Q = (1/R)\ [\sqrt{(L/C)}]$$

In order to eliminate the high-Q resonance, the well-known method can be leveraged to add extra capacitance into PDN network to make multi-section PDN transmission line. This is translated into adding extra power/ground plane pairs close to BGA pin out (bottom layers of package). *It should be noticed that this PDN enhancement is sole requirement for crosstalk reduction, rather than PDN impedance seen by die*. The PDN as-is is adequate to meet low impedance target to deliver power over entire signal frequency range.

After the layout is revised, the new PDN characteristic impedance curve is shown in Figure17. The resulting crosstalk reduction between the same TX-RX pair is shown in

Figure 18 accordingly. The salient result shows 17dB improvement for adjacent TX and RX. By this result, both ground only referencing and power-ground co-referencing yield similar TX to RX crosstalk.

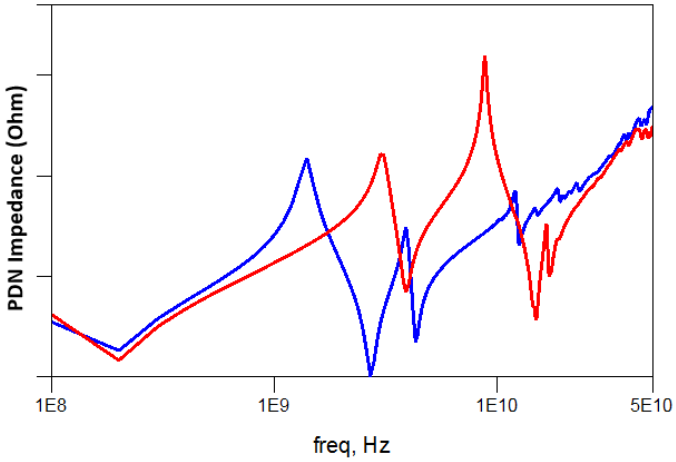

Figure 17. PDN resonance reduction after additional pairs added near BGA

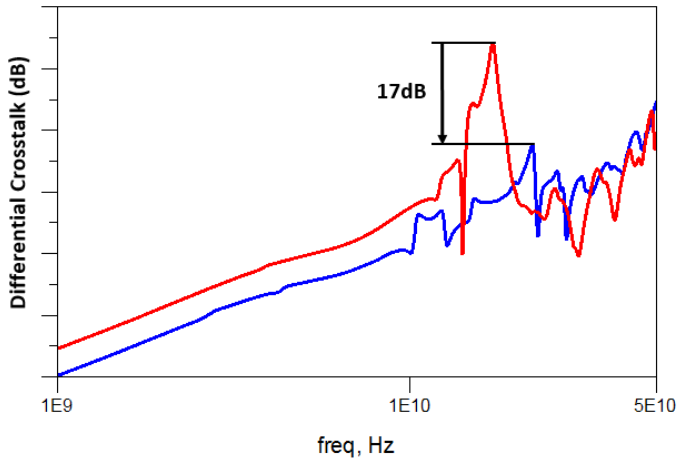

Figure 18. Cross coupling improvement after PDN resonance is damped

In summary to power-ground co-referencing crosstalk, we find and validate by modeling that PDN network behaves as inductively coupled resonator coupled equally to TX and RX pairs. The transfer function from TX (or RX) to PDN is a bandpass filter with dominant passband in frequencies where PDN experiences the least impedance. With design enhancement, the performance difference between power-ground referencing and all-ground referencing are practically negligible. Under both conditions, -50dB at 16GHz isolation can be achieved. As the result, package designers can use power pins replacing ground pins for up to 50% pin count saving without compromising performance of transceiver.

Summary

Three types of advanced crosstalk mechanisms are clearly identified and thoroughly studied for its individual behavior and compound effect to jitter margin loss. *Package to PCB breakout coupling* is attributed to inductive coupling among "cylinders" made by BGA balls and extend PCB vias underneath. Its detrimental effect is direct, severe, and indifferent of PCB board optimization. The mitigation to specific 28G long reach devices is to implement additional ground pins. *Vertical structure to horizontal trace coupling* is attributed to the magnetic flux excited in the vertical signal-to-ground loop structure and coupled to the horizontal loop formed between stripline transmission line and ground plane. This phenomenon is found to be profound in "skip-layer" transmission line structures. Both types of package crosstalk are validated by 28G long reach simulation and hardware measurement to show direct and precise correlation to jitter margin loss measured at receivers. We demonstrated package solution offering lower than -70dB cross coupling between TX and RX pair with using ground wall and single layer stripline. For mixed short reach RX and long reach RX application, as low as -50dB coupling can be achieved in our package design.

Power-ground co-referencing induced crosstalk is attributed to inductively coupled PDN resonator coupling equally to TX and RX pairs. The transfer function from TX (or RX) to PDN is a bandpass filter with dominant passband in frequencies where PDN experiences the least impedance. With design enhancement, the performance difference between power-ground referencing and all-ground referencing are practically negligible. As low as -50dB at 16GHz can be readily achieved in our package design. As the result, package designers can choose using power pins replacing ground pins for up to 50% pin count saving without compromising performance of transceiver.

Lastly, we suggest various levels of package options for different high speed link applications. For short and mid-reach 16-32Gbps transceivers, loss-to-coupling ratio is ample to allow extra crosstalk. Power-ground co-referencing can be implemented in package pinout for superior pin efficiency and cost saving. For long reach 28G and 56G PAM4, ground wall pinout should be used and advantage of -70dB crosstalk can be taken in system design.

References

[1] Hong Shi, Xiaohong Jiang, Yeehuan Yew, "Effect of Power and Ground Co-Reference to Performance of Memory Interface I/Os in FPGA and Structural ASIC Device Package", Electronic Components ans Technology Conference, 2007.

[2] Jianmin Zhang, Siow Chek Tan, Hong Shi, Dan Oh, "Investigation of Power & Ground Co-Reference for High-Speed Signal in Package Design", IEEE International Symposium on Electromagnetic Compatibility 2013.