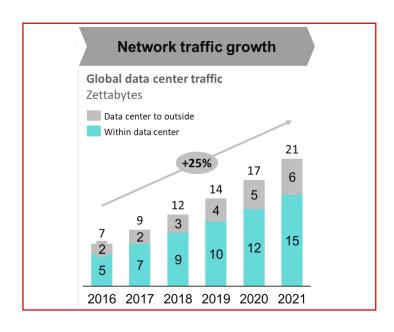
# Xilinx Alveo U25 SmartNIC Platform Launch Press and Analyst Briefings



## **Networking Crisis in the Data Center**



Explosion of Network Traffic in the Data Center



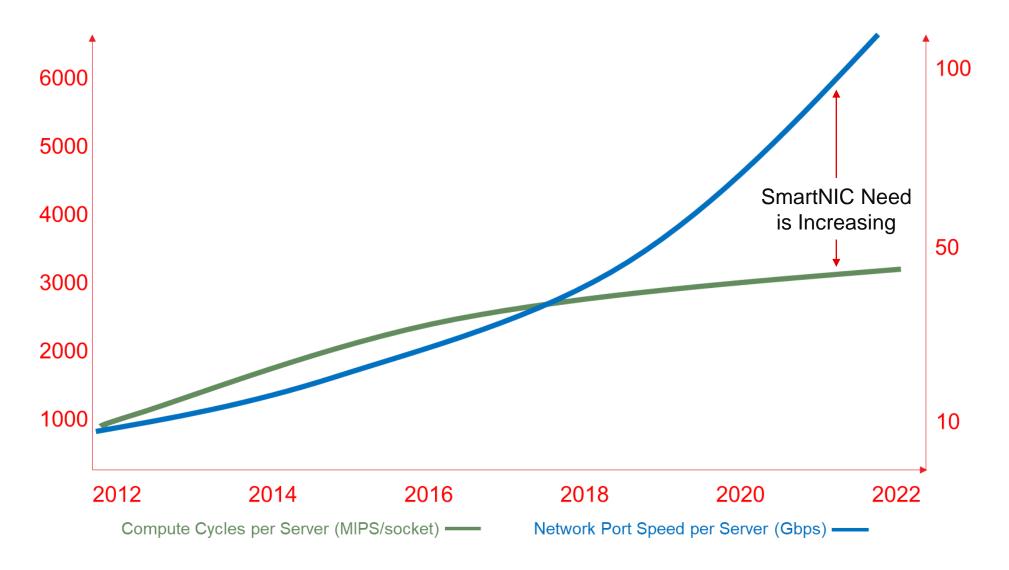
Significant Compute Resources
Dedicated to Networking

>80%
Cloud Server Nodes don't have SmartNIC access Today

Networking offload is hard to implement today



## **Port Speeds Outstripping Moore's Law**





## **Announcing Industry's First Comprehensive SmartNIC Platform**

True convergence of network, storage, and compute acceleration functions on a single platform

Bump-in-the-wire network, storage, and compute offload and acceleration

Powered by new Line of Powerful Alveo™ SmartNICs

Starting with Alveo U25 SmartNIC

Delivers range of turn-key accelerated applications

Open vSwitch, IPSEC, ....

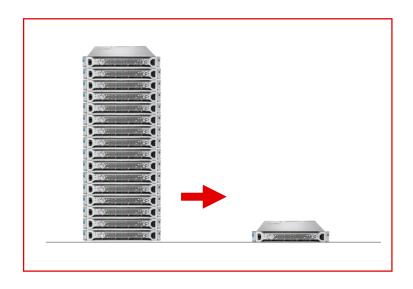
Fully Programmable

With Xilinx Vitis™ Unified Development Environment

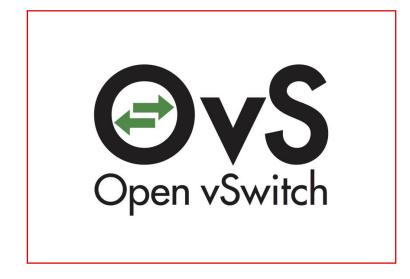




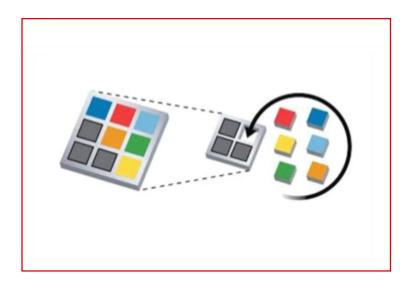
## Why Xilinx SmartNIC Platform Matters



Simplified and lower cost data center infrastructure



Turnkey applications that cover a broad set of compute problems

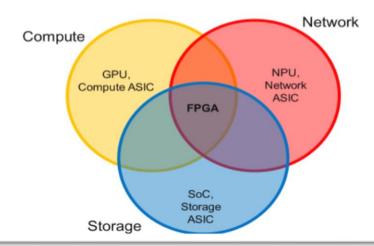


Optimize or extend functionality leveraging programmability and IP plugins



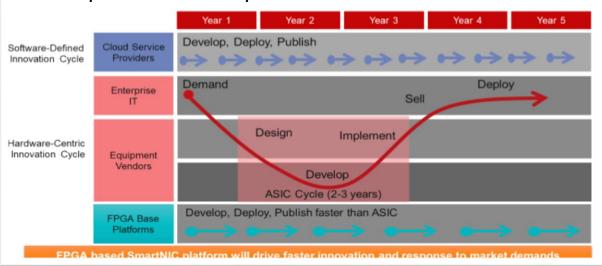
### Core Attributes of Xilinx FPGA SmartNIC Platform

Great for Network, Storage, and Compute

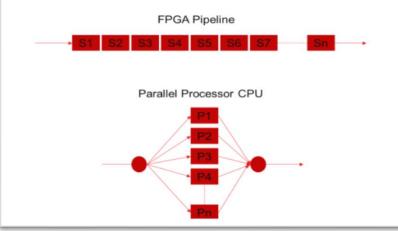


FPGAs Are Uniquely Positioned to Handle the Widest Range of Data Center Workload – the only Technology that Occupies all 3 Circles in the Venn Diagram

#### Development at the Speed of Software



#### Performance/Watt is 10x better than SoCs



- One packet per processing stage
- Pipeline has enough stages to process entire data plane
- High Degree of Parallelism (1000's)
- Can complete one packet per clock cycle – 300Mpps at 300Mhz
- One packet per Processor CPU
- One CPU takes 100's-1000's of cycles to process a single packet
- Low Degree of Parallelism (8-16)
- Throughput proportional to number of instructions/pkt divided by clock cycle time times the number of cores
- 32Mpps for 16 core processor@2Ghx

#### Cloud Ready

- New Functions can be developed and loaded while the FPGA is running existing functions
- Functions can be connected and combined dynamically
- For Cloud Operators this means they have less downtime and they can scale out with ease





## **Alveo U25 SmartNIC Adapter Features**

#### **Hardware**

- 2x 10/25G ports
- 2x PCle Gen3x8
- SFP28 Direct Attach Copper | SR Optical, Form Factor: HHHL

#### **Acceleration | Low Latency**

- Onload®
- TCP Direct
- Netdev and DPDK Poll Mode Drivers

#### **Baseline NIC Features**

- Stateless and Tunneling Offloads
- LSO/TSO, RSS, Checksum
- SR-IOV, Multiqueue, NetQueue
- 2048 vNICs support

#### Storage

NVMe<sup>™</sup>/TCP (kernel + user space)

#### **Timing & Monitoring**

PTP

#### **FPGA**

- 520K+ LUTs
- Quad ARM A53 Processor Complex
- 6GB DDR4 SDRAM

#### **FPGA Bump-In-The-Wire Acceleration**

- OVS, Encryption, Security ACLs, DPI, etc
- Machine Learning, Video Transcoding, Data Analytics

#### **OS Support**

• Linux

#### **Manageability and Pre-boot**

- PXE, UEFI w/ HII
- MCTP SMbus, MCTP PCIe, and PLDM
- Secure Firmware Upgrade





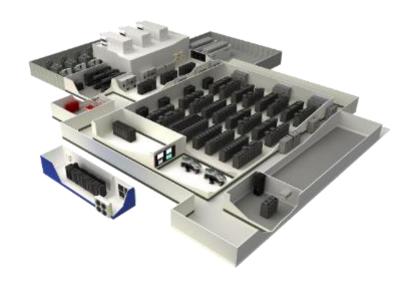
## **Built on Solarflare Technology**

Ultra high performance chips, adapters cards, software and turnkey systems

Deployed in enterprise, telco and cloud data centers







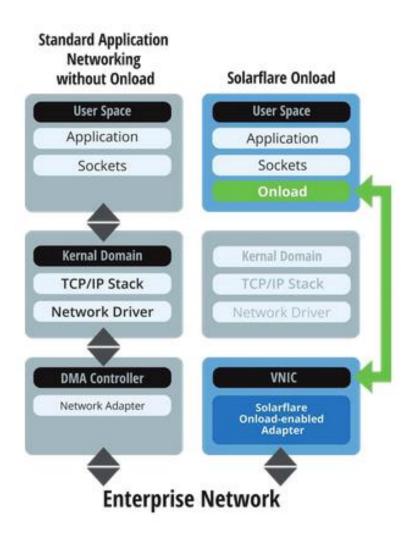








## Onload Technology on every Alveo SmartNIC



#### Why Onload?

- Applications utilizing kernel based networking, are limited in efficiency due to:
  - Large numbers of memory copies
  - Lots of context switching
  - High interrupt rate, and lock contention.
- Onload eliminates Linux networking stack penalties, allowing your application to deliver greater transactions per second (TPS)

#### > How Onload Delivers

- Onload bypasses the kernel and operates in user-space, freeing up CPU cycles for the main application
- Direct connection between applications and networks
- >> Onload enables fast connect and disconnect times allowing for greater connectivity, supporting industry-standard TCP/IP stack.

#### > Seamlessly integrates into existing infrastructures:

- Binary compatible with industry-standard POSIX interfaces APIs
- No software modifications needed Install and Go

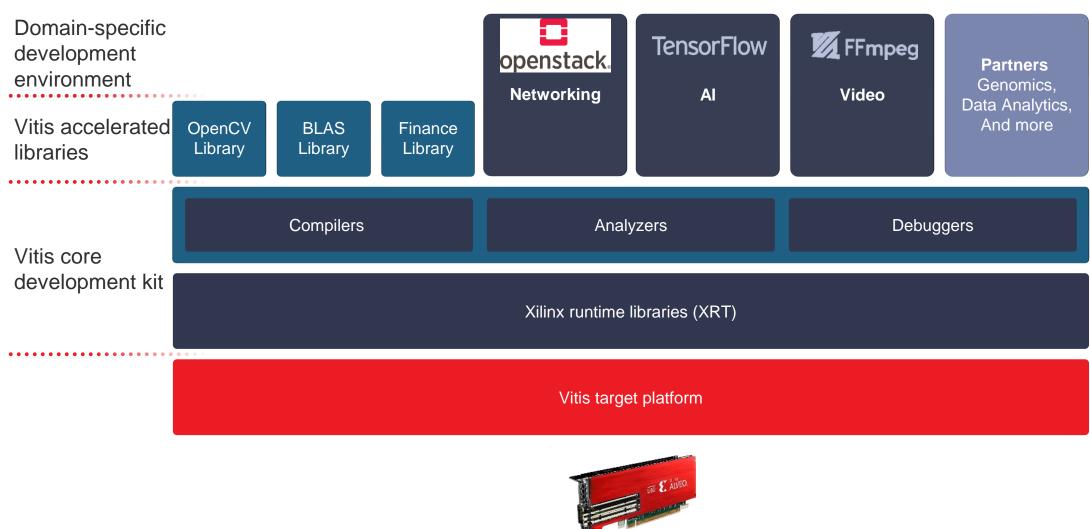
#### Improves Latency and Performance

- Reduced latency by 80% compared to standard kernel methods
- Near zero jitter
- Improves TCP based application performance by up to 400%

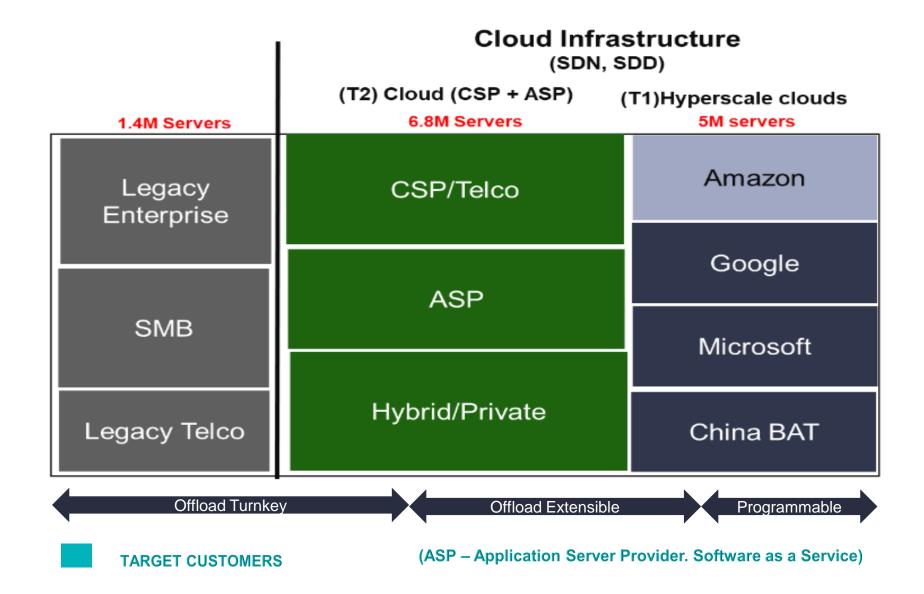


### **SmartNIC Platform Stack**

Python, C++, C, P4, RTL



## **Target End Users**





## **New OCP Form Factor Base Products**



## New XtremeScale™ X2562 First OCP 3.0 Form Factor Ethernet Adapter





## X2562 | 10/25GbE OCP 3.0 SFP28 Network Adapter

#### **Hardware**

- 2x 10/25G ports
- OCP 3.0
- SFP28 Direct Attach Copper | Optical support, AOC (future)
- Intelligent Auto Negotiation

#### **Acceleration | Low Latency**

- Onload (with PLUS SKU)
- TCP Direct (with PLUS SKU)
- DPDK Poll Mode Driver

#### Virtualization

Stateless and Tunneling Offloads SR-IOV, Multiqueue, NetQueue 2048 vNICs support

#### **Storage**

NVMe/TCP kernel NVMe/TCP user space compatible

#### **Security**

ServerLock™ compatible

#### **Timing & Monitoring**

- PTP (with PLUS SKU)
- Hardware timestamping
- SolarCapture™ Pro

#### **Manageability and Pre-boot**

- PXE, UEFI w/ HII
- MCTP SMbus, MCTP PCIe VDM, NC-SI and PLDM
- Secure Firmware Upgrade

#### **OS Support**

Linux, VMware, Windows

#### **Availability**

- Limited Sampling Now; GA: Q2-2020
- X2562, X2562-PLUS SKUs

#### **Target Solutions (Application):**

- Fintech (ET/HFT)
- Software Load Balancer
- Message Brokers
- In Memory DB
- WEB/App Hosting
- Content Delivery Networks
- DNS / Routers



## OpenCompute Accelerator Module (OAM)

Reference Architecture



## World's First FPGA Based OpenCompute Accelerator Module (OAM) Reference Architecture



- Powerful Virtex<sup>®</sup> UltraScale+<sup>™</sup> FPGA with 8GB of HBM Memory
- Seven 25Gbps x8 Links Enable Rich Inter-module System Topologies
- Compliant with Open Accelerator Infrastructure (OAI)





## Thank You

