Introducing the Vitis Unified Software Platform



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Learn Directly From Experts HOURS OF TECHNICAL SESSIONS **IN 6 TRACKS**

LABS **AVAILABLE FOR 20 HOURS**

DEMOS

18 Xilinx Demos, 39 Partners, 12 Alveo Demos (Partners)

XDF 2019

Heterogeneous Compute





Cloud to Edge



Al Proliferation

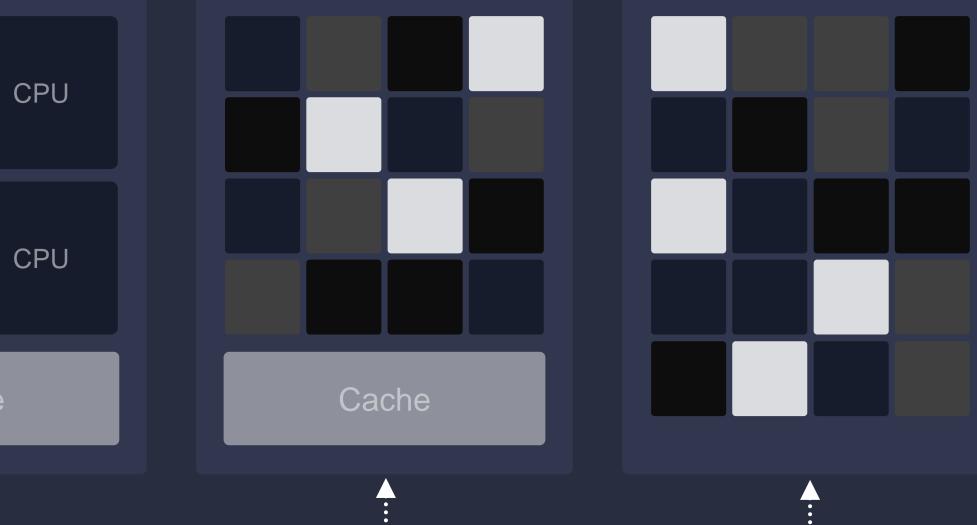
Industry Trend: Heterogeneous Compute

Heterogeneous Compute

Engines Customized to Accelerate Specific Domains

CPU CPU Cache

Domain-Specific Accelerator 1



Domain-Specific

Accelerator 2

Key Challenge Programming & integration of Adaptive Acceleration Engines

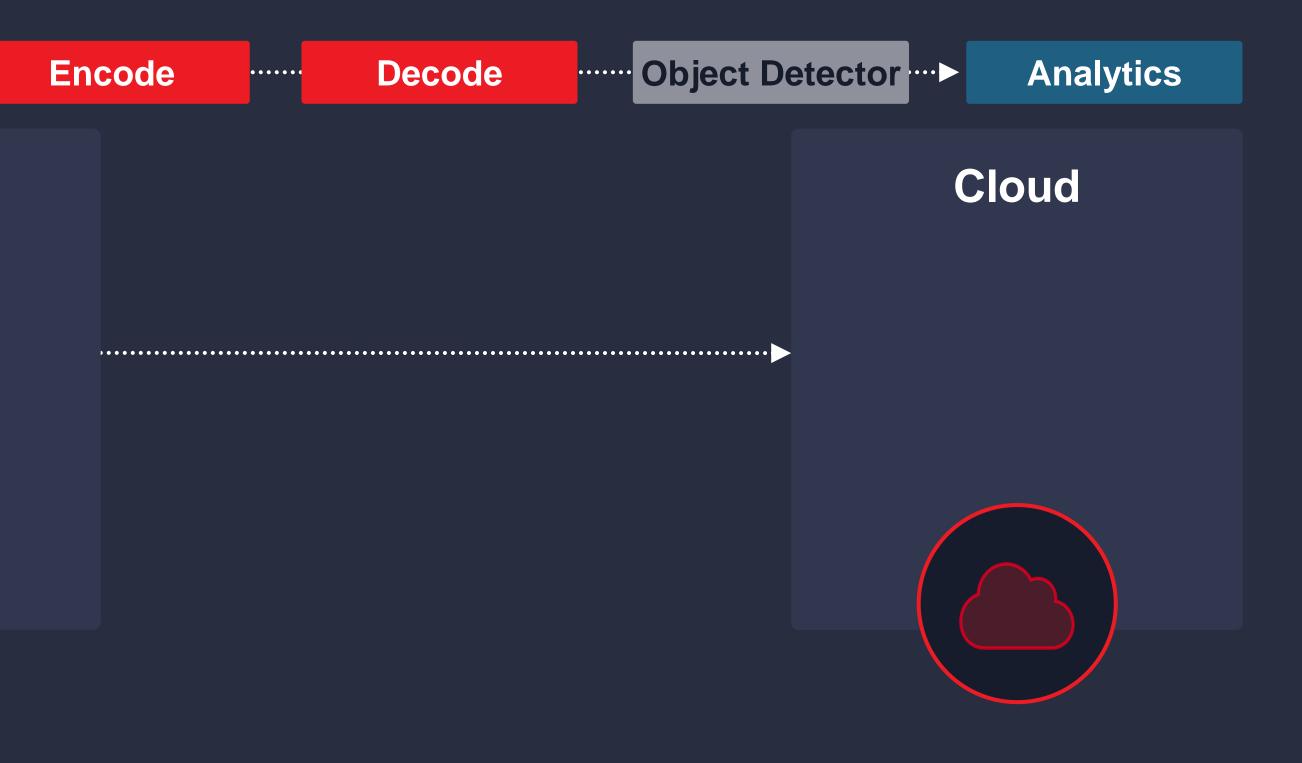


Camera

Cloud to Edge

Applications are often split between cloud and edge

Endpoint





Cloud to Edge

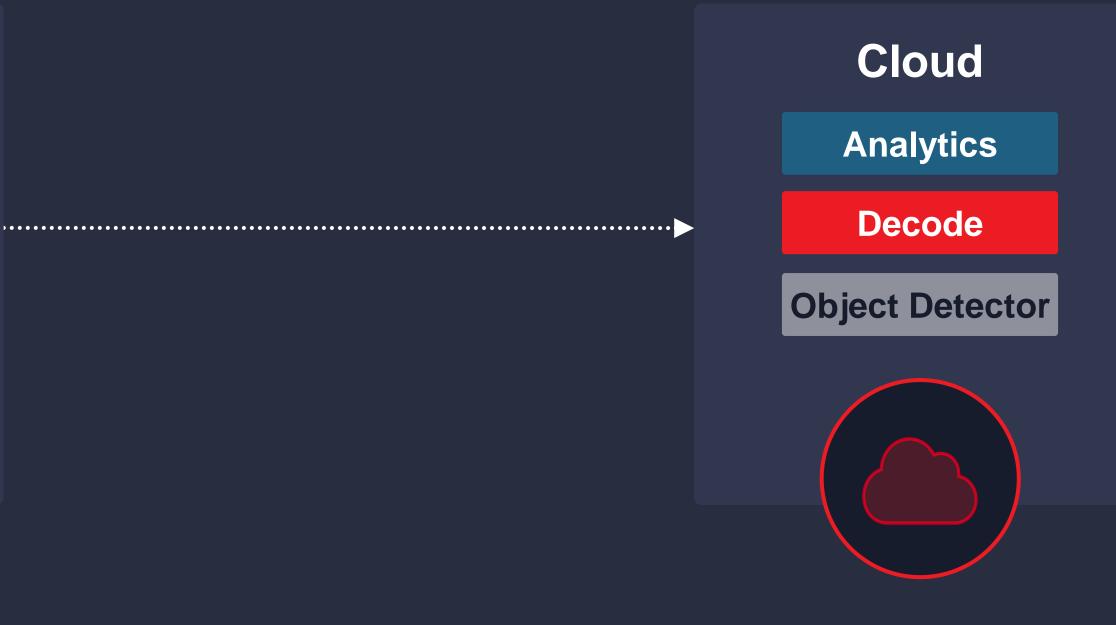
Applications are often split between cloud and edge



Encode









Cloud to Edge

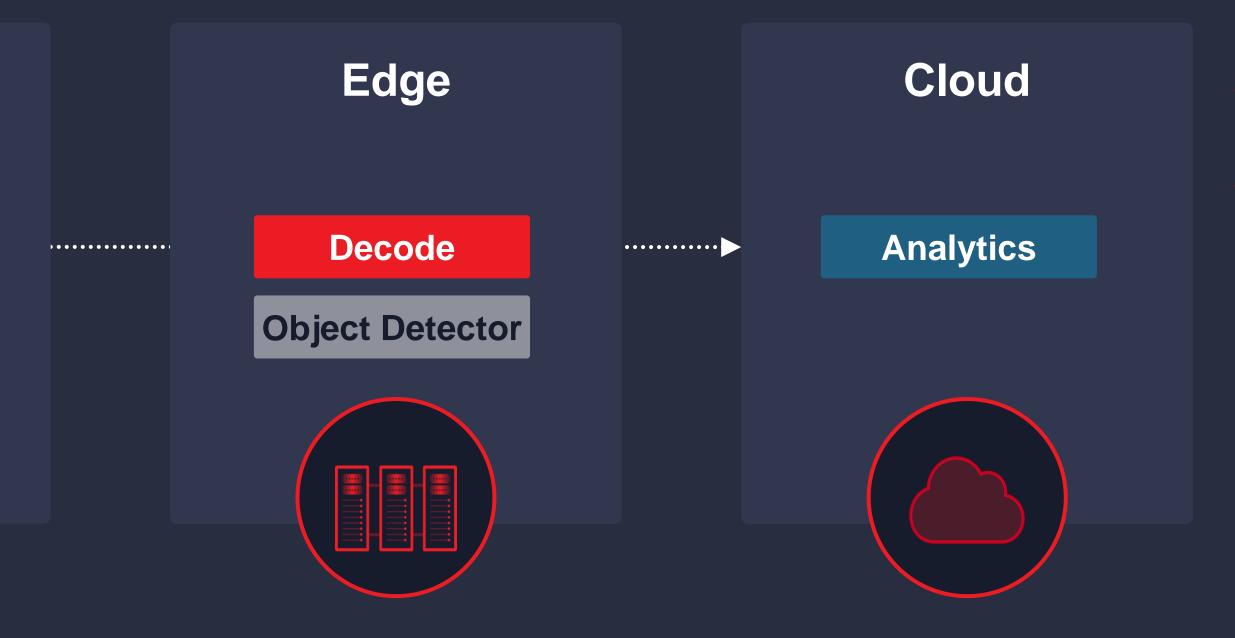
Applications are often split between cloud and edge



Encode







Key Challenge Need for Retargetability

Cloud to Edge

Applications are often split between cloud and edge

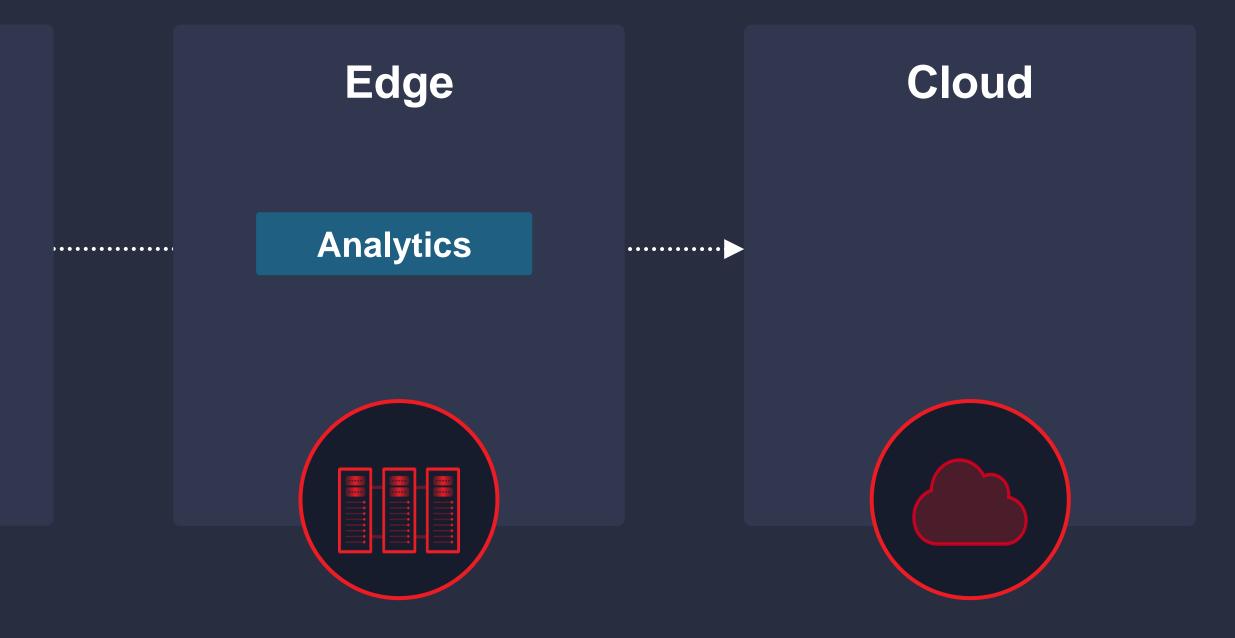
Endpoint

Camera

Object Detector







Key Challenge Need for Retargetability

Industry Trend: AI Proliferation

AI Proliferation



Smart City

Genomics

Al is being used in many applications









Smart Retail

Autonomous Driving

Security



Video Analytics



Healthcare



Finance

Key Challenge Acceleration and Integration of the Whole Application

Heterogeneous Compute

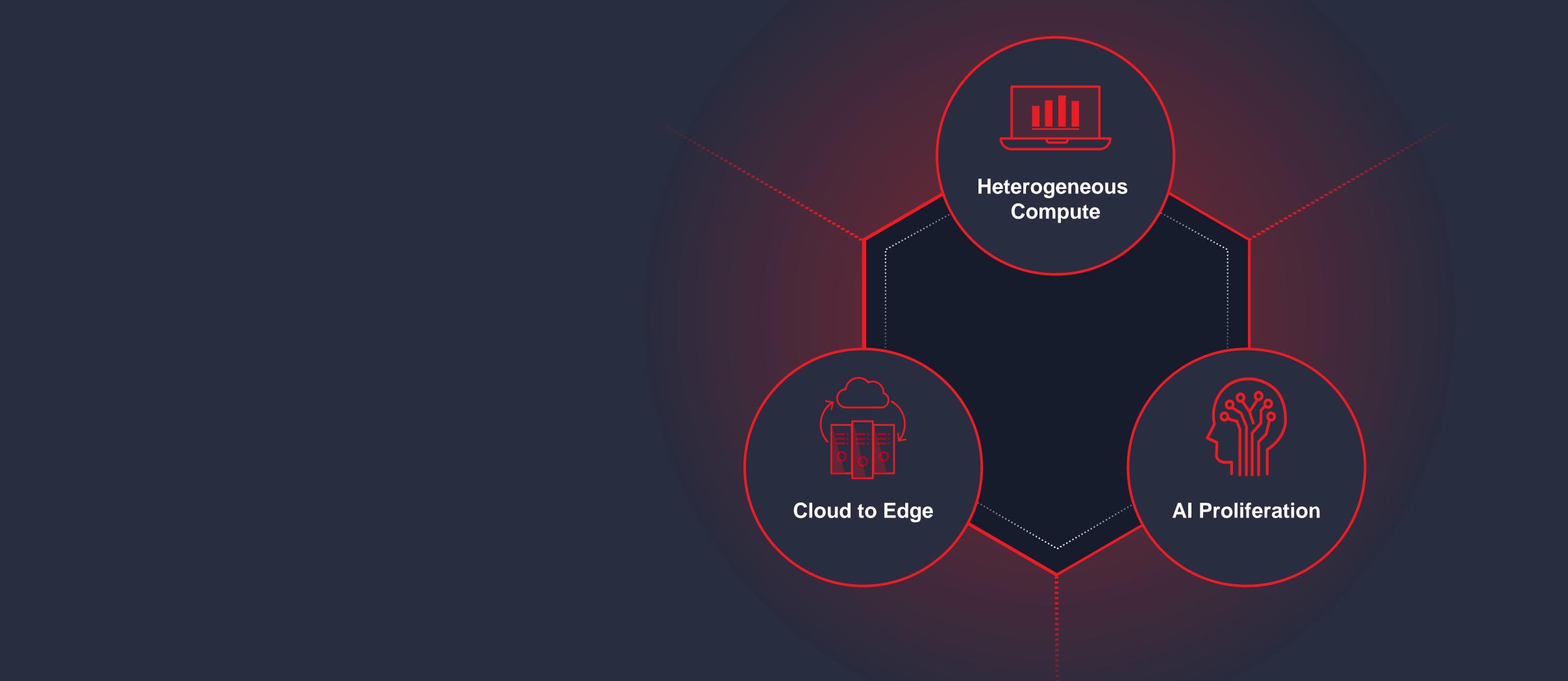




Cloud to Edge



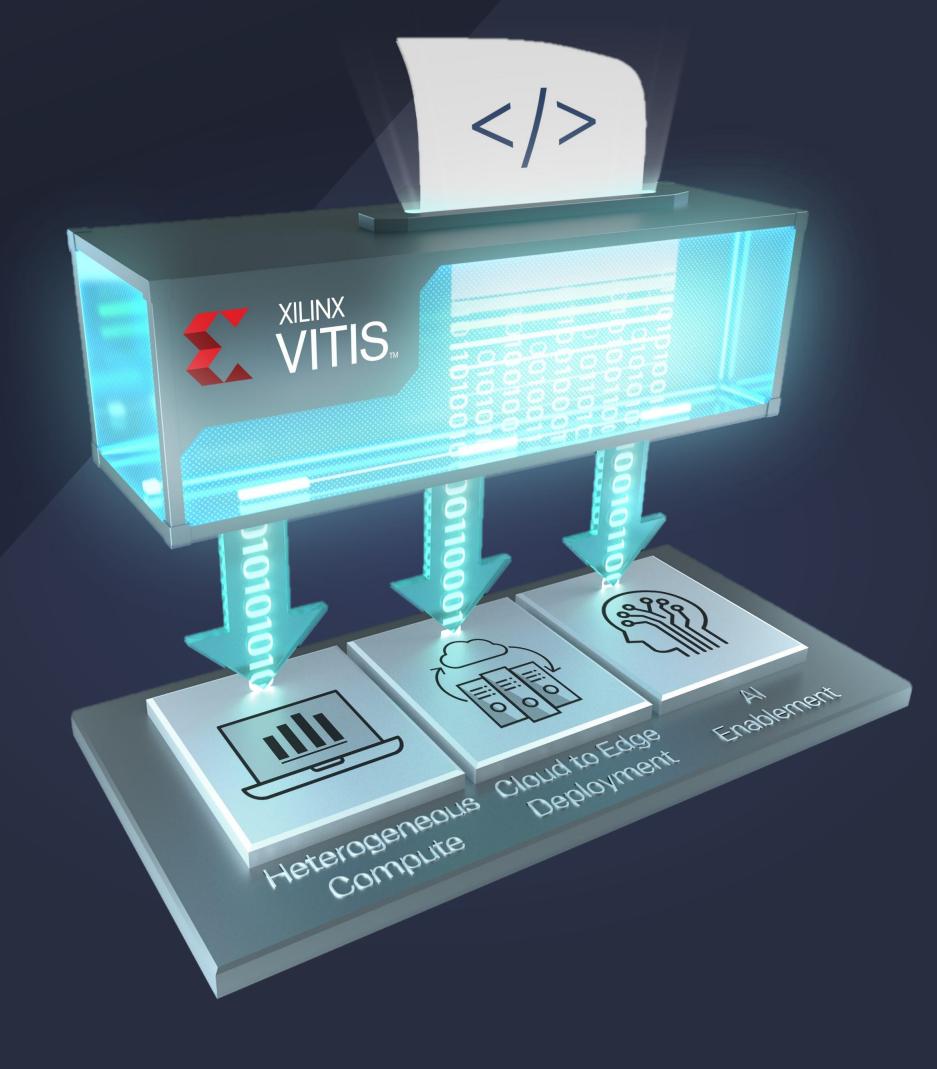
Al Proliferation



Vitis Unified Software Platform

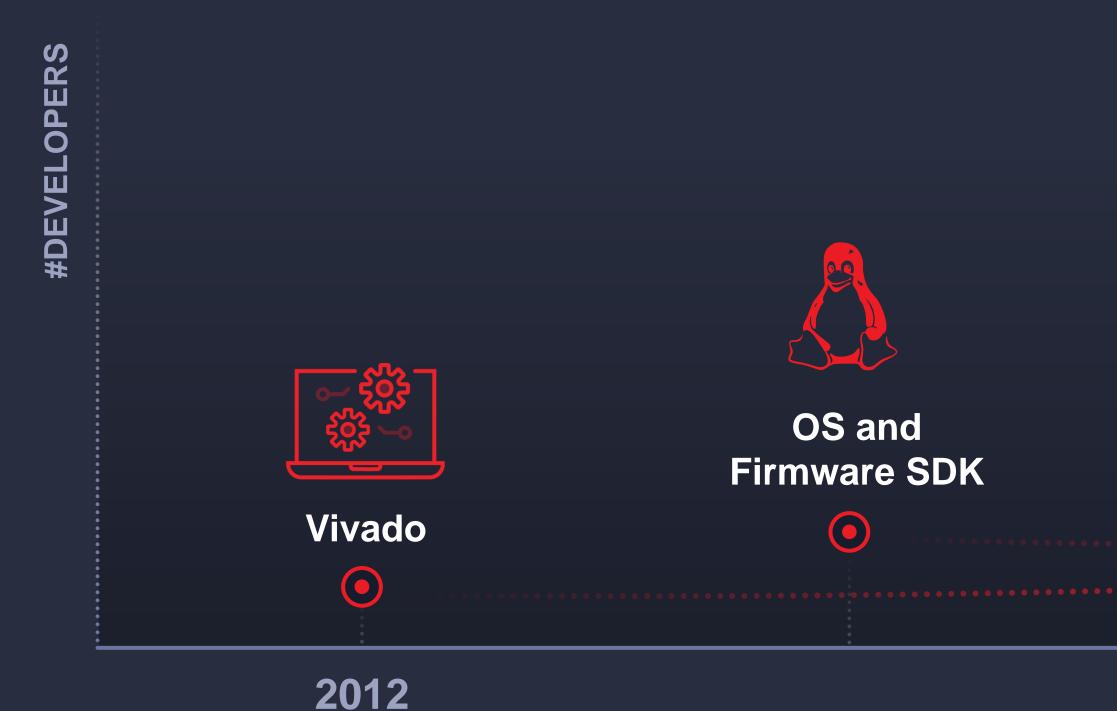


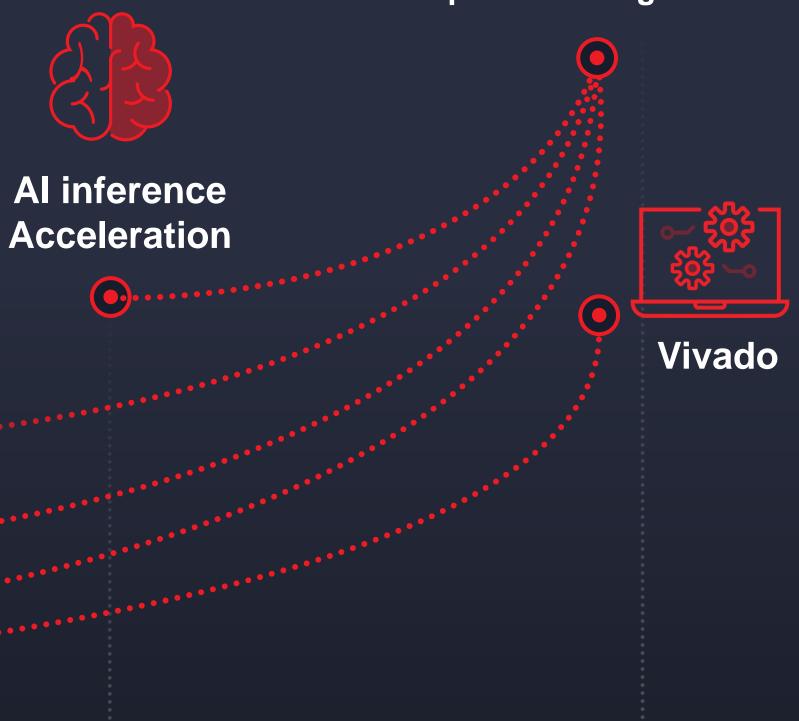






Platform Transformation









SDAccel, Data Center (FaaS, Alveo)

SDSoC, Embedded

Vitis Unified **Software Platform** Adaptable & Programmable



Build

Enables all Developers to Build and Deploy to All Platforms







Embedded Developers

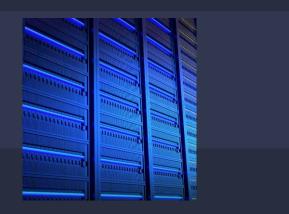
Enterprise **Application Developers**

Enterprise Infrastructure Developers



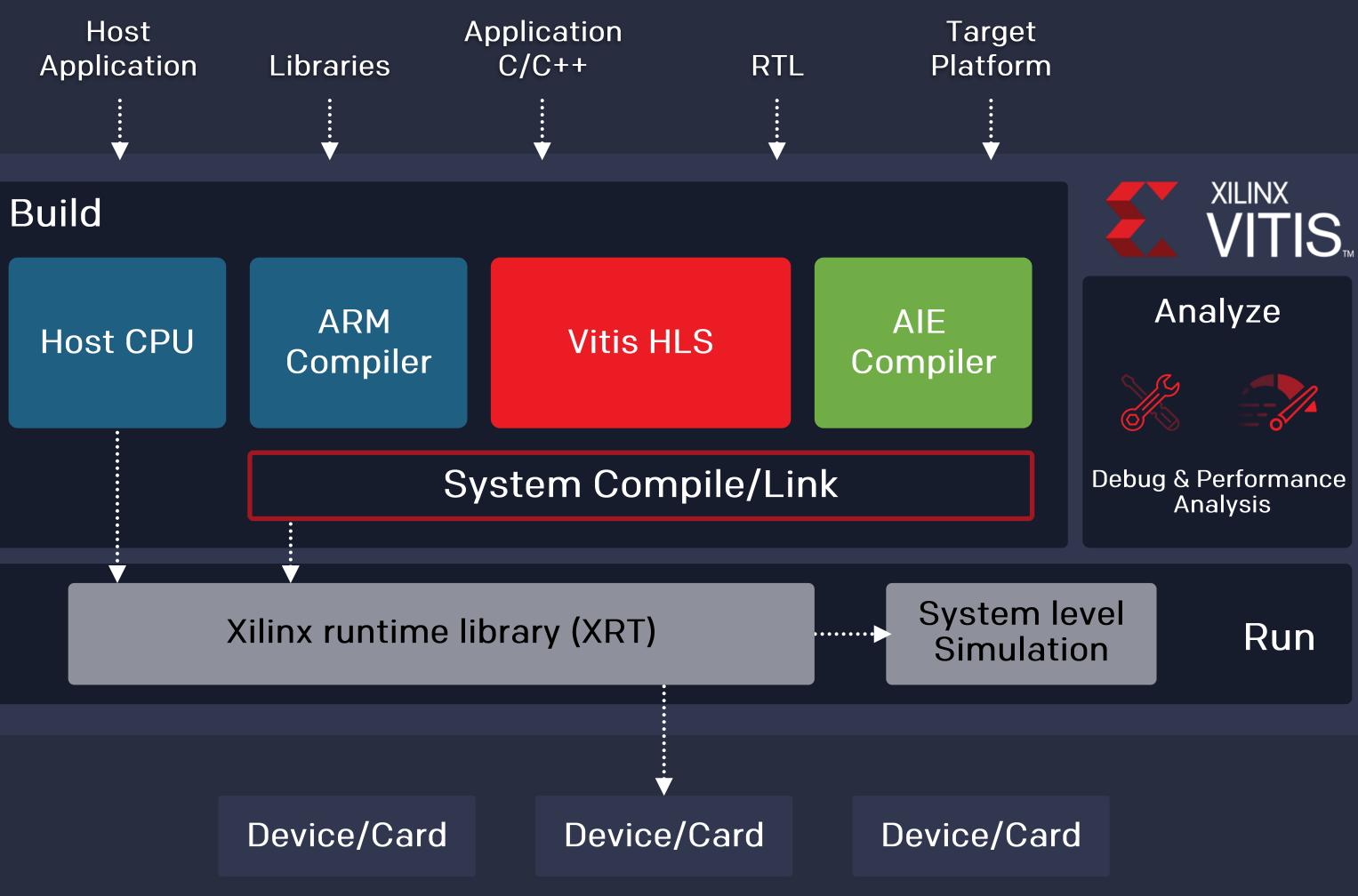


Data & Al Scientists



Data Center Rack

Build Comprehensive Development **Tool Suite**









Build Comprehensive Development **Tool Suite**







Vision & Image



Math

400+ functions across multiple libraries Open-Source, performance-optimized out-of-the-box acceleration

Domain-Specific Libraries



Finance

Data Analytics & Database

Data Compression

Common Libraries



Linear Algebra



Statistics

DSP





Data Security

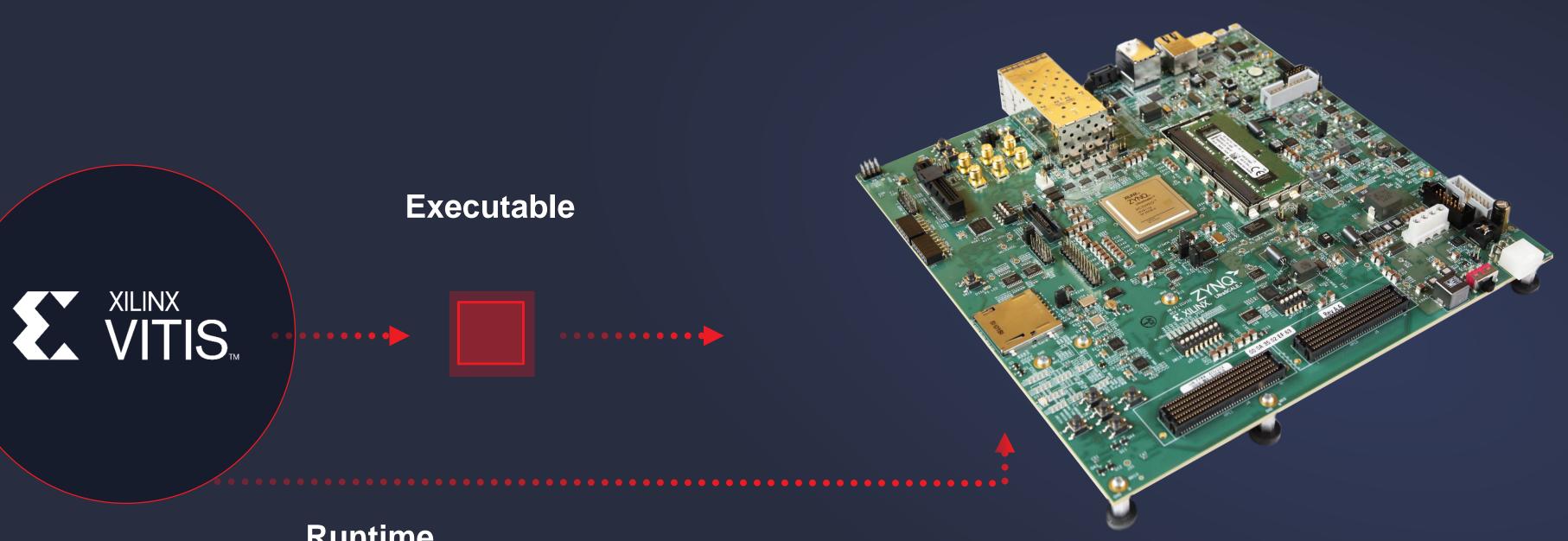


Data Management

Deploy Embedded Deployment





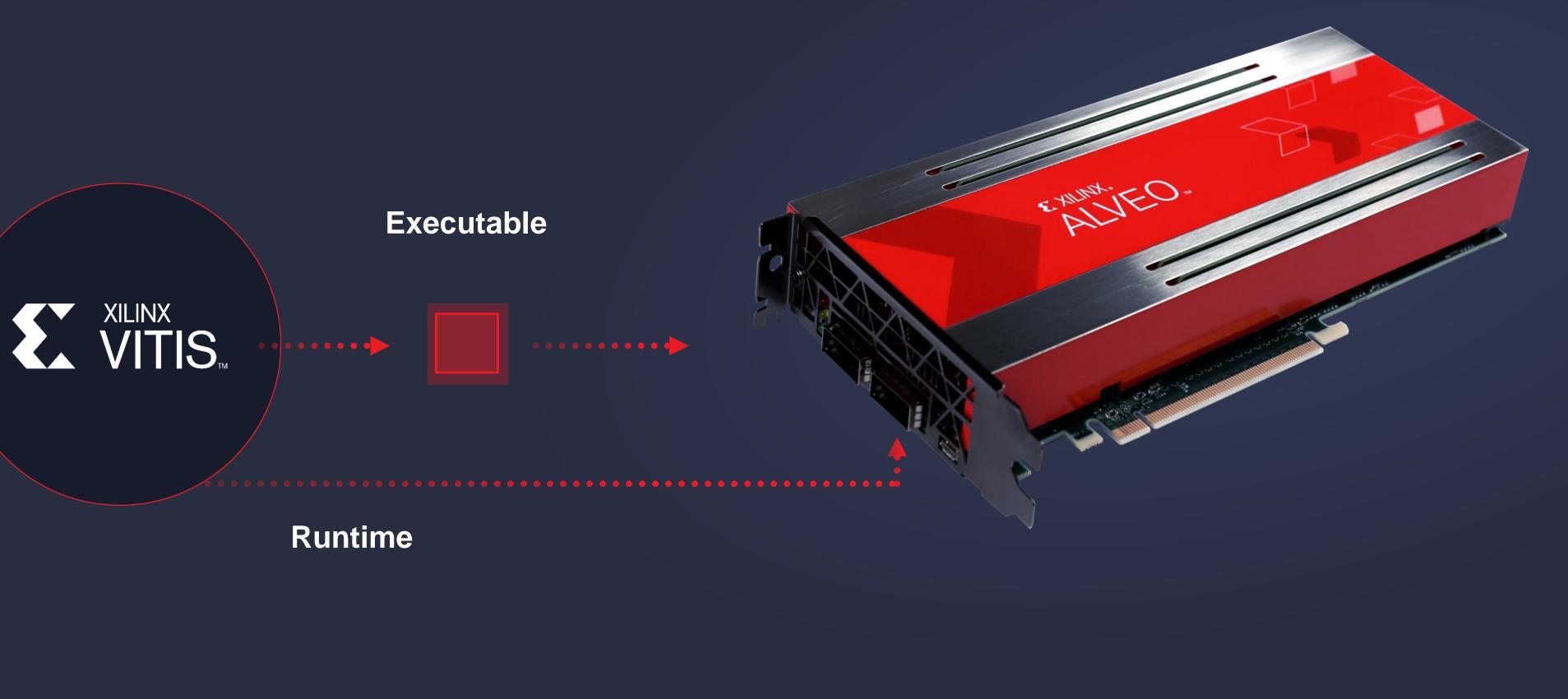


Runtime

Deploy Single Server Deployment



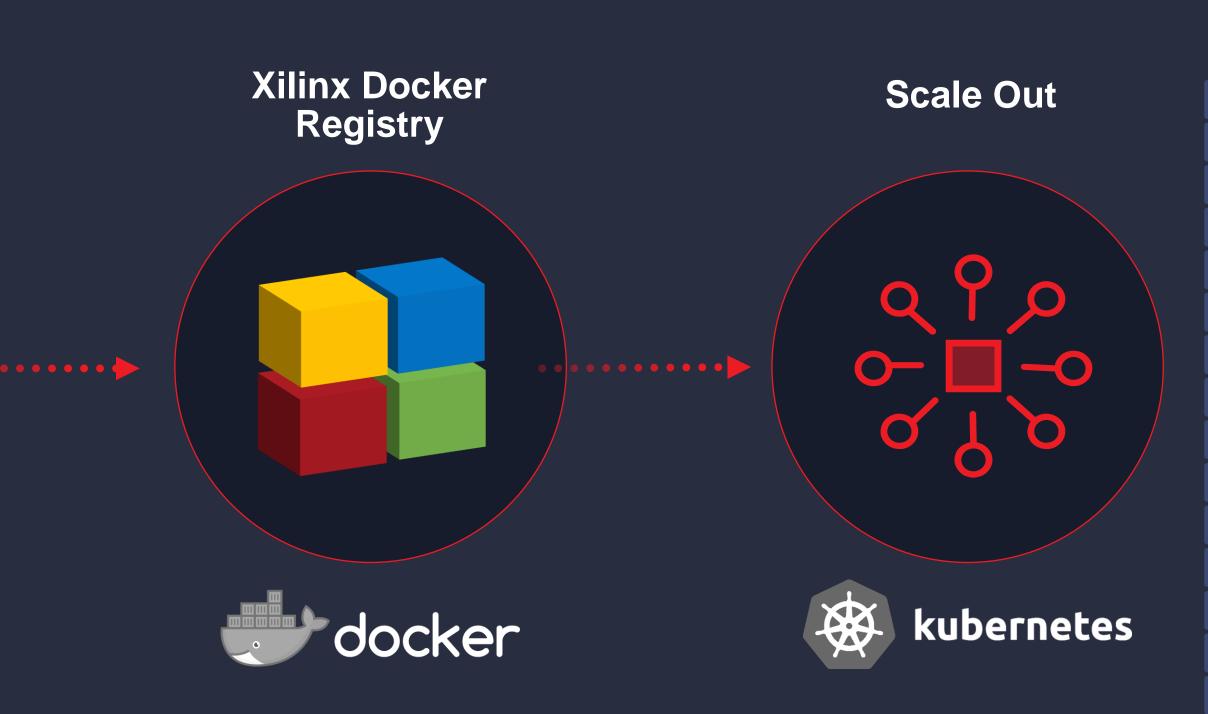


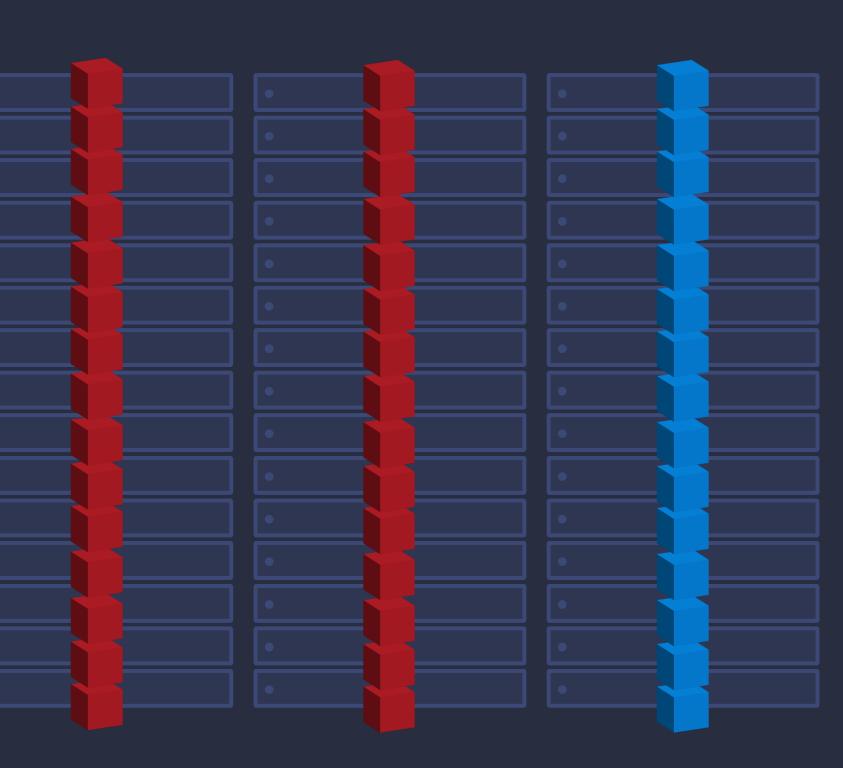


Deploy Executable Scale Out Deployment

Runtime







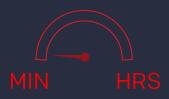
Vitis AI: From TensorFlow to Implementation in Minutes



DNN Processing Unit (DPU)

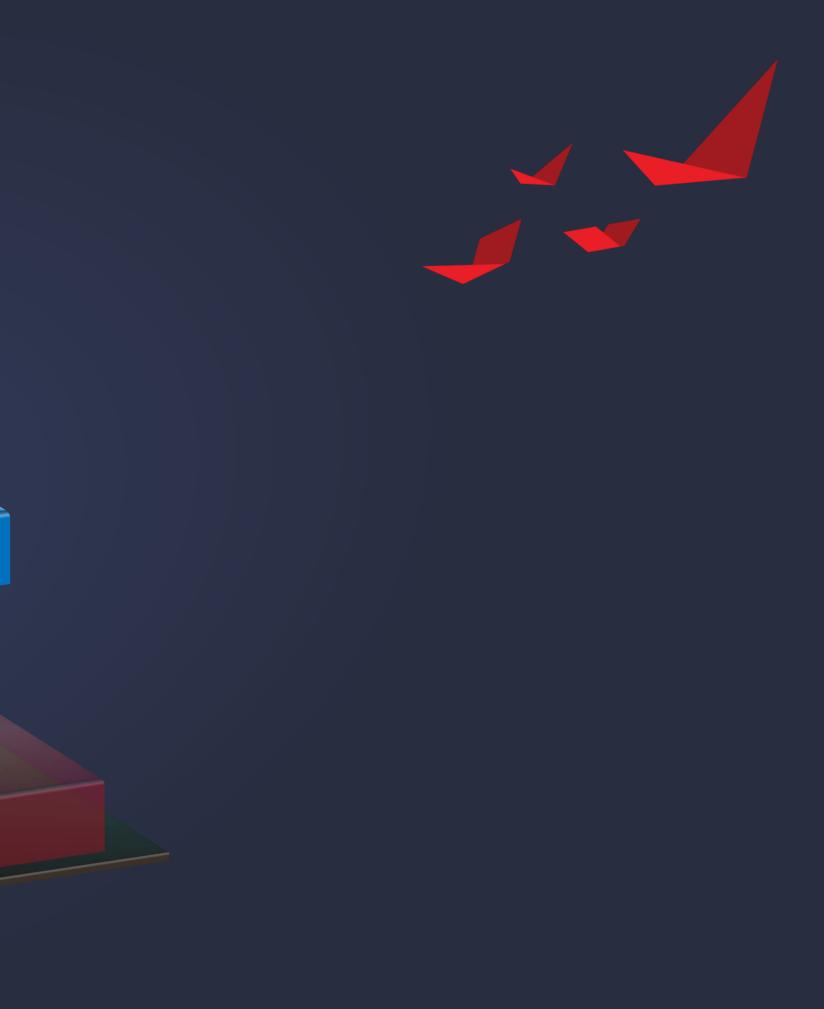


Direct Framework Compilation



Minutes of Compile Times

Adaptive Device DPU



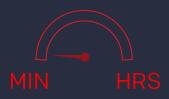
Vitis AI: From TensorFlow to Implementation in Minutes



DNN Processing Unit (DPU)



Direct Framework Compilation



Minutes of Compile Times



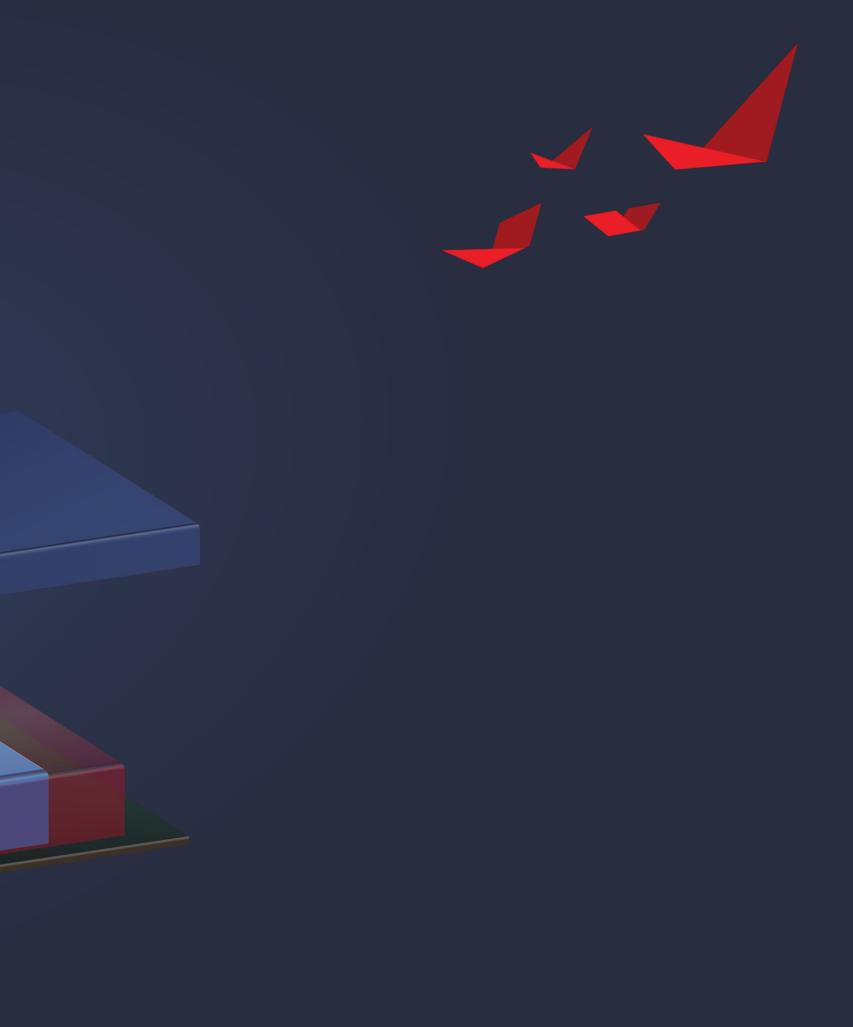








DPU



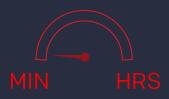
Vitis AI: From TensorFlow to Implementation in Minutes



DNN Processing Unit (DPU)



Direct Framework Compilation



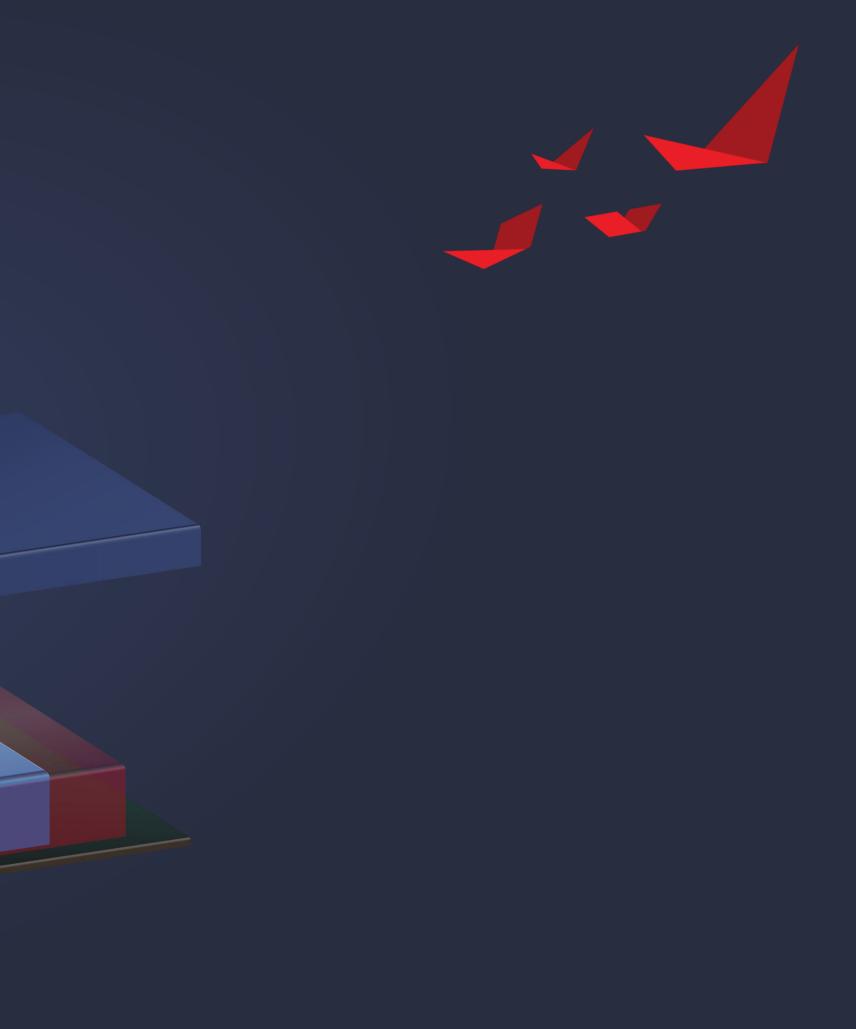
Minutes of Compile Times





Vitis Al

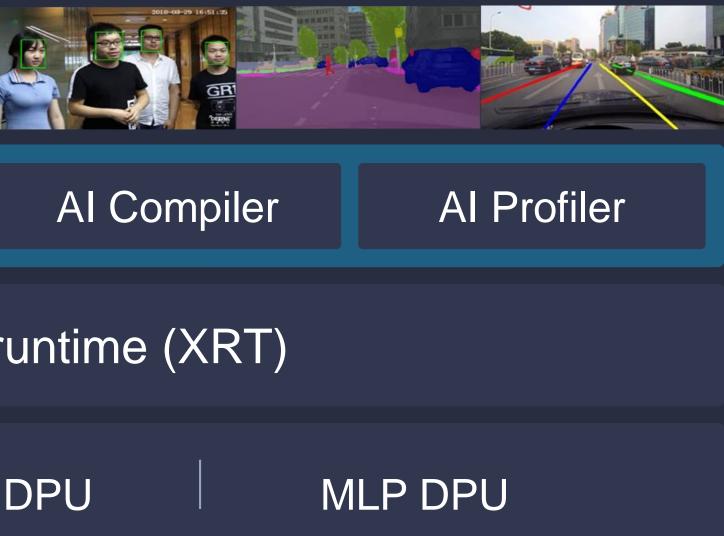
Adaptive Device



Enabling Al

Frameworks	Tenso	orFlow	Caf
Vitis Al Models			
Vitis Al Development Kit	AI Optimizer	Al Quan	tizer
		Vitis dri	vers & rui
DSA	CNN DP	U	LSTM D

ffe ⁽) PyTorch



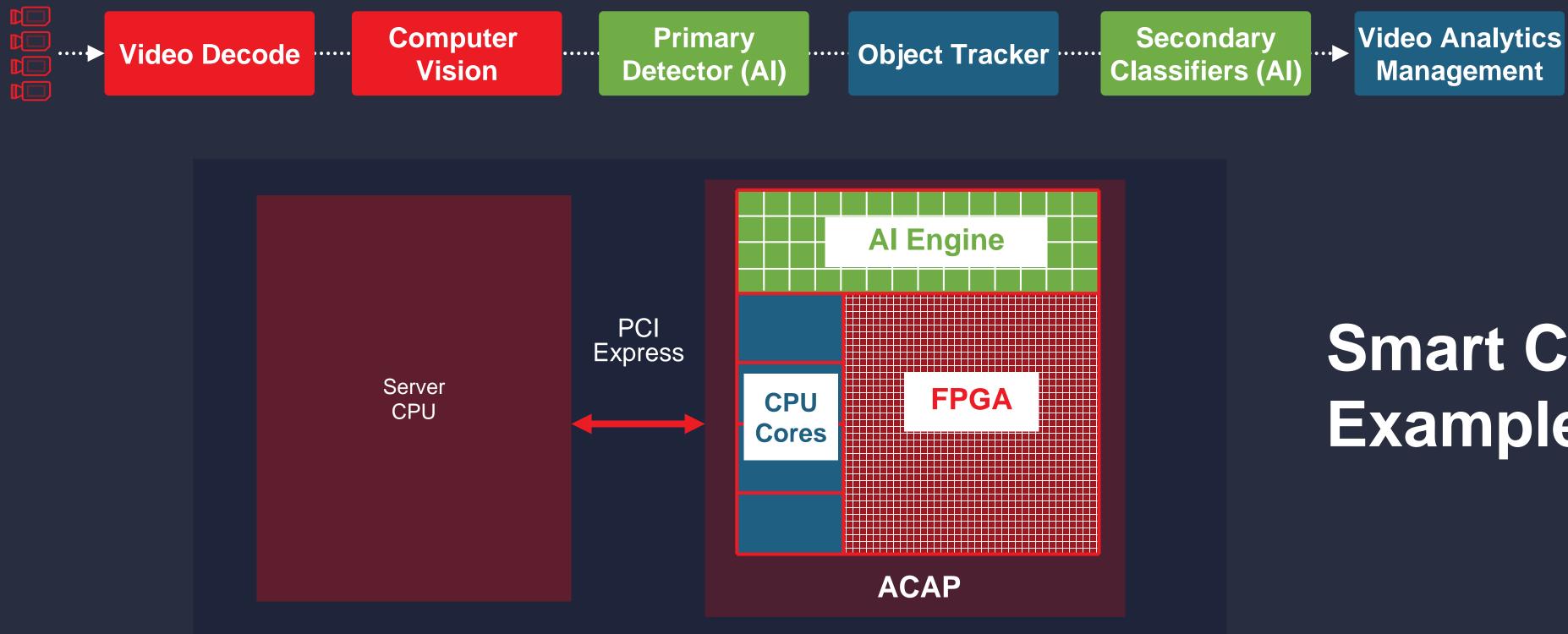
30+ pretrained, optimized reference models

programmability



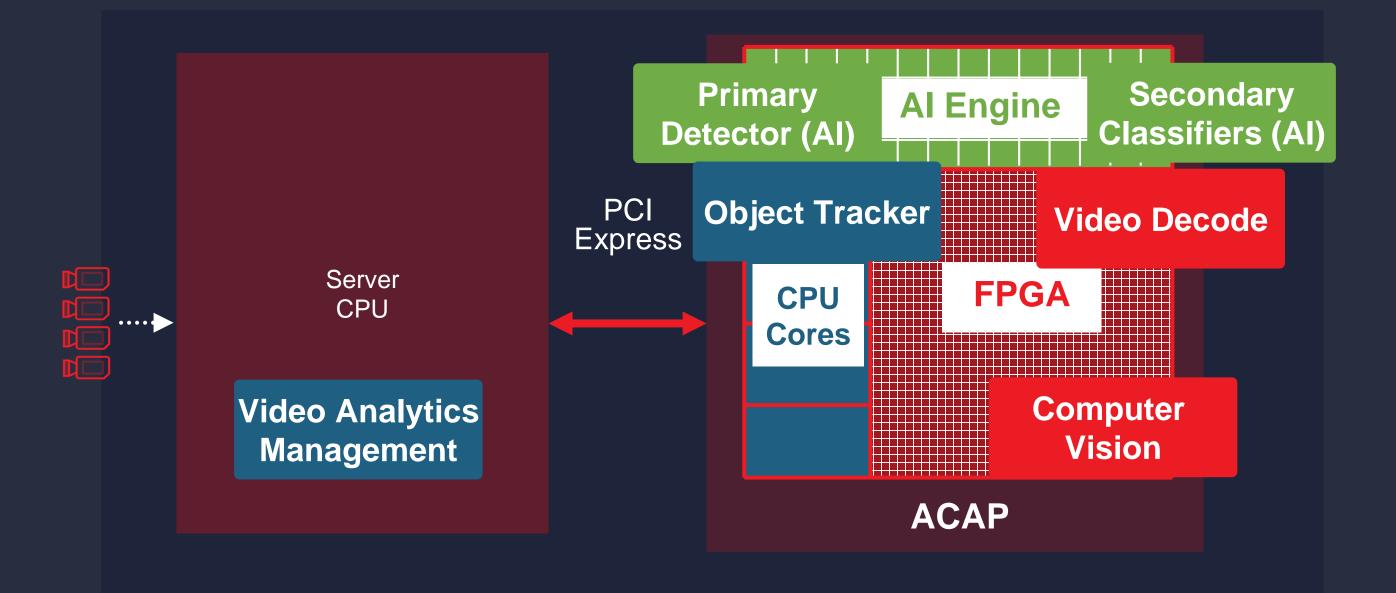
Performance improvement up to 10-20x

Tensor based ISA for true software

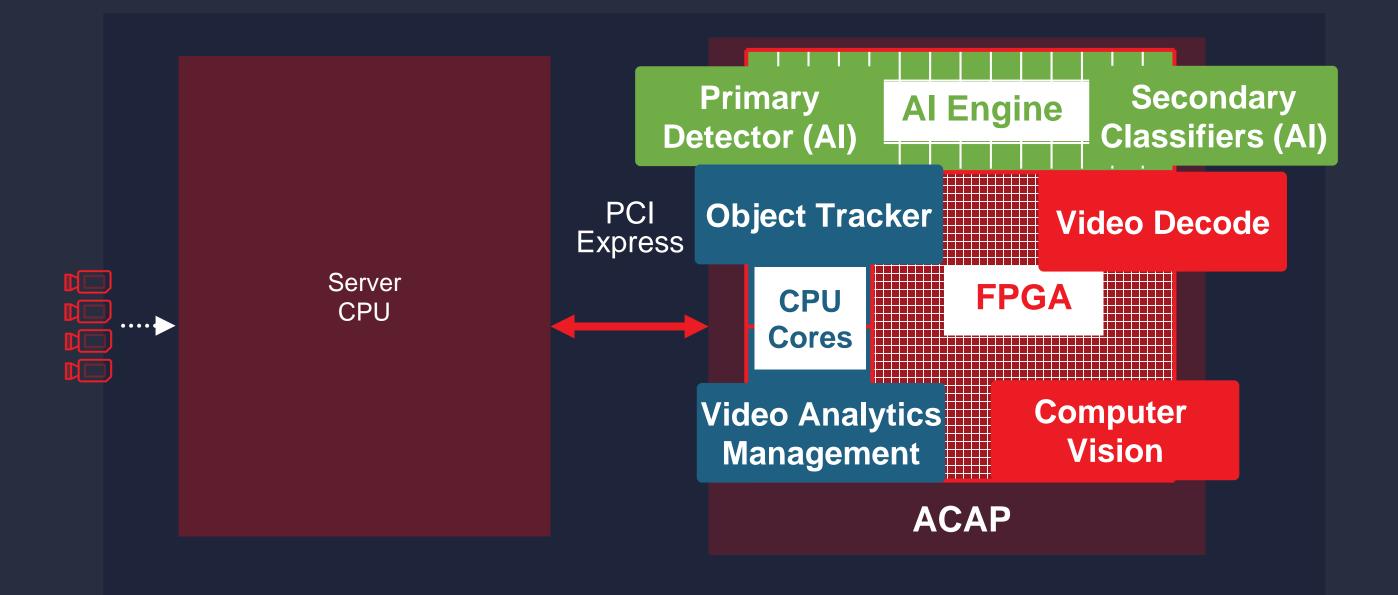




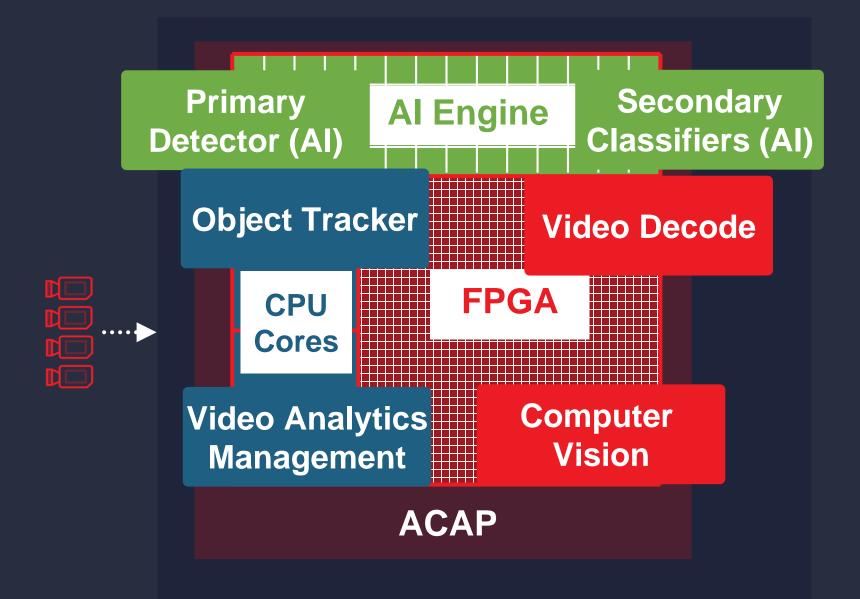




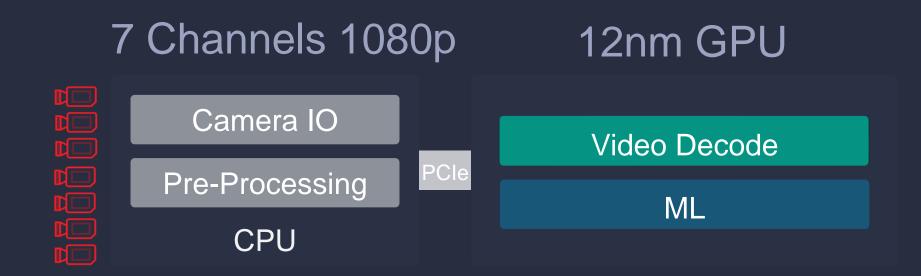








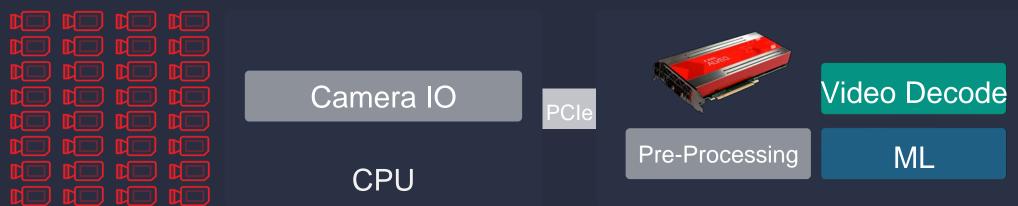
Impact of Whole Application Acceleration



> 4.5x throughput > 1/6 latency

32 Channels 1080p

Versal ACAP



Source: Xilinx Analysis GPU – Nvidia T4. DeepStream 4.0 running on T4 in GCP

Decode Detect + Classify

Decode Detect + Classify

Launching developer.xilinx.com

Beta Site Now Available

Tutorials, Articles & Projects

Accessible from a Single Location

Learn Directly from Vitis Experts



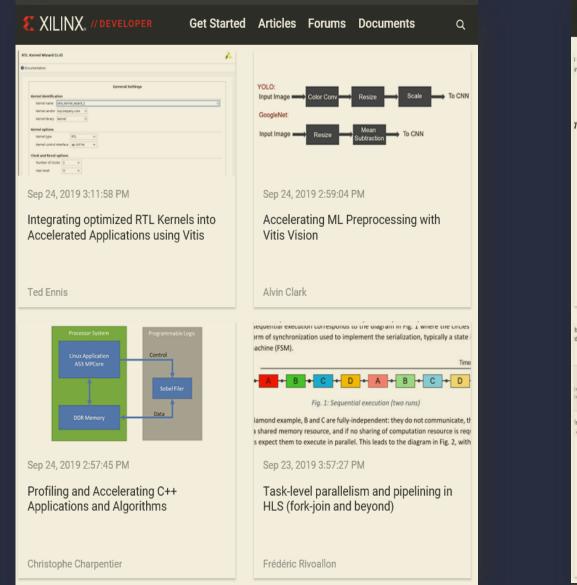
XILINX, // developer	Get Started	Articles Forums	s Doc
	LUINCE	40.12	
	FPN	64.29	
	Unet-Full	14.27	
	Unet-Lite	36.25	
Using data gathered throughout this tut from section 4.1. Albeit, this isn't a fair of 1. We are comparing an embedded 2. The ZCU102 execution time includ inference time of the models	comparison for two reasons: ~20W device with a 225W GPU		
		funth an understanding. The fel	
That said, this still provides some data p measured on the ZCU102 vs. the GTX10	· · · · · ·	Turther understanding. The foi	lowing chart show
120			
100			
80			Values
60			ZCU102 (FF
00			Display@1
40			
			Floating Pc
20			
20			Floating Pc
20	ESPNet FPN	Unet-Full Unet-lite	Floating Po

0 Enet ESPNet FPN Unet-Full Unet-Lite What is perhaps a bit more useful than comparing raw FPS, however, is to compare FPS/W (performance/Watt) as this is

performance is achievable for a certain power cost. Bear in mind, this is still not a fair comparison due to reason 2, but th little more in this light. In reality the advantage is even more pronounced if only the DPU throughput is considered.

In order to perform this comparison, ~20W was measured on the ZCU102 board during forward inference, and the nvidia-s during forward inference of each of the models as part of section 4.1. The comparison between the two can be seen in th





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🚺 XILINX. Get Started Articles Forums Documents umbers. Specifically, it is a measure of the cosine of angle between two vec orm of synchronization used to implement the serialization, typically a ilar) to 180 degrees (most dissimilar). Accordingly, cosine of the angle (cos θ) (achine (FSM). A·B rity(A,B) =AXB amond example. B and C are fully-independent: they do not shared memory resource, and if no sharing of computation resource is expect them to execute in parallel. This leads to the diagram in Fig. 2, w Sep 24, 2019 1:13:57 PM Sep 23, 2019 3:57:27 PM Cosine Similarity Using Xilinx Alveo Task-level parallelism and pipelining in HLS (fork-join and beyond) Alvin Clark , Kumar Deepak , Liang Ma Frédéric Rivoallon

ore, we'll configure the library (in the hardware, via tempiates in our hardware source are algorithm is no^m₀₀ equivalent to listing 3.21 in standard OpenCV: Listing 3.21: Example & Bilateral Resize an

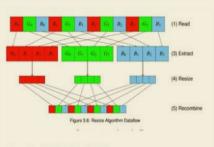
re resizing as in Example 7, and as we mentioned are applying a 7×7 window to the Ga

image, resize_ocv, cv::Size(out_width, out_height), 0, 0, CV_INTER_LIN nBlur(resize_ocv, result_ocv, cv::Size(7, 7), 3.0f, 3.0f, cv::BORDER_C

Sep 23, 2019 3:31:04 PM

Get Moving with Alveo: Example 8 Pipelining Operations with OpenCV

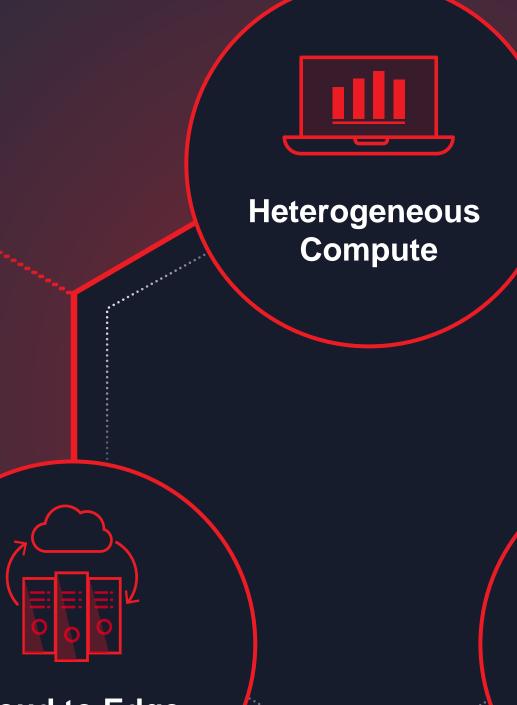
Rob Armstrong



Sep 23, 2019 3:30:44 PM

Get Moving with Alveo: Example 7 Image Resizing with OpenCV

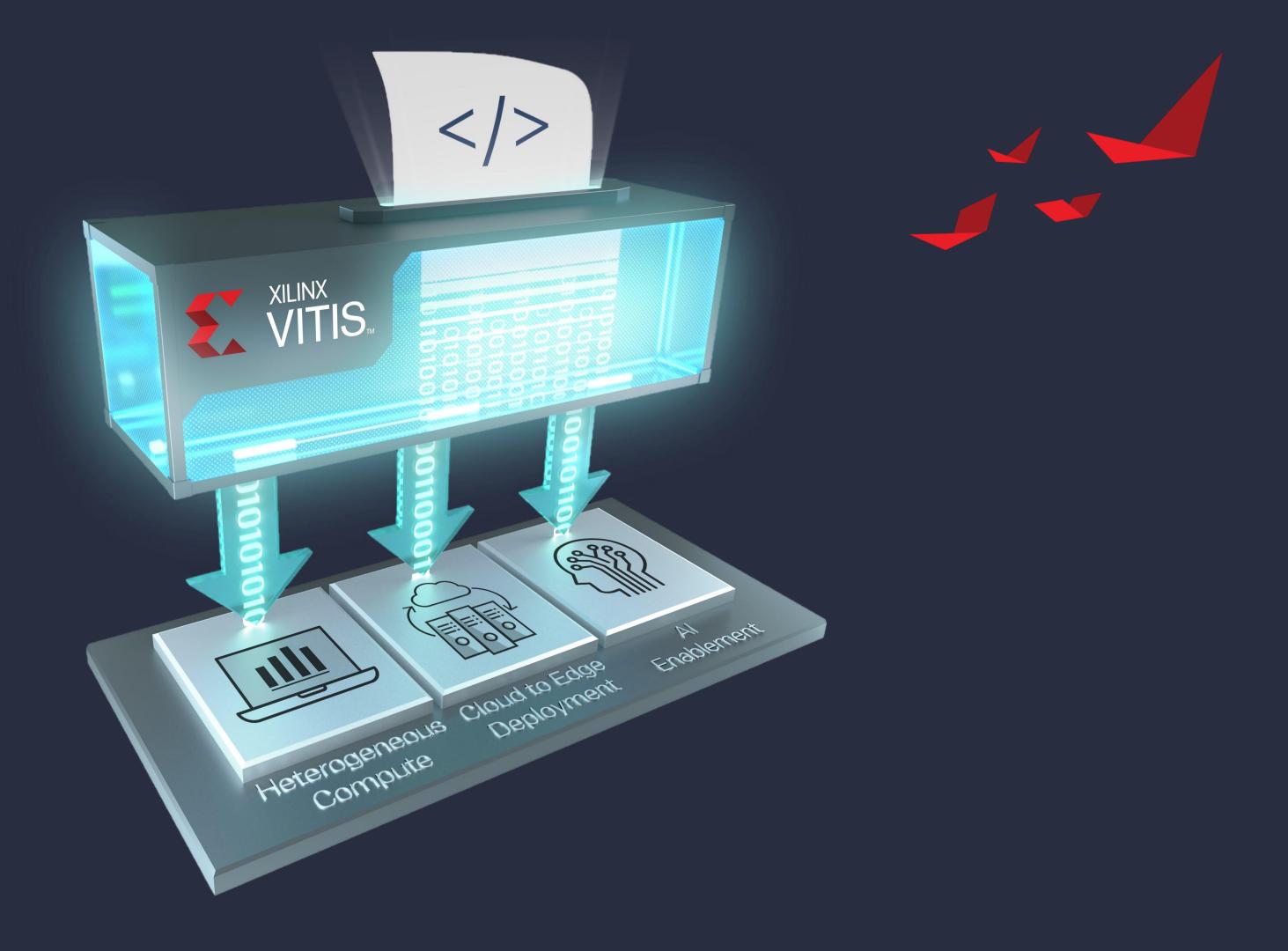
Rob Armstrong



Cloud to Edge



AI Proliferation





Sumit Gupta Vice President of Product AI/ML & HPC





Tom Eby SVP & GM, Compute & Networking Business Unit, Micron Technology



Development Platforms for ALL Developers

• Unified

Open Source Libraries

Free!

Embedded / **SoC Developers** Application Software **Developers**

Hardware Developers

AI & Data **Scientists**

